DIODES
INCORPORATED

Lead-free Green

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

NEW PRODUCT

Description

The 74HCT164 is a serial input 8-bit edge-triggered shift register that has outputs from each of eight stages.

SERIAL DATA INPUT PINS
The serial input data is entered at pin SDA or pin SDB as these are logically ANDED. Either input could be used as an active HIGH enable with data entry on the other pin. If a single input is desired, the pins can be tied together or the unused input can be tied HIGH.

DATA ENTRY
Data is shifted into Q0 from the serial input pins on each LOW to HIGH transition of the CP pin. Also during the CP edge the data is transferred from each Qn to Qn+1. The serial data on pins DSA and DSB must be stable before and after the CP rising edge to meet the set-up and hold timing requirements.

RESET
When asserted LOW the Master Reset ($\overline{MR}$) pin sets all Qn to LOW. This action does not depend on the condition of serial input or clock pins. The $\overline{MR}$ must be asserted HIGH for a recovery time before the next CP positive edge pulse.

Pin Assignments

(Top View)

Pin		Pin
DSA	1	14 Vcc
DSB	2	13 Q7
Q0	3	12 Q6
Q1	4	11 Q5
Q2	5	10 Q4
Q3	6	9 $\overline{MR}$
GND	7	8 CP

SO-14 / TSSOP-14 / PDIP-14*
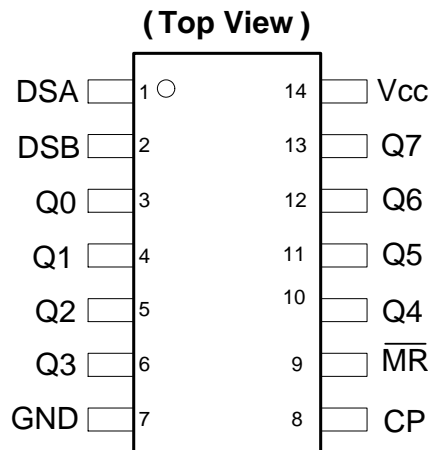
*PDIP-14 is a future product

Features

- Supply Voltage Range from 4.5V to 5.5V
- Sinks or Sources 4mA at V_{CC} = 4.5V
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- TTL Compatible
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115)
  - 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- General Purpose Logic
- Wide Array of Products Such as:
  - PCs, Networking, Notebooks, Netbooks
  - Computer Peripherals, Hard Drives, CD/DVD ROM
  - TV, DVD, DVR, Set-Top Box

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Device ordering information is on page 7

74HCT164
Document number: DS36280 Rev. 1 - 2

1 of 10
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NEW PRODUCT

Pin Descriptions

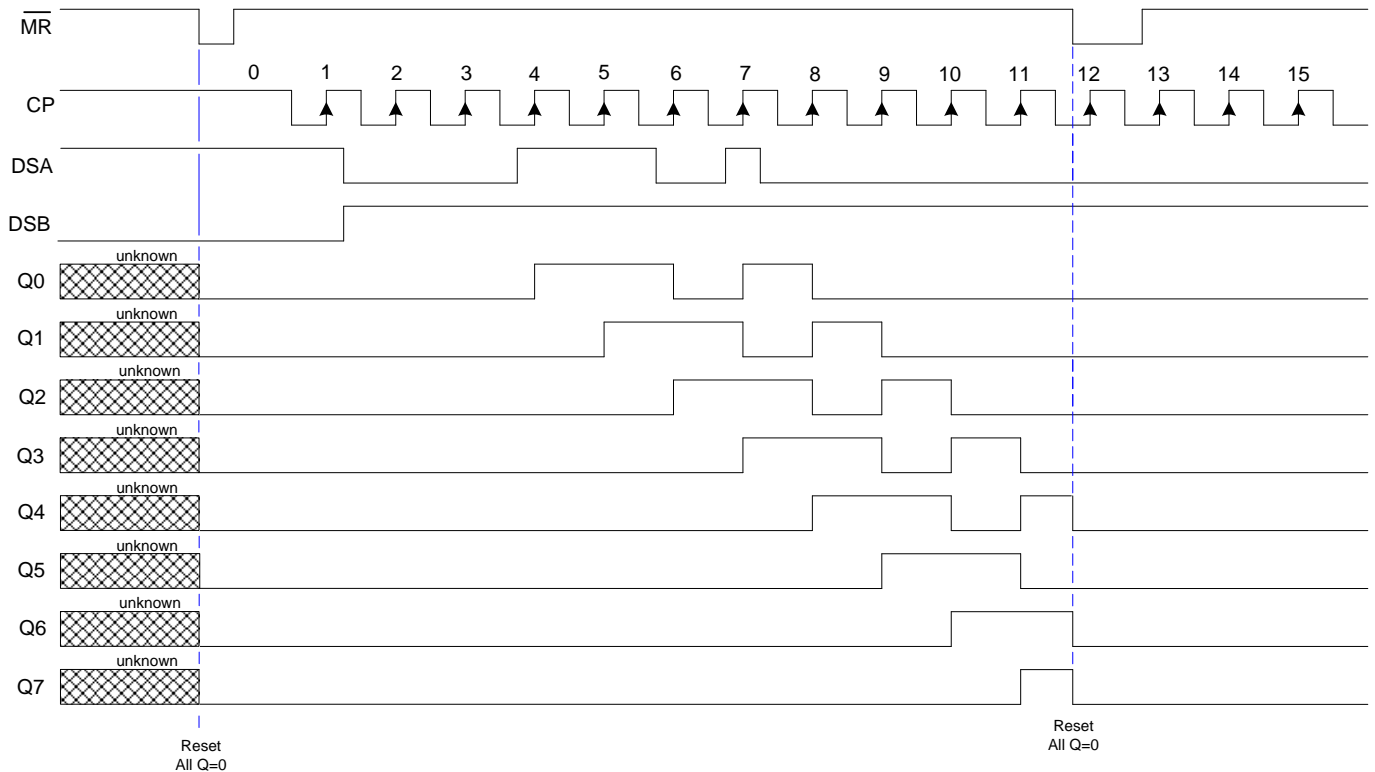| Pin Number	Pin Name	Function
1	DSA	Serial Data Input
2	DSB	Serial Data Input
3	Q0	Data Output
4	Q1	Data Output
5	Q2	Data Output
6	Q3	Data Output
7	GND	Ground
8	CP	Clock Pulse –Positive Edge Triggered
9	$\overline{MR}$	Master Reset - Asynchronous
10	Q4	Data Output
11	Q5	Data Output
12	Q6	Data Output
13	Q7	Data Output
14	V_{CC}	Supply Voltage

Function Table

Mode	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1-Q7
Reset	L	X	X	X	L	L
Shift	H	↑	L	X	L	Qn←Qn-1 (n= 1 to7)
	H	↑	X	L	L	Qn←Qn-1 (n= 1 to7)
	H	↑	H	H	H	Qn←Qn-1 (n= 1 to7)

Note: 4. Signals asserted on DSA and DSB must be in place longer than Tsu (set up time) before CP occurs and remain in place Thold (hold time) after CP.

74HCT164
Document number: DS36280 Rev. 1 - 2

2 of 10
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Logic Diagram
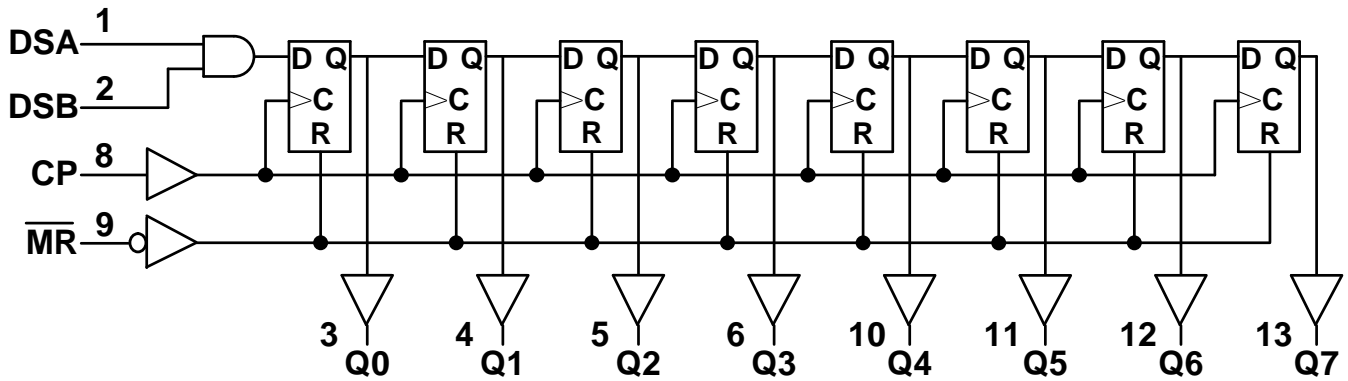
Timing Diagram

Notes:
5. All Q values are reset to LOW when $\overline{MR}$ goes low. $\overline{MR}$ is asynchronous and overrides all other signals.
6. Serial data supplied at DSA and DSB is ANDED and transferred to Q0 on positive edge of CP.

74HCT164
Document number: DS36280 Rev. 1 - 2

3 of 10
www.diodes.com

September 2014
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Absolute Maximum Ratings (Note 7) (T$_A$ = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V$_{CC}$	Supply Voltage Range	-0.5 to +7.0	V
V$_I$	Input Voltage Range (Note 8)	-0.5 to +7.0	V
I$_{IK}$	Input Clamp Current V$_I$ < -0.5V or Vi > V$_{CC}$ +0.5V	±20	mA
I$_{OK}$	Output Clamp Current V$_O$ < -0.5V or V$_O$ > V$_{CC}$ +0.5V	±20	mA
I$_O$	Continuous Output Current -0.5V < V$_O$ V$_{CC}$ +0.5V	+/- 25	mA
I$_{CC}$	Continuous Current Through Vcc	50	mA
I$_{GND}$	Continuous Current Through GND	-50	mA
T$_J$	Operating Junction Temperature	-40 to +150	°C
T$_{STG}$	Storage Temperature	-65 to +150	°C
P$_{TOT}$	Total Power Dissipation	500	mW

Notes: 7. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should
be within recommend values.
8. Input Voltage cannot exceed Vcc to the extent the Maximum clamp current is exceeded.

Recommended Operating Conditions (Note 9) (T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V$_{CC}$	Supply Voltage	-	4.5	5.5	V
V$_I$	Input Voltage	-	0	V$_{CC}$	V
V$_O$	Output Voltage	-	0	V$_{CC}$	V
Δt/ΔV	Input transition rise or fall rate	V$_{CC}$ = 4.5V	-	140	ns/V
T$_A$	Operating Free-Air Temperature	-	-40	+125	°C

Note: 9. Unused inputs should be held at V$_{CC}$ or Ground.

Electrical Characteristics (T$_A$ = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V$_{CC}$	T$_A$ = +25°C			T$_A$ = -40°C to +85°C		T$_A$ = -40°C to +125°C		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V$_{IH}$	High-Level Input Voltage	-	4.5V to 5.5V	2.0	1.6	-	2.0	-	2.0	-	V
V$_{IL}$	Low-level Input Voltage	-	4.5V to 5.5V	-	1.2	0.8	-	0.8	-	0.8	V
V$_{OH}$	High-level Output Voltage	I$_{OH}$ = -20μA	4.5V	4.4	4.5	-	4.4	-	4.4	-	V
		I$_{OH}$ = -4.0mA	4.5V	3.98	4.32	-	3.84	-	3.7	-	
V$_{OL}$	Low-level Output Voltage	I$_{OL}$ = 20μA	4.5V	-	0	0.1	-	0.1	-	0.1	V
		I$_{OL}$ = 4mA	4.5V	-	0.15	0.26	-	0.33	-	0.4	
I$_I$	Input Current	V$_I$ =GND or Vcc	6.0V	-	-	±0.1	-	± 1	-	± 1	μA
I$_{CC}$	Supply Current	V$_I$ = GND or V$_{CC}$, I$_O$ = 0	6.0V	-	-	8.0	-	80	-	160	μA
ΔI$_{CC}$	Additional Supply current	V$_I$=V$_{CC}$-2.1V I$_O$ = 0 Other inputs at V$_{CC}$ or GND.	4.5V to 5.5V	-	100	360	-	450	-	490	μA

74HCT164
Document number: DS36280 Rev. 1 - 2

4 of 10
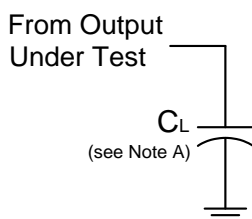**www.diodes.com**

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Switching Characteristics

| Symbol / Parameter	Pins	Test Conditions	Vcc	T_A=25°C			-40°C to 85°C		-40°C to 125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
f_{MAX} Maximum	CP	Figure 1	4.5V	27	55	-	22	-	18	-	MHz
			5.0V	-	61	-	-	-	-	-	
t_W Pulse Width	CP HIGH or LOW	Figure 1	4.5V	18	7	-	23	-	27	-	ns
	$\overline{MR}$ LOW	Figure 1	4.5V	18	10	-	23	-	27	-	ns
t_{SU} Set-up Time	DSA or DSB to CP	Figure 1	4.5V	12	6	-	15	-	18	-	ns
t_H Hold Time	DSA or DSB to CP	Figure 1	4.5V	4	-2	-	4	-	4	-	ns
t_{rec} Recovery Time	$\overline{MR}$ to CP	Figure 1	4.5V	16	7	-	20	-	24	-	ns-
t_{PD} Propagation	CP to Qn	Figure 1	4.5V	-	17	36	-	45	-	54	ns
			5.0V	-	14		-		-		
t_{PHL} HIGH to LOW Propagation	$\overline{MR}$ to Qn	Figure 1	4.5V	-	19	38	-	48	-	57	ns
			5.0V	-	16	-	-	-	-	-	
t_T Transition Time	All Signals	Figure 1	4.5V	-	7	15	-	19	-	22	ns

Operating Characteristics (T_A = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V_{CC} = 6V	Unit
			Typ	
C_{pd}	Power Dissipation Capacitance per Gate	f = 1 MHz V_I = Gnd to Vcc-1.5V	40	pF
C_I	Input Capacitance	V_I = Gnd or Vcc	3.5	pF

74HCT164
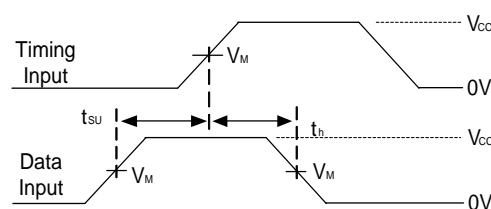Document number: DS36280 Rev. 1 - 2

5 of 10
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Parameter Measurement Information

From Output
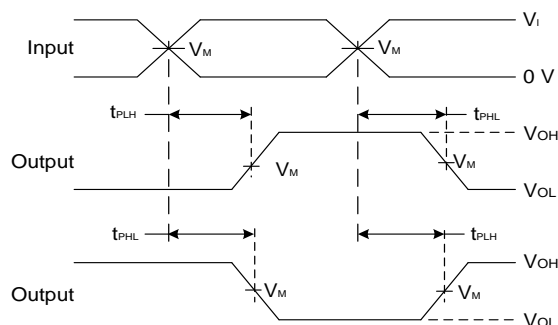Under Test

C_L
(see Note A)

V_{CC}	Inputs		V_M	C_L
	V_I	t_r/t_f		
4.5V	V_{CC}	6ns	1.3V	50pF
5.0V	V_{CC}	6ns	1.3V	15pF
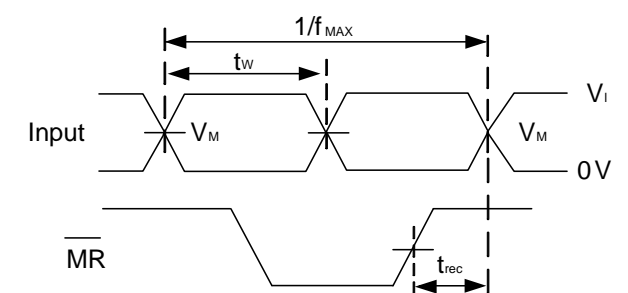
**Voltage Waveform
Pulse Duration and Recovery Time**
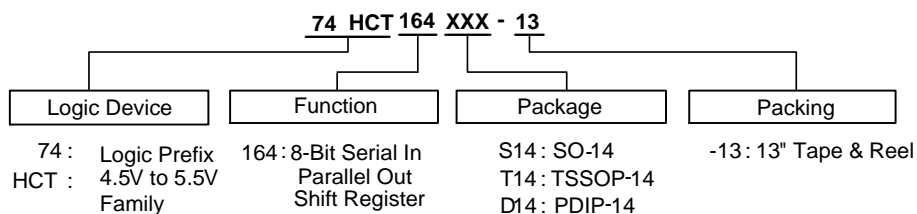
**Voltage Waveform
Set-up and Hold Times**

**Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs**

Notes: A . Includes test lead and test apparatus capacitance.
   B. All pulses are supplied at pulse repetition rate ≤10 MHz
   C. Inputs are measured separately one transition per measurement
   D. t_{PLH} and t_{PHL} are the same as t_{PD}
   E. Transition times t_t, t_{tlh}, t_{thl} are measured from the 10% to 90% or 90% to 10% of the appropriate waveform.

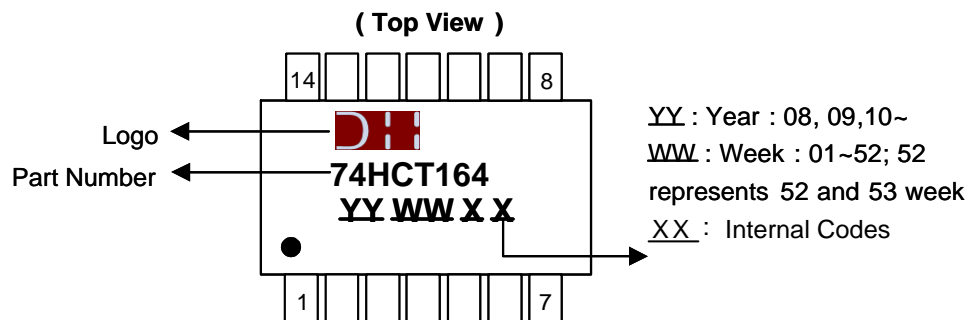**Figure 1 Load Circuit and Voltage Waveforms**

74HCT164
Document number: DS36280 Rev. 1 - 2

6 of 10
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Ordering Information

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74 HCT 164 XXX - 13
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Logic Device	Function	Package	Packing
74 : Logic Prefix HCT : 4.5V to 5.5V Family	164 : 8-Bit Serial In Parallel Out Shift Register	S14 : SO-14 T14 : TSSOP-14 D14 : PDIP-14	-13 : 13" Tape & Reel

Device	Package Code	Packaging	Packing	
			Quantity	Part Number Suffix
74HCT164S14-13	S14	SO-14	2500/Tape & Reel	-13
74HCT164T14-13	T14	TSSOP-14	2500/Tape & Reel	-13
74HCT164D14 **Future Product**	D14	PDIP-14	Tube	-

## Marking Information

(1) SO-14, TSSOP-14, PDIP-14

(Top View)

Logo

Part Number

74HCT164
YY WW X X

YY : Year : 08, 09,10~
WW : Week : 01~52; 52
represents 52 and 53 week
XX : Internal Codes

Part Number	Package
74HCT164S14-13	SO-14
74HCT164T14-13	TSSOP-14
74HCT164D14	PDIP-14

74HCT164
Document number: DS36280 Rev. 1 - 2

7 of 10
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Package Outline Dimensions (All dimensions in mm.)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

Package Type: SO-14
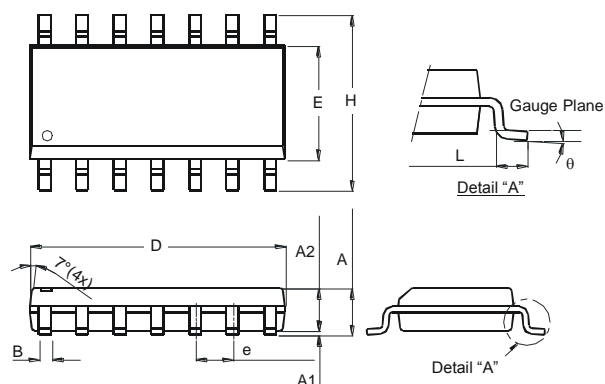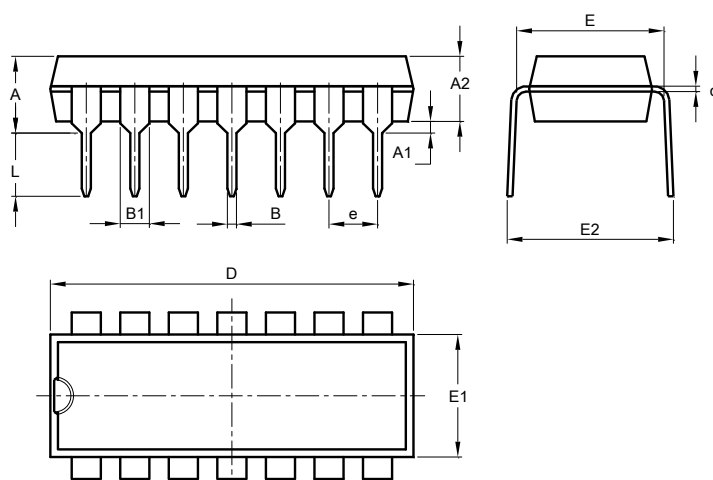
SO-14		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

Package Type: TSSOP-14
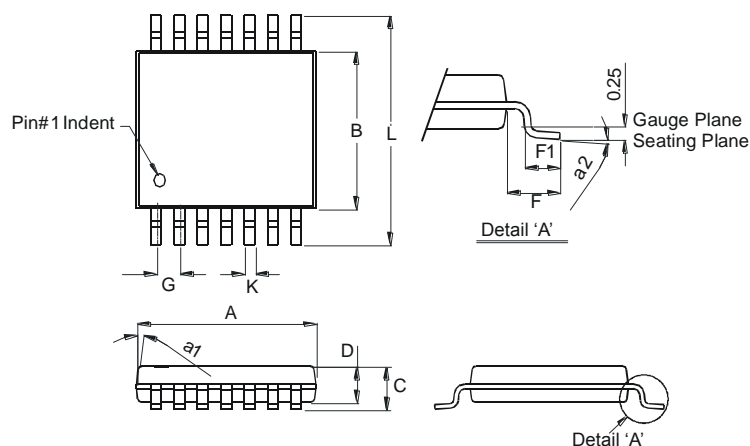
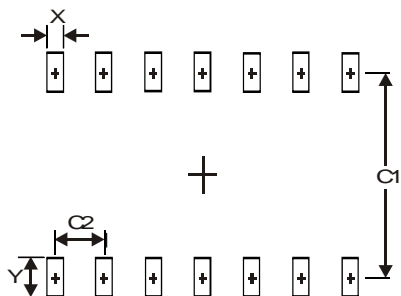| TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

Package Type: PDIP-14

PDIP-14		
Dim	Min	Max
A	3.710	4.310
A1	0.510	-
A2	3.200	3.600
B	0.380	0.570
B1	1.524 (BSC)	
c	0.204	0.360
D	18.800	19.200
E	6.200	6.600
E1	7.320	7.920
E2	8.400	9.000
e	2.540 (BSC)	
L	3.000	3.600
All Dimensions in mm		

74HCT164
Document number: DS36280 Rev. 1 - 2

September 2014
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Suggested Pad Layout
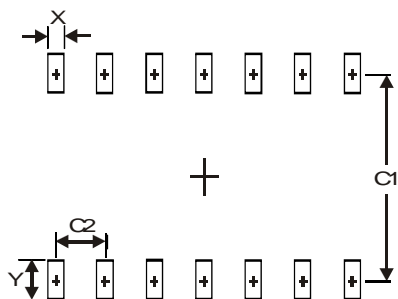
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for latest version.

Package Type: SO-14

Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14

Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

74HCT164
Document number: DS36280 Rev. 1 - 2

9 of 10
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September 2014
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74HCT164
Document number: DS36280 Rev. 1 - 2

10 of 10
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September 2014
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