MAX6954

4-Wire Interfaced, 2.7V to 5.5V LED Display Driver with I/O Expander and Key Scan

General Description

The MAX6954 is a compact display driver that interfaces microprocessors to a mix of 7-segment, 14-segment, and 16-segment LED displays through an SPI-/QSPI™-compatible 4-wire serial interface. The serial interface may be cascaded through multiple devices. The MAX6954 drives up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, or 128 discrete LEDs, while functioning from a supply voltage as low as 2.7V. The driver includes five I/O expander (or GPIO) lines, some or all of which may be configured as a key-switch reader, which automatically scans and debounces a matrix of up to 32 switches.

Included on chip are full 14- and 16-segment ASCII 104-character fonts, a hexadecimal font for 7-segment displays, multiplex scan circuitry, anode and cathode drivers, and static RAM that stores each digit. The maximum segment current for the display digits is set using a single external resistor. Digit intensity can be independently adjusted using the 16-step internal digital brightness control. The MAX6954 includes a low-power shutdown mode, a scan-limit register that allows the user to display from 1 to 16 digits, segment blinking (synchronized across multiple drivers, if desired), and a test mode, which forces all LEDs on. The LED drivers are slew-rate limited to reduce EMI.

For a 2-wire interfaced version, refer to the MAX6955 data sheet. An evaluation kit (EV kit) for the MAX6955 is available.

Applications

- Set-Top Boxes
- Panel Meters
- White Goods
- Bar Graph Displays
- Audio/Video Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6954AAX	-40°C to +125°C	36 SSOP
MAX6954APL	-40°C to +125°C	40 PDIP
MAX6954ATL+	-40°C to +125°C	40 TQFN-EP*

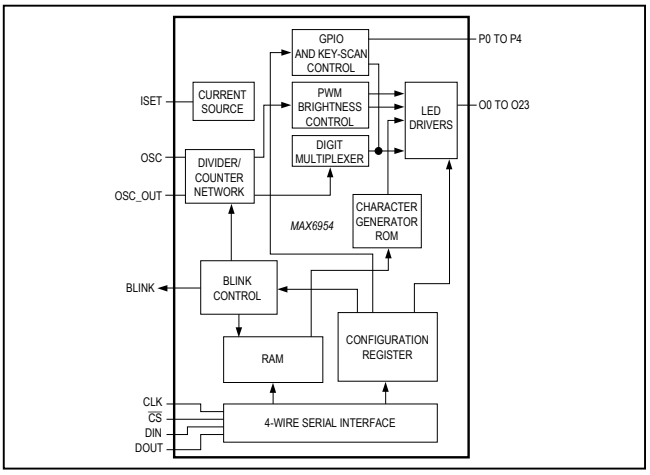
+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

- High-Speed 26MHz SPI/QSPI/MICROWIRE®-Compatible Serial Interface
- 2.7V to 5.5V Operation
- Drives Up to 16 Digits 7-Segment, 8 Digits 14-Segment, 8 Digits 16-Segment, 128 Discrete LEDs, or a Combination of Digit Types
- Drives Common-Cathode Monocolor and Bicolor LED Displays
- Built-In ASCII 104-Character Font for 14-Segment and 16-Segment Digits and Hexadecimal Font for 7-Segment Digits
- Automatic Blinking Control for each Segment
- 10µA (typ) Low-Power Shutdown (Data Retained)
- 16-Step Digit-by-Digit Digital Brightness Control
- Display Blanked on Power-Up
- Slew-Rate Limited Segment Drivers for Lower EMI
- Five GPIO Port Pins Can Be Configured as Key-Switch Reader to Scan and Debounce Up to 32 Switches with n-Key Rollover
- IRQ Output when a Key Input Is Debounced
- 36-Pin SSOP and 40-Pin DIP and TQFN Packages
- Automotive Temperature Range Standard

Functional Diagram



Pin Configurations and Typical Operating Circuits appear at end of data sheet.

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Absolute Maximum Ratings

(Voltage with respect to GND.)
- V+ .....-0.3V to +6V
- All Other Pins.....-0.3V to (V+ + 0.3V)

Current
- O0–O7 Sink Current.....935mA
- O0–O18 Source Current.....55mA
- DIN, CLK, $\overline{CS}$, OSC, DOUT, BLINK, OSC_OUT, ISET..20mA
- P0, P1, P2, P3, P4 .....40mA
- GND.....1A

Continuous Power Dissipation (T_A = +70°C)
- 36-Pin SSOP (derate at 11.8mW/°C above +70°C)....941mW
- 40-Pin PDIP (derate at 16.7mW/°C above +70°C) ...1333mW
- 40-Pin TQFN (derate at 37mW/°C above +70°C).....2963mW

Operating Temperature Range (T_{MIN} to T_{MAX})..... -40°C to +125°C

Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(Typical Operating Circuits, V+ = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.7		5.5	V
Shutdown Supply Current	I_{SHDN}	Shutdown mode, all digital inputs at V+ or GND	T_A = +25°C		10	35	µA
			T_A = T_{MIN} to T_{MAX}			40	
Operating Supply Current	I+	All segments on, all digits scanned, intensity set to full, internal oscillator, DOUT open circuit, no display or OSC_OUT load connected	T_A = +25°C		22	30	mA
			T_A = T_{MIN} to T_{MAX}			35	
Master Clock Frequency	f_{OSC}	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			4		MHz
		OSC driven externally		1		8	
Dead Clock Protection Frequency	f_{OSC}				95		kHz
OSC Internal/External Detection Threshold	V_{OSC}				1.7		V
OSC High Time	t_{CH}			50			ns
OSC Low Time	t_{CL}			50			ns
Slow Segment Blink Period	$f_{SLOWBLINK}$	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			1		s
Fast Segment Blink Period	$f_{FASTBLINK}$	OSC = RC oscillator, R_{SET} = 56kΩ, C_{SET} = 22pF, V+ = 3.3V			0.5		s
Fast or Slow Segment Blink Duty Cycle				49.5		50.5	%

DC Electrical Characteristics (continued)

(Typical Operating Circuits, V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Segment Drive Source Current	I_{SEG}	V_{LED} = 2.2V, V+ = 3.3V	T_A = +25°C	-34.5	-40	-46.5	mA
Segment Current Slew Rate	$\Delta I_{SEG}/\Delta t$	T_A = +25°C, V+ = 3.3V			11		mA/µs
Segment Drive Current Matching	ΔI_{SEG}	T_A = +25°C, V+ = 3.3V			5	10	%
LOGIC INPUTS AND OUTPUTS							
Input Leakage Current DIN, CLK, $\overline{CS}$, OSC, P0, P1, P2, P3, P4	I_{IH}, I_{IL}			-1		+1	µA
4-Wire Logic-High Input Voltage DIN, CLK, $\overline{CS}$	V_{IHSPI}			1.8			V
4-Wire Logic-Low Input Voltage DIN, CLK, $\overline{CS}$	V_{ILSPI}					0.6	V
Port Logic-High Input Voltage P0, P1, P2, P3, P4	V_{IHP}			0.7 x V+			V
Port Logic-Low Input Voltage P0, P1, P2, P3, P4	V_{ILP}					0.3 x V+	V
Port Hysteresis Voltage P0, P1, P2, P3, P4	ΔV_{IP}				0.03 x V+		V
Port Input Pullup Current from V+	I_{IPU}	P0 to P3 configured as keyscan input, V+ = 3.3V			75		µA
Port Output Low Voltage	V_{OLP}	I_{SINK} = 8mA			0.3	0.5	V
Blink Output Low Voltage	V_{OLBK}	I_{SINK} = 0.6mA			0.1	0.3	V
DOUT Output High Voltage	V_{OHDO}	I_{SOURCE} = 1.6mA		V+ - 0.2			V
DOUT Output Low Voltage	V_{OLDO}	I_{SINK} = 1.6mA				0.2	V
OSC_OUT Output High Voltage	V_{OHOSC}	I_{SOURCE} = 1.6mA		V+ - 0.4			V
OSC_OUT Output Low Voltage	V_{OLOSC}	I_{SINK} = 1.6mA				0.4	V

Timing Characteristics

(*Typical Operating Circuits*, V+ = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

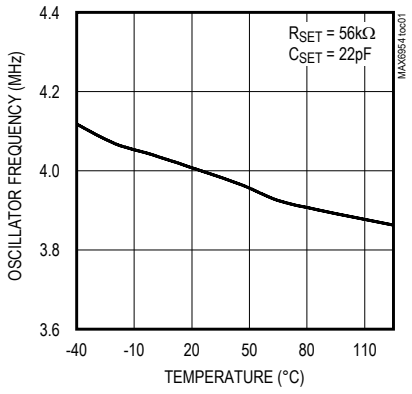
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Clock Period	t_{CP}		38.4			ns
CLK Pulse Width High	t_{CH}		16			ns
CLK Pulse Width Low	t_{CL}		16			ns
$\overline{CS}$ Fall to CLK Rise Setup Time	t_{CSS}		9.5			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		9.5			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	V+ = 3.0V to 5.5V			19	ns
		V+ = 2.7V			25	
DOUT Output Rise and Fall Times	t_{FT}	C_{LOAD} = 10pF, V+ = 3.0V to 5.5V			10	ns
Minimum $\overline{CS}$ Pulse High	t_{CSW}		19.5			ns

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

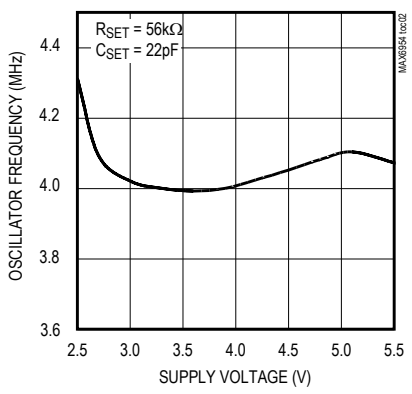
Typical Operating Characteristics

(V+ = 3.3V, LED forward voltage = 2.4V, typical application circuit, T_A = +25°C, unless otherwise noted.)

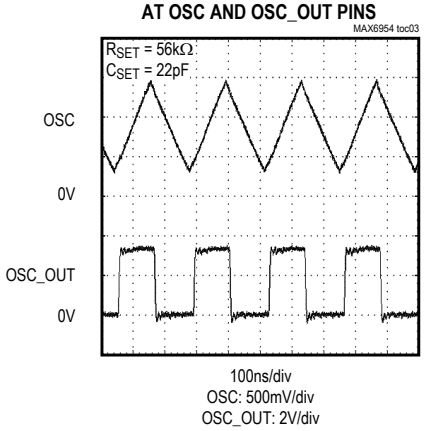
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



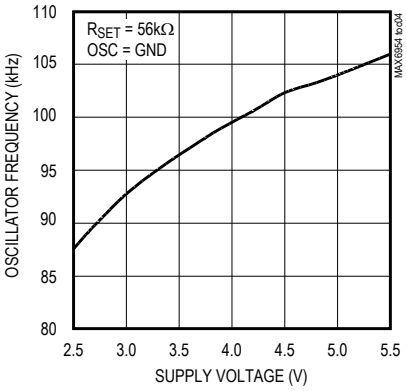
INTERNAL OSCILLATOR WAVEFORM AT OSC AND OSC_OUT PINS



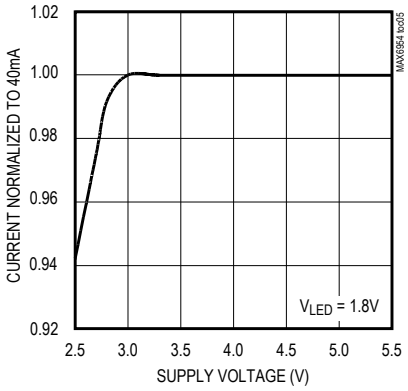
Typical Operating Characteristics (continued)

(V+ = 3.3V, LED forward voltage = 2.4V, typical application circuit, T_A = +25°C, unless otherwise noted.)

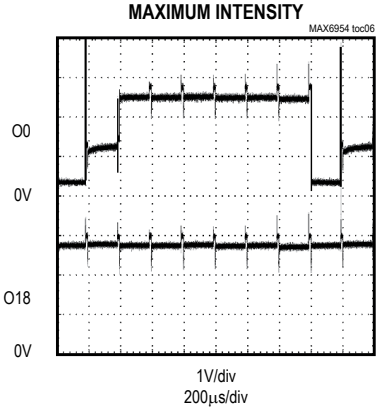
DEAD CLOCK OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



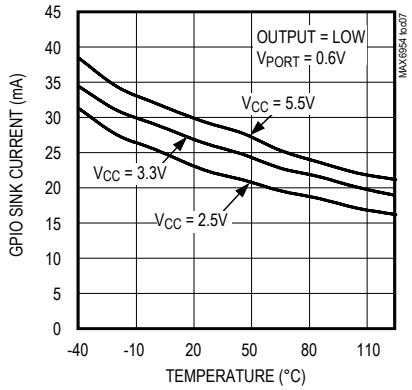
SEGMENT SOURCE CURRENT vs. SUPPLY VOLTAGE



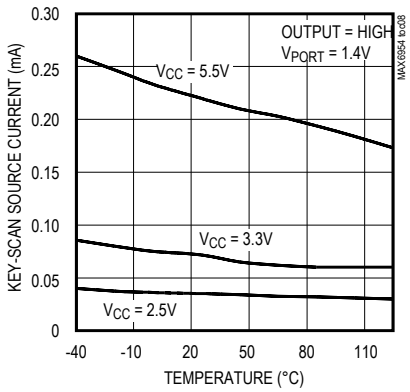
WAVEFORM AT PINS O0 AND O18, MAXIMUM INTENSITY



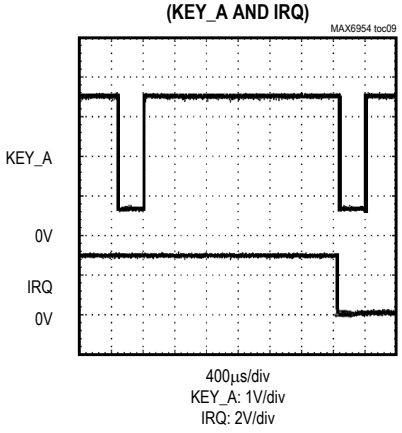
GPIO SINK CURRENT vs. TEMPERATURE



PORT INPUT PULLUP CURRENT vs. TEMPERATURE



KEYSCAN OPERATION (KEY_A AND IRQ)



Pin Description

PIN			NAME	FUNCTION
SSOP	PDIP	TQFN-EP		
1, 2, 34, 35, 36	1, 2, 38, 39, 40	36, 37, 33, 34, 35	P0–P4	General-Purpose I/O Ports (GPIOs). GPIO can be configured as logic inputs or open-drain outputs. Enabling key scanning configures some or all ports P0–P3 as key-switch matrix inputs with internal pullup and port P4 as $\overline{IRQ}$ output.
3	3	38	$\overline{CS}$	Chip-Select Input. Serial data is loaded into the shift register while $\overline{CS}$ is low. The most recent 16 bits of data latch on $\overline{CS}$'s rising edge.
4	4	39	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 15.5 clock cycles later. Use this pin to daisy-chain several devices or allow data readback. Output is push-pull.
5	5	40	CLK	Serial-Clock Input. On CLK's rising edge, data shifts into the internal shift register. On CLK's falling edge, data is clocked out of DOUT. CLK is active only while $\overline{CS}$ is low.
6	6	1	DIN	Serial-Data Input. Data from DIN loads into the internal 16-bit shift register on CLK's rising edge.
7–15, 22–31	7–15, 26–35	2–10, 21–30	O0–O18	Digit/Segment Drivers. When acting as digit drivers, outputs O0 to O7 sink current from the display common cathodes. When acting as segment drivers, O0 to O18 source current to the display anodes. O0 to O18 are high impedance when not being used as digit or segment drivers.
16, 18	17, 18, 20	12, 13, 15	GND	Ground
17	19	14	ISET	Segment Current Setting. Connect ISET to GND through series resistor R_{SET} to set the peak current.
19, 21	21, 23, 24	16, 18, 19	V+	Positive Supply Voltage. Bypass V+ to GND with a 47µF bulk capacitor and a 0.1µF ceramic capacitor.
20	22	17	OSC	Multiplex Clock Input. To use internal oscillator, connect capacitor C_{SET} from OSC to GND. To use external clock, drive OSC with a 1MHz to 8MHz CMOS clock.
32	36	31	BLINK	Blink Clock Output. Output is open drain.
33	37	32	OSC_OUT	Clock Output. OSC_OUT is a buffered clock output to allow easy blink synchronization of multiple MAX6954s. Output is push-pull.
—	16, 25	11, 20	N.C.	Not Connected Internally
—	—	—	EP	Exposed Pad (TQFN package only). Internally connected to GND. Connect to a large ground plane to maximize thermal performance.

Detailed Description

The MAX6954 is a serially interfaced display driver that can drive up to 16 digits 7-segment, 8 digits 14-segment, 8 digits 16-segment, 128 discrete LEDs, or a combination of these display types. Table 1 shows the drive capability of the MAX6954 for monocolor and bicolor displays.

The MAX6954 includes 104-character ASCII font maps for 14-segment and 16-segment displays, as well as the hexadecimal font map for 7-segment displays. The characters follow the standard ASCII font, with the addition of the following common symbols: £, €, ¥, °, µ, ±, ↑, and ↓. Seven bits represent the 104-character font map; an 8th bit is used to select whether the decimal point (DP) is lit. Seven-segment LED digits may be controlled directly or use the hexadecimal font. Direct segment control allows the MAX6954 to be used to drive bar graphs and discrete LED indicators.

Tables 2, 3, and 4 list the connection schemes for 16-, 14-, and 7-segment digits, respectively. The letters in Tables 2, 3, and 4 correspond to the segment labels shown in Figure 1. (For applications that require mixed display types, see Tables 37–40.)

Serial Interface

The MAX6954 communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs: clock (CLK), chip select ($\overline{CS}$), and data in (DIN), and one output, data out (DOUT). $\overline{CS}$ must be low to

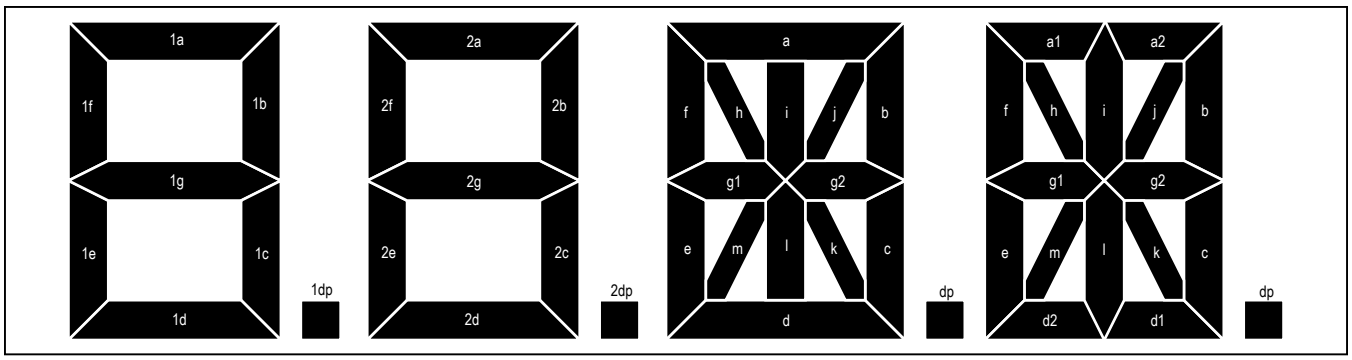


Figure 1. Segment Labeling for 7-Segment Display, 14-Segment Display, and 16-Segment Display

Table 1. MAX6954 Drive Capability

DISPLAY TYPE	7 SEGMENT (16-CHARACTER HEXADECIMAL FONT)	14 SEGMENT/ 16 SEGMENT (104-CHARACTER ASCII FONT MAP)	DISCRETE LEDs (DIRECT CONTROL)
Monocolor	16	8	128
Bicolor	8	4	64

clock data into or out of the device, and DIN must be stable when sampled on the rising edge of CLK. DOUT is stable on the rising edge of CLK. Note that while the SPI protocol expects DOUT to be high impedance when the MAX6954 is not being accessed, DOUT on the MAX6954 is never high impedance.

CLK and DIN may be used to transmit data to other peripherals. The MAX6954 ignores all activity on CLK and DIN except when CS is low.

Control and Operation Using the 4-Wire Interface

Controlling the MAX6954 requires sending a 16-bit word. The first byte, D15 through D8, is the command, and the second byte, D7 through D0, is the data byte (Table 5).

Connecting Multiple MAX6954s to the 4-Wire Bus

Multiple MAX6954s may be daisy-chained by connecting the DOUT of one device to the DIN of the next, and driving CLK and $\overline{CS}$ lines in parallel (Figure 2). Data at DIN propagates through the internal shift registers and appears at DOUT 15.5 clock cycles later, clocked out on the falling edge of CLK. When sending commands to daisy-chained MAX6954s, all devices are accessed at the same time. An access requires (16 x n) clock cycles, where n is the number of MAX6954s connected together. To update just one device in a daisy-chain, the user can send the no-op command (0x00) to the others. Figure 3 is the MAX6954 timing diagram.

The MAX6954 is written to using the following sequence:

1) Take CLK low.
2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.
3) Clock 16 bits of data into DIN, D15 first to D0 last, observing the setup and hold times. Bit D15 is low, indicating a write command.
4) Take $\overline{CS}$ high (while CLK is still high after clocking in the last data bit).
5) Take CLK low.
6) Figure 4 shows a write operation when 16 bits are transmitted.

If fewer or greater than 16 bits are clocked into the MAX6954 between taking $\overline{CS}$ low and taking $\overline{CS}$ high again, the MAX6954 stores the last 16 bits received, including the previous transmission(s). The general case is when n bits (where n > 16) are transmitted to the MAX6954. The last bits are comprising bits {n-15} to {n}, are retained, and are parallel loaded into the 16-bit latch as bits D15 to D0, respectively (Figure 5).

Table 2. Connection Scheme for Eight 16-Segment Digits

DIGIT	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0	CCO	—	a1	a2	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
1	—	CC1	a1	a2	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
2	a1	a2	CC2	—	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
3	a1	a2	—	CC3	b	c	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
4	a1	a2	b	c	CC4	—	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
5	a1	a2	b	c	—	CC5	d1	d2	e	f	g1	g2	h	i	j	k	l	m	dp
6	a1	a2	b	c	d1	d2	CC6	—	e	f	g1	g2	h	i	j	k	l	m	dp
7	a1	a2	b	c	d1	d2	—	CC7	e	f	g1	g2	h	i	j	k	l	m	dp

Table 3. Connection Scheme for Eight 14-Segment Digits

DIGIT	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0	CCO	—	a	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
1	—	CC1	a	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
2	a	—	CC2	—	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
3	a	—	—	CC3	b	c	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
4	a	—	b	c	CC4	—	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
5	a	—	b	c	—	CC5	d	—	e	f	g1	g2	h	i	j	k	l	m	dp
6	a	—	b	c	d	—	CC6	—	e	f	g1	g2	h	i	j	k	l	m	dp
7	a	—	b	c	d	—	—	CC7	e	f	g1	g2	h	i	j	k	l	m	dp

Table 4. Connection Scheme for Sixteen 7-Segment Digits

DIGIT*	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18
0, 0a	CC0	—	1a	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
1, 1a	—	CC1	1a	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
2, 2a	1a	—	CC2	—	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
3, 3a	1a	—	—	CC3	1b	1c	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
4, 4a	1a	—	1b	1c	CC4	—	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
5, 5a	1a	—	1b	1c	—	CC5	1d	1dp	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
6, 6a	1a	—	1b	1c	1d	1dp	CC6	—	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp
7, 7a	1a	—	1b	1c	1d	1dp	—	CC7	1e	1f	1g	2a	2b	2c	2d	2e	2f	2g	2dp

Each cathode driver output (CC0-CC7) connects to **two digit common cathode pins.*

Table 5. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	ADDRESS							MSB			DATA				LSB

Reading Device Registers

Any register data within the MAX6954 may be read by sending a logic-high to bit D15. The sequence is:

1) Take CLK low.
2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.
3) Clock 16 bits of data into DIN, D15 first to D0 last. D15 is high, indicating a read command and bits D14 through D8 contain the address of the register

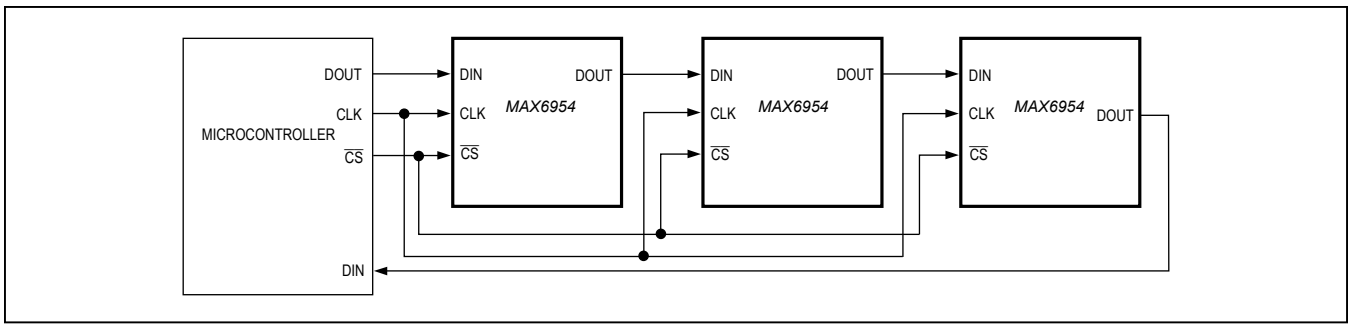


Figure 2. MAX6954 Daisy-Chain Connection

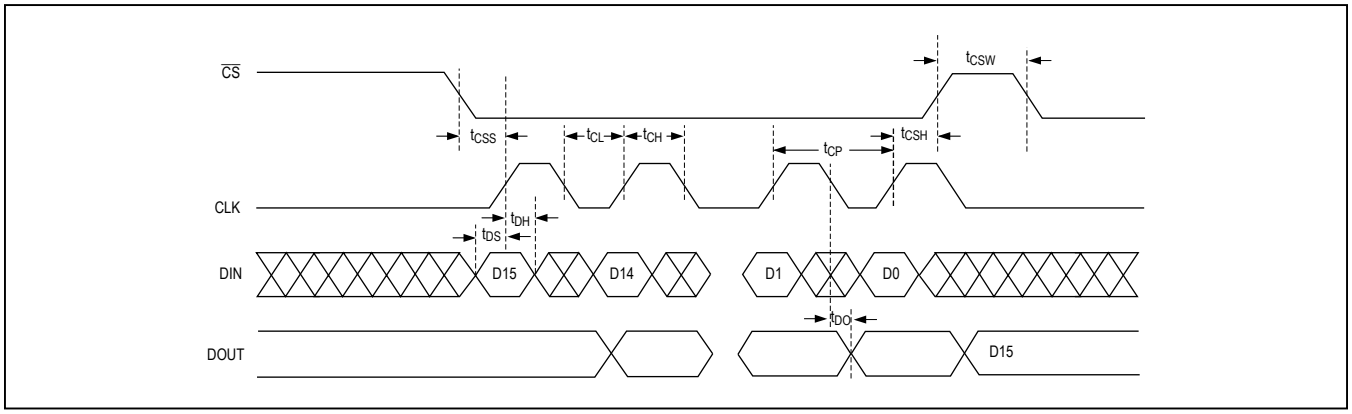


Figure 3. Timing Diagram

to read. Bits D7 to D0 contain dummy data, which is discarded.

4) Take $\overline{CS}$ high (while CLK is still high after clocking in the last data bit), positions D7 through D0 in the shift register are now loaded with the register data addressed by bits D15 through D8.
5) Take CLK low.
6) Issue another read or write command (which can be a no-op), and examine the bit stream at DOUT; the second 8 bits are the contents of the register addressed by bits D14 through D8 in step 3.

Digit Type Registers

The MAX6954 uses 32 digit registers to store the characters that the user wishes to display. These digit registers are implemented with two planes, P0 and P1. Each digit is represented by 2 bytes of memory, 1 byte in plane P0 and the other in plane P1. The digit registers are mapped so that a digit's data can be updated in plane P0, plane P1, or both planes at the same time (Table 6).

If the blink function is disabled through the Blink Enable Bit E (Table 19) in the configuration register, then the digit register data in plane P0 is used to multiplex the display. The digit register data in P1 is not used. If the blink function is enabled, then the digit register data in both plane P0 and plane P1 are alternately used to multiplex the display. Blinking is achieved by multiplexing the LED display using data plane P0 and plane P1 on alternate phases of the blink clock (Table 20).

The data in the digit registers does not control the digit segments directly for 14- and 16-segment displays. Instead, the register data is used to address a character generator that stores the data for the 14- and 16-segment fonts (Tables 7 and 8). The lower 7 bits of the digit data (D6 to D0) select the character from the font.

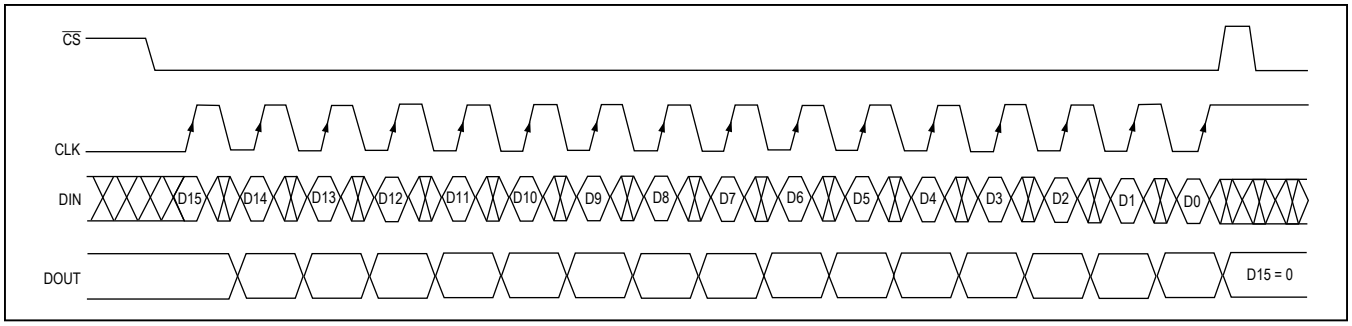


Figure 4. Transmission of 16 Bits to the MAX6954

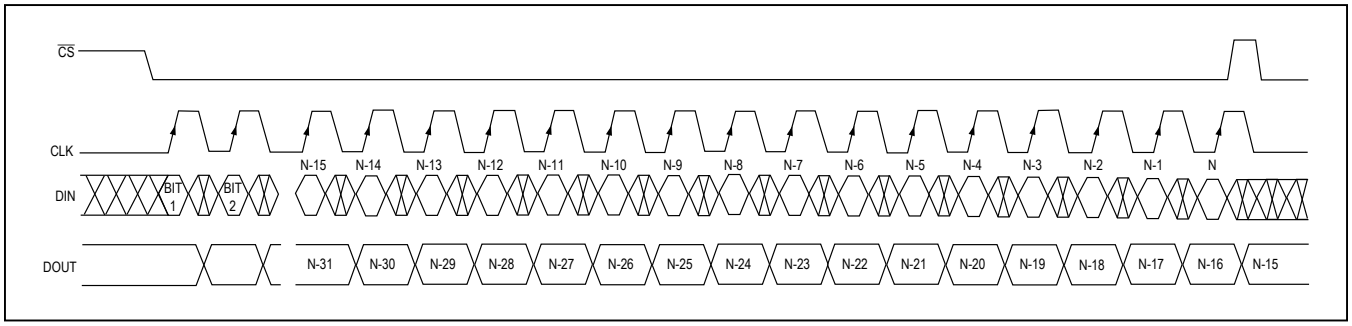


Figure 5. Transmission of More than 16 Bits to the MAX6954

The most significant bit of the register data (D7) controls the DP segment of the digits; it is set to 1 to light DP, and to zero to leave DP unlit (Table 9).

For 7-segment displays, the digit plane data register can be used to address a character generator, which contains the data of a 16-character font containing the hexadecimal font. The decode mode register can be used to disable the character generator and allow the segments to be controlled directly. Table 10 shows the one-to-one pairing of each data bit to the appropriate segment line in the digit plane data registers. The hexadecimal font is decoded according to Table 11.

The digit-type register configures the display driver for various combinations of 14-segment digits, 16-segment digits, and/or pairs, or 7-segment digits. The function of this register is to select the appropriate font for each digit and route the output of the font to the appropriate MAX6954 driver output pins. The MAX6954 has four digit drive slots. A slot can be filled with various combinations of monocolor and bicolor 16-segment displays, 14-segment displays, or two 7-segment displays. Each pair of bits in the register corresponds to one of the four digit drive slots, as shown in Table 12. Each bit also corresponds to one of the eight common-cathode digit drive outputs, CC0 to CC7. When using bicolor digits, the anode connections for the two digits within a slot are always the same. This means that a slot correctly drives two monocolor or one bicolor 14- or 16-segment digit. The digit type register can be written, but cannot be read. Examples of configuration settings required for some display digit combinations are shown in Table 13.

7-Segment Decode-Mode Register

In 7-segment mode, the hexadecimal font can be disabled (Table 14). The decode-mode register selects between hexadecimal code or direct control for each of eight possible pairs of 7-segment digits. Each bit in the register corresponds to one pair of digits. The digit pairs are {digit 0, digit 0a} through {digit 7, digit 7a}. Disabling decode mode allows direct control of the 16 LEDs of a dual 7-segment display. Direct control mode can also be used to drive a matrix of 128 discrete LEDs.

A logic-high selects hexadecimal decoding, while a logic-low bypasses the decoder. When direct control is selected, the data bits D7 to D0 correspond to the segment lines of the MAX6954. Write x0010000 to blank all segments in hexadecimal decode mode.

Display Blink Mode

The display blinking facility, when enabled, makes the driver flip automatically between displaying the digit register data in planes P0 and P1. If the digit register data for any digit is different in the two planes, then that digit appears to flip between two characters. To make a character appear to blink on or off, write the character to one plane, and use the blank character (0x20) for the other plane. Once blinking has been configured, it continues automatically without further intervention.

Blink Speed

The blink speed is determined by the frequency of the multiplex clock, OSC, and by the setting of the Blink Rate Selection Bit B (Table 18) in the configuration register. The Blink Rate Selection Bit B sets either fast or slow blink speed for the whole display.

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, intensities are set to minimum, and shutdown is enabled (Table 15).

Configuration Register

The configuration register is used to enter and exit shutdown, select the blink rate, globally enable and disable the blink function, globally clear the digit data, select between global or digit-by-digit control of intensity, and reset the blink timing (Tables 16–19 and 21–24).

The configuration register contains 7 bits:

- S bit selects shutdown or normal operation (read/write).
- B bit selects the blink rate (read/write).
- E bit globally enables or disables the blink function (read/write).
- T bit resets the blink timing (data is not stored—transient bit).
- R bit globally clears the digit data for both planes P0 and P1 for ALL digits (data is not stored—transient bit).
- I bit selects between global or digit-by-digit control of intensity (read/write).
- P bit returns the current phase of the blink timing (read only—a write to this bit is ignored).

Character Generator Font Mapping

The font is composed of 104 characters in ROM. The lower 7 bits of the 8-bit digit register represent the character selection. The most significant bit, shown as x in the ROM map of Tables 7 and 8, is 1 to light the DP segment and zero to leave the DP segment unlit.

The character map follows the standard ASCII font for 96 characters in the x0101000 through x1111111 range. The first 16 characters of the 16-segment ROM map cover 7-segment displays. These 16 characters are numeric 0 to 9 and characters A to F (i.e., the hexadecimal set).

Multiplex Clock and Blink Timing

The OSC pin can be fitted with capacitor C_{SET} to GND to use the internal RC multiplex oscillator, or driven by an external clock to set the multiplex clock frequency and blink rate. The multiplex clock frequency determines the frequency that the complete display is updated. With OSC at 4MHz, each display digit is enabled for 200µs.

The internal RC oscillator uses an external resistor, R_{SET}, and an external capacitor, C_{SET}, to set the oscillator frequency. The suggested values of R_{SET} (56kΩ) and C_{SET} (22pF) set the oscillator at 4MHz, which makes the blink frequency 0.5Hz or 1Hz.

The external clock is not required to have a 50:50 duty cycle, but the minimum time between transitions must be 50ns or greater and the maximum time between transitions must be 750ns.

The on-chip oscillator may be accurate enough for applications using a single device. If an exact blink rate is required, use an external clock ranging between 1MHz and 8MHz to drive OSC. The OSC inputs of multiple MAX6954s can be tied together to a common external clock to make the devices blink at the same rate. The relative blink phasing of multiple MAX6954s can be synchronized by setting the T bit in the control register for all the devices in quick succession. If the serial interfaces of multiple MAX6954s are daisy-chained by connecting the DOUT of one device to the DIN of the next, then synchronization is achieved automatically by updating the configuration register for all devices simultaneously. Figure 6 is the multiplex timing diagram.

OSC_OUT Output

The OSC_OUT output is a buffered copy of either the internal oscillator clock or the clock driven into the OSC pin if the external clock has been selected. The feature is useful if the internal oscillator is used, and the user wishes to synchronize other MAX6954s to the same blink frequency. The oscillator is disabled while the MAX6954 is in shutdown.

Scan-Limit Register

The scan-limit register sets how many 14-segment digits or 16-segment digits or pairs of 7-segment digits are displayed, from 1 to 8. A bicolor digit is connected as two monocolor digits. The scan register also limits the number of keys that can be scanned.

Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading-zero suppression). Table 25 shows the scan-limit register format.

Intensity Registers

Digital control of display brightness is provided and can be managed in one of two ways: globally or individually. Global control adjusts all digits together. Individual control adjusts the digits separately.

The default method is global brightness control, which is selected by clearing the global intensity bit (I data bit D6) in the configuration register. This brightness setting applies to all display digits. The pulse-width modulator is then set by the lower nibble of the global intensity register, address 0x02. The modulator scales the average segment current in 16 steps from a maximum of 15/16 down to 1/16 of the peak current. The minimum interdigit blanking time is set to 1/16 of a cycle. When using bicolor digits, 256 color/brightness combinations are available.

Individual brightness control is selected by setting the global intensity bit (I data bit D6) in the configuration register. The pulse-width modulator is now no longer set by the lower nibble of the global intensity register, address 0x02, and the data is ignored. Individual digital control of display brightness is now provided by a separate pulse-width modulator setting for each digit. Each digit is controlled by a nibble of one of the four intensity registers: intensity10, intensity32, intensity54, and intensity76 for all display types, plus intensity10a, intensity32a, intensity54a, and intensity76a for the extra eight digits possible when 7-segment displays are used. The data from the relevant register is used for each digit as it is multiplexed. The modulator scales the average segment current in 16 steps in exactly the same way as global intensity adjustment.

Table 26 shows the global intensity register format, Table 27 shows individual segment intensity registers, Table 28 is the even individual segment intensity format, and Table 29 is the odd individual segment intensity format.

GPIO and Key Scanning

The MAX6954 feature five general-purpose input/output (GPIO) ports: P0 to P4. These ports can be individually enabled as logic inputs or open-drain logic outputs. The GPIO ports are not debounced when configured as inputs. The ports can be read and the outputs set using the 4-wire interface.

Some or all of the five ports can be configured to perform key scanning of up to 32 keys. Ports P0 to P4 are renamed Key_A, Key_B, Key_C, Key_D, and IRQ, respectively, when used for key scanning. The full key-scanning configuration is shown in Figure 7. Table 30 is the GPIO data register.

One diode is required per key switch. These diodes can be common-anode dual diodes in SOT23 packages, such as the BAW56. Sixteen diodes would be required for the maximum 32-key configuration.

The MAX6954 can only scan the maximum 32 keys if the scan-limit register is set to scan the maximum eight digits. If the MAX6954 is driving fewer digits, then a maximum of (4 x n) switches can be scanned, where n is the number of digits set in the scan-limit register. For example, if the MAX6954 is driving four 14-segment digits cathode drivers O0 to O3 are used. Only 16 keys can be scanned in this configuration; the switches shown connected to O4 through O7 are not read.

If the user wishes to scan fewer than 32 keys, then fewer scan lines can be configured for key scanning. The unused Key_x ports are released back to their original GPIO functionality. If key scanning is enabled, regardless of the number of keys being scanned, P4 is always configured as IRQ (Table 31).

The key-scanning circuit utilizes the LEDs' common-cathode driver outputs as the key-scan drivers. O0 to 07 go low for nominally 200µs (with OSC = 4MHz) in turn as the displays are multiplexed. By varying the oscillator frequency, the debounce time changes, though key scanning still functions. Key_x inputs have internal pullup resistors that allow the key condition to be tested. The Key_x input is low during the appropriate digit multiplex period when the key is pressed. The timing diagram of Figure 8 shows the normal situation where all eight LED cathode drivers are used.

Table 6. Register Address Map

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	R/$\overline{W}$	0	0	0	0	0	0	0	0x00
Decode Mode	R/$\overline{W}$	0	0	0	0	0	0	1	0x01
Global Intensity	R/$\overline{W}$	0	0	0	0	0	1	0	0x02
Scan Limit	R/$\overline{W}$	0	0	0	0	0	1	1	0x03
Configuration	R/$\overline{W}$	0	0	0	0	1	0	0	0x04
GPIO Data	R/$\overline{W}$	0	0	0	0	1	0	1	0x05
Port Configuration	R/$\overline{W}$	0	0	0	0	1	1	0	0x06
Display Test	R/$\overline{W}$	0	0	0	0	1	1	1	0x07
Write KEY_A Mask Read KEY_A Debounce	R/$\overline{W}$	0	0	0	1	0	0	0	0x08
Write KEY_B Mask Read KEY_B Debounce	R/$\overline{W}$	0	0	0	1	0	0	1	0x09
Write KEY_C Mask Read KEY_C Debounce	R/$\overline{W}$	0	0	0	1	0	1	0	0x0A
Write KEY_D Mask Read KEY_D Debounce	R/$\overline{W}$	0	0	0	1	0	1	1	0x0B
Write Digit Type Read KEY_A Pressed	R/$\overline{W}$	0	0	0	1	1	0	0	0x0C
Read KEY_B Pressed*	1	0	0	0	1	1	0	1	0x0D
Read KEY_C Pressed*	1	0	0	0	1	1	1	0	0x0E
Read KEY_D Pressed*	1	0	0	0	1	1	1	1	0x0F
Intensity 10	R/$\overline{W}$	0	0	1	0	0	0	0	0x10
Intensity 32	R/$\overline{W}$	0	0	1	0	0	0	1	0x11
Intensity 54	R/$\overline{W}$	0	0	1	0	0	1	0	0x12
Intensity 76	R/$\overline{W}$	0	0	1	0	0	1	1	0x13
Intensity 10a (7 Segment Only)	R/$\overline{W}$	0	0	1	0	1	0	0	0x14
Intensity 32a (7 Segment Only)	R/$\overline{W}$	0	0	1	0	1	0	1	0x15
Intensity 54a (7 Segment Only)	R/$\overline{W}$	0	0	1	0	1	1	0	0x16
Intensity 76a (7 Segment Only)	R/$\overline{W}$	0	0	1	0	1	1	1	0x17
Digit 0 Plane P0	R/$\overline{W}$	0	1	0	0	0	0	0	0x20
Digit 1 Plane P0	R/$\overline{W}$	0	1	0	0	0	0	1	0x21
Digit 2 Plane P0	R/$\overline{W}$	0	1	0	0	0	1	0	0x22
Digit 3 Plane P0	R/$\overline{W}$	0	1	0	0	0	1	1	0x23
Digit 4 Plane P0	R/$\overline{W}$	0	1	0	0	1	0	0	0x24
Digit 5 Plane P0	R/$\overline{W}$	0	1	0	0	1	0	1	0x25
Digit 6 Plane P0	R/$\overline{W}$	0	1	0	0	1	1	0	0x26
Digit 7 Plane P0	R/$\overline{W}$	0	1	0	0	1	1	1	0x27
Digit 0a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	0	0	0	0x28
Digit 1a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	0	0	1	0x29
Digit 2a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	0	1	0	0x2A
Digit 3a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	0	1	1	0x2B

**Do NOT write to register.*

Table 6. Register Address Map (continued)

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Digit 4a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	1	0	0	0x2C
Digit 5a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	1	0	1	0x2D
Digit 6a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	1	1	0	0x2E
Digit 7a Plane P0 (7 Segment Only)	R/$\overline{W}$	0	1	0	1	1	1	1	0x2F
Digit 0 Plane P1	R/$\overline{W}$	1	0	0	0	0	0	0	0x40
Digit 1 Plane P1	R/$\overline{W}$	1	0	0	0	0	0	1	0x41
Digit 2 Plane P1	R/$\overline{W}$	1	0	0	0	0	1	0	0x42
Digit 3 Plane P1	R/$\overline{W}$	1	0	0	0	0	1	1	0x43
Digit 4 Plane P1	R/$\overline{W}$	1	0	0	0	1	0	0	0x44
Digit 5 Plane P1	R/$\overline{W}$	1	0	0	0	1	0	1	0x45
Digit 6 Plane P1	R/$\overline{W}$	1	0	0	0	1	1	0	0x46
Digit 7 Plane P1	R/$\overline{W}$	1	0	0	0	1	1	1	0x47
Digit 0a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	0	0	0	0x48
Digit 1a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	0	0	1	0x49
Digit 2a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	0	1	0	0x4A
Digit 3a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	0	1	1	0x4B
Digit 4a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	1	0	0	0x4C
Digit 5a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	1	0	1	0x4D
Digit 6a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	1	1	0	0x4E
Digit 7a Plane P1 (7 Segment Only)	R/$\overline{W}$	1	0	0	1	1	1	1	0x4F
Write Digit 0 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	0	0	0	0x60
Write Digit 1 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	0	0	1	0x61
Write Digit 2 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	0	1	0	0x62
Write Digit 3 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	0	1	1	0x63
Write Digit 4 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	1	0	0	0x64
Write Digit 5 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	1	0	1	0x65
Write Digit 6 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	1	1	0	0x66
Write Digit 7 Planes P0 and P1 with Same Data, Reads as 0x00	R/$\overline{W}$	1	1	0	0	1	1	1	0x67
Write Digit 0a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	0	0	0	0x68
Write Digit 1a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	0	0	1	0x69

Table 6. Register Address Map (continued)

REGISTER	ADDRESS (COMMAND BYTE)								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Write Digit 2a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	0	1	0	0x6A
Write Digit 3a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	0	1	1	0x6B
Write Digit 4a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	1	0	0	0x6C
Write Digit 5a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	1	0	1	0x6D
Write Digit 6a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	1	1	0	0x6E
Write Digit 7a Planes P0 and P1 with Same Data (7 Segment Only), Reads as 0x00	R/$\overline{W}$	1	1	0	1	1	1	1	0x6F

Note: *Unused register bits read as zero.*

The timing in Figure 8 loops over time, with 32 keys experiencing a full key-scanning debounce over typically 25.6ms. Four keys are sampled every 1.6ms, or every multiplex cycle. If at least one key that was not previously pressed is found to have been pressed during both sampling periods, then that key press is debounced, and an interrupt is issued. The key-scan circuit detects any combination of keys being pressed during each debounce cycle (n-key rollover).

Port Configuration Register

The port configuration register selects how the five port pins are used. The port configuration register format is described in Table 32.

Key Mask Registers

The Key_A Mask, Key_B Mask, Key_C Mask, and Key_D Mask write-only registers (Table 33) configure the key-scanning circuit to cause an interrupt only when selected (masked) keys have been debounced. Each bit in the register corresponds to one key switch. The bit is clear to disable interrupt for the switch, and set to enable interrupt. Keys are always scanned (if enabled through the port configuration register), regardless of the setting of these interrupt bits, and the key status is stored in the appropriate Key_x pressed register.

Key Debounced Registers

The Key_A debounced, Key_B debounced, Key_C debounced, and Key_D debounced read-only registers (Table 34) show which keys have been detected as debounced by the key-scanning circuit.

Each bit in the register corresponds to one key switch. The bit is set if the switch has been correctly debounced since the register was read last. Reading a debounced register clears that register (after the data has been read) so that future keys pressed can be identified. If the debounced registers are not read, the key-scan data accumulates. However, as there is no FIFO in the MAX6954, the user is not able to determine key order, or whether a key has been pressed more than once, unless the debounced key status registers are read after each interrupt, and before the next key-scan cycle.

Reading any of the four debounced registers clears the IRQ output. If a key is pressed and held down, the key is reported as debounced (and IRQ issued) only once. The key must be detected as released by the key-scanning circuit, before it debounces again. If the debounced registers are being read in response to the IRQ being asserted, then the user should generally read all four registers to ensure that all the keys that were detected by the key-scanning circuit are discovered.

Key Pressed Registers

The Key_A pressed, Key_B pressed, Key_C pressed and Key_D pressed read-only registers (Table 35)show which keys have been detected as pressed by the key-scanning circuit during the last test.

Each bit in the register corresponds to one key switch. The bit is set if the switch has been detected as pressed by the key-scanning circuit during the last test.

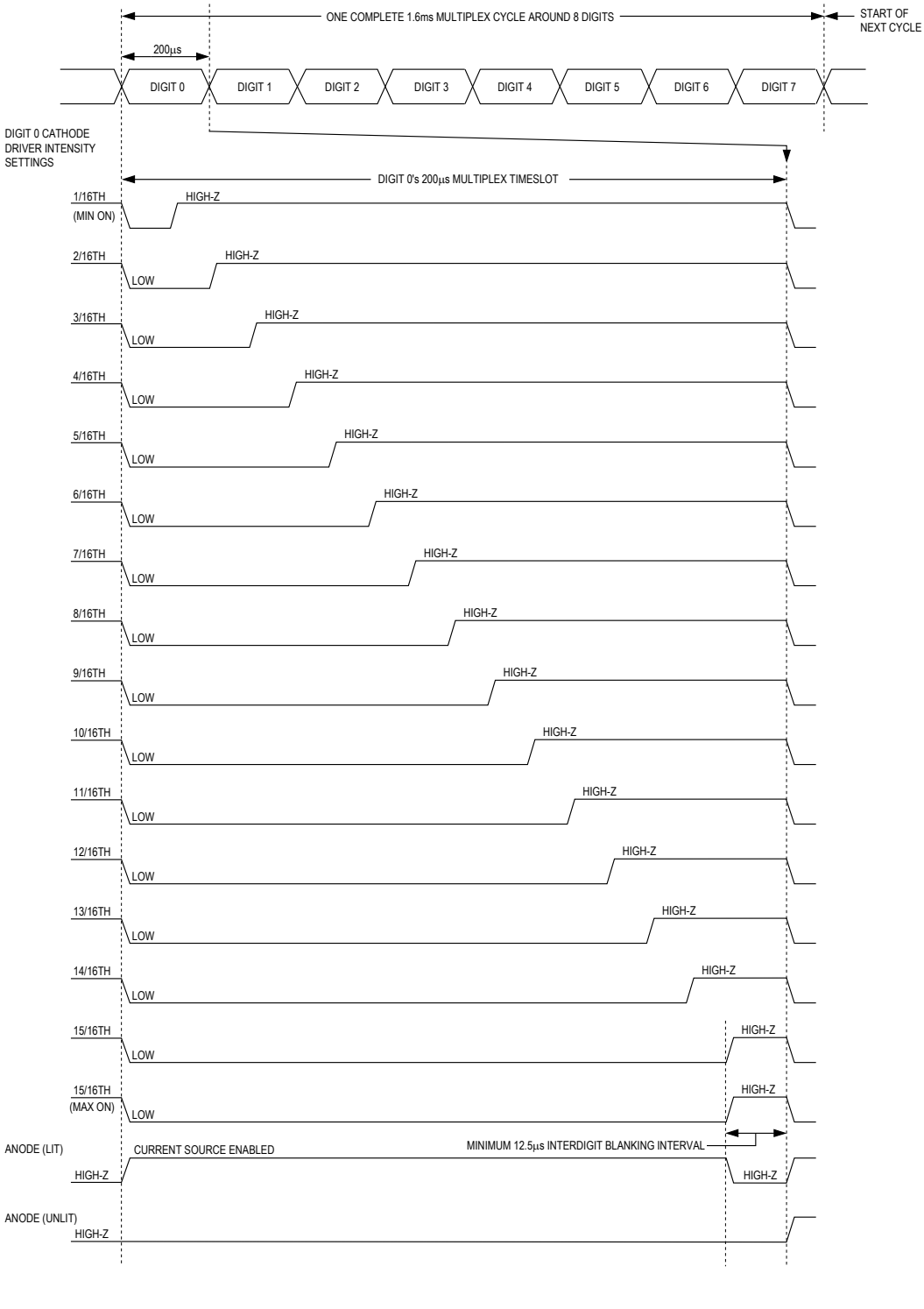


Figure 6. Multiplex Timing Diagram (OSC = 4MHz)

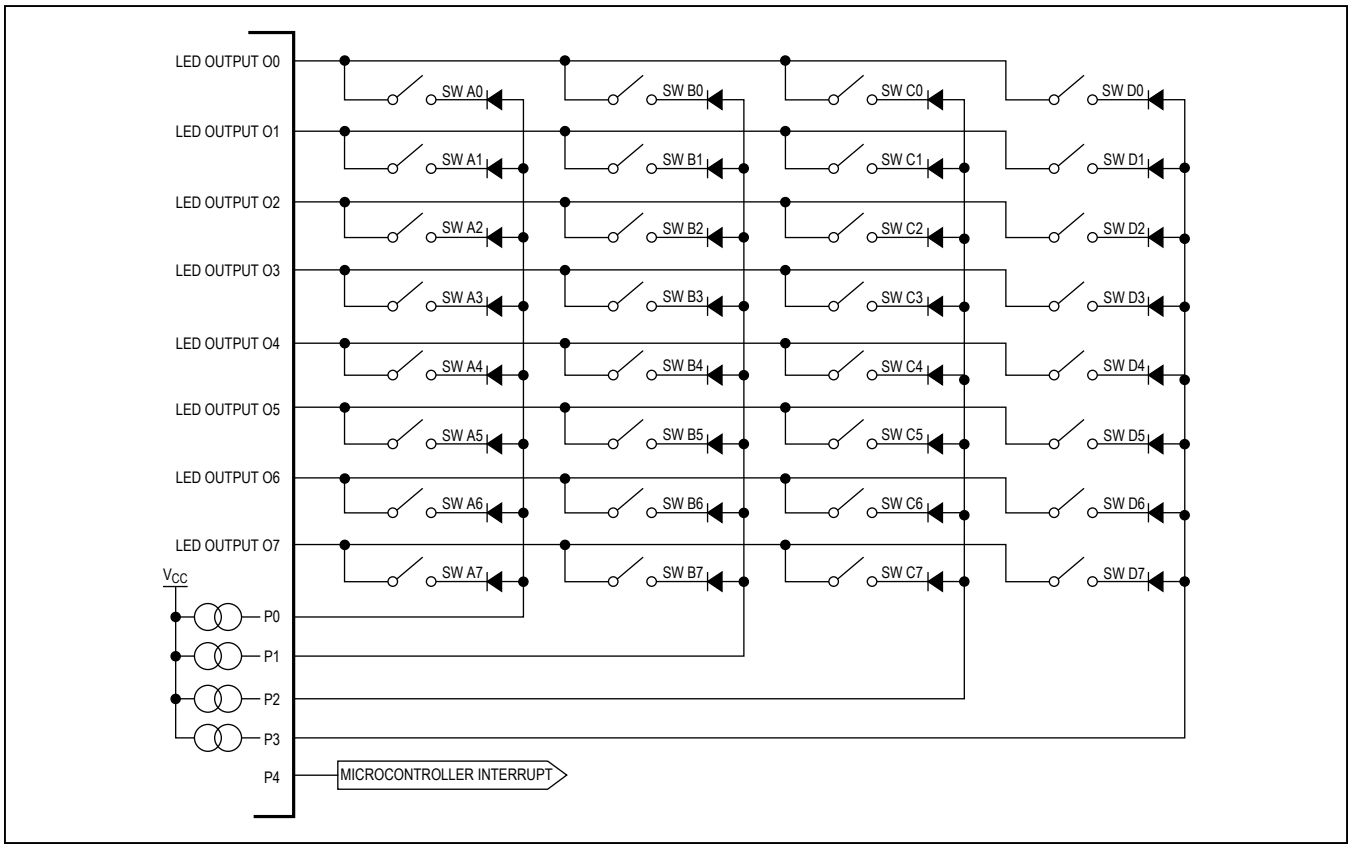


Figure 7. Key-Scanning Configuration

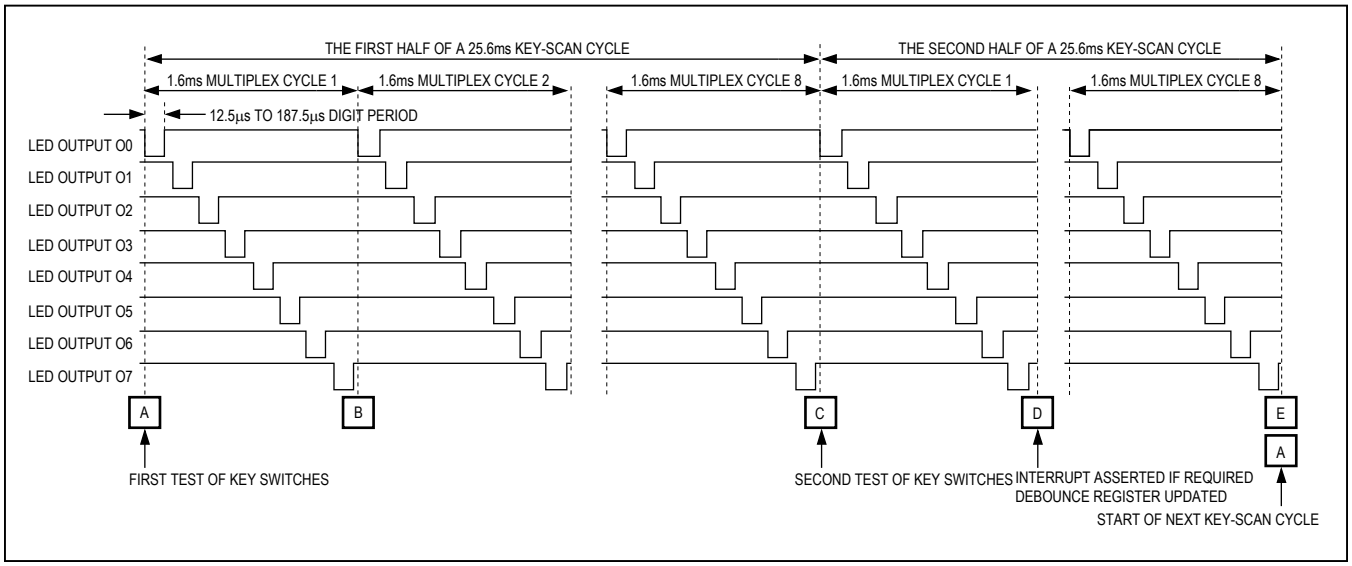


Figure 8. Key-Scan Timing Diagram

The bit is cleared if the switch has not been detected as pressed by the key-scanning circuit during the last test. Reading a pressed register does not clear that register or clear the IRQ output.

Display Test Register

The display test register (Table 36) operates in two modes: normal and display test. Display test mode turns all LEDs on (including DPs) by overriding, but not altering, all controls and digit registers (including the shutdown register), except for the digit-type register and the GPIO configuration register. The duty cycle, while in display test mode, is 7/16 (see the *Choosing Supply Voltage to Minimize Power Dissipation* section).

Selecting External Components R_{SET} and C_{SET} to Set Oscillator Frequency and Peak Segment Current

The RC oscillator uses an external resistor, R_{SET}, and an external capacitor, C_{SET}, to set the frequency, f_{OSC}. The allowed range of f_{OSC} is 1MHz to 8MHz. R_{SET} also sets the peak segment current. The recommended values of R_{SET} and C_{SET} set the oscillator to 4MHz, which makes the blink frequencies selectable between 0.5Hz and 1Hz. The recommended value of R_{SET} also sets the peak current to 40mA, which makes the segment current adjustable from 2.5mA to 37.5mA in 2.5mA steps.

$$I_{SEG} = KL / R_{SET} \text{ mA}$$
$$f_{OSC} = KF / (R_{SET} \times C_{SET}) \text{ MHz}$$

where:

K_L = 2240

K_F = 5376

R_{SET} = external resistor in kΩ

C_{SET} = external capacitor in pF

C_{STRAY} = stray capacitance from OSC pin to GND in pF, typically 2pF

The recommended value of R_{SET} is 56kΩ and the recommended value of C_{SET} is 22pF.

The recommended value or R_{SET} is the minimum allowed value, since it sets the display driver to the maximum allowed peak segment current. R_{SET} can be set to a higher value to set the segment current to a lower peak value where desired. The user must also ensure that the peak current specifications of the LEDs connected to the driver are not exceeded.

The effective value of RSET includes not only the actual external capacitor used, but also the stray capacitance from OSC to GND. This capacitance is usually in the 1pF to 5pF range, depending on the layout used.

Applications Information

Driving Bicolor LEDs

Bicolor digits group a red and a green die together for each display element, so that the element can be lit red or green (or orange), depending on which die (or both) is lit. The MAX6954 allows each segment's current to be set individually from the 1/16th (minimum current and LED intensity) to 15/16th (maximum current and LED intensity), as well as off (zero current). Thus, a bicolor (red-green) segment pair can be set to 256 color/intensity combinations.

Choosing Supply Voltage to Minimize Power Dissipation

The MAX6954 drives a peak current of 40mA into LEDs with a 2.2V forward-voltage drop when operated from a supply voltage of at least 3.0V. The minimum voltage drop across the internal LED drivers is therefore (3.0V - 2.2V) = 0.8V. If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.8V of headroom.

The voltage drop across the drivers with a nominal 5V supply (5.0V - 2.2V) = 2.8V is nearly 3 times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V) = 1.1V. In most systems, consumption is an important design criterion, and the MAX6954 should be operated from the system's 3.3V nominal supply. In other designs, the lowest supply voltage may be 5V. The issue now is to ensure the dissipation limit for the MAX6954 is not exceeded. This can be achieved by inserting a series resistor in the supply to the MAX6954, ensuring that the supply decoupling capacitors are still on the MAX6954 side of the resistor. For example, consider the requirement that the minimum supply voltage to a MAX6954 must be 3.0V, and the input supply range is 5V ±5%. Maximum supply current is 35mA + (40mA x 17) = 715mA. Minimum input supply voltage is 4.75V. Maximum series resistor value is (4.75V - 3.0V)/0.715A = 2.44Ω. We choose 2.2Ω ±5%. Worst-case resistor dissipation is at maximum toleranced resistance, i.e., (0.715A) 2 x (2.2Ω x 1.05) = 1.18W. The maximum MAX6954 supply voltage is at maximum input supply voltage and minimum toleranced resistance, i.e., 5.25V - (0.715A x 2.2Ω x 0.95) = 3.76V.

Low-Voltage Operation

The MAX6954 works over the 2.7V to 5.5V supply range. The minimum useful supply voltage is determined by the forward voltage drop of the LEDs at the

peak current ISEG, plus the 0.8V headroom required by the driver output stages. The MAX6954 correctly regulates I_{SEG} with a supply voltage above this minimum voltage. If the supply drops below this minimum voltage, the driver output stages may brown out, and be unable to regulate the current correctly. As the supply voltage drops further, the LED segment drive current becomes effectively limited by the output driver's on-resistance, and the LED drive current drops. The characteristics of each individual LED in a display digit are well matched, so the result is that the display intensity dims uniformly as supply voltage drops out of regulation and beyond.

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX6954 is determined from the following equation:

$$P_D = (V+ \times 35mA) + (V+ - V_{LED}) (DUTY \times I_{SEG} \times N)$$

where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 17)

V_{LED} = LED forward voltage at I_{SEG}

I_{SEG} = segment current set by R_{SET}

P_D = Power dissipation, in mW if currents are in mA

Dissipation example:

I_{SEG} = 30mA, N = 17, DUTY = 15/16,
V_{LED} = 2.4V at 30mA, V+ = 3.6V

P_D = 3.6V (35mA) + (3.6V - 2.4V)(15/16 x 30mA x 17) = 0.700W

Thus, for a 36-pin SSOP package (T_{JA} = 1 / 0.0118 = +85°C/W from Operating Ratings), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + (P_D \times T_{JA}) = +150°C$$
$$= T_A + (0.700 \times +85°C/W)$$

So T_A = +90.5°C. Thus, the part can be operated safely at a maximum package temperature of +85°C.

Power Supplies

The MAX6954 operates from a single 2.7V to 5.5V power supply. Bypass the power supply to GND with a 0.1µF capacitor as close to the device as possible. Add a 47µF capacitor if the MAX6954 is not close to the board's input bulk decoupling capacitor.

Terminating the Serial Interface

The MAX6954 uses fixed voltage thresholds of 0.6V and 1.8V for the 4-wire interface inputs. These fixed thresholds allow the MAX6954 to be controlled by a host operating from a lower supply voltage than the MAX6954; for example, 2.5V. The fixed thresholds also reduce the logic input noise margin when operating the MAX6954 from a higher supply voltage, such as 5V. At higher supply voltages, it may be necessary to fit termination components to the CLK, DIN, and $\overline{CS}$ inputs to avoid signal reflections that the MAX6954 could respond to as multiple transitions. Suitable termination components can be either a 33pF capacitor or 4.7kΩ resistor fitted from each of the CLK, DIN, and $\overline{CS}$ inputs to GND.

Table 7. 16-Segment Display Font Map

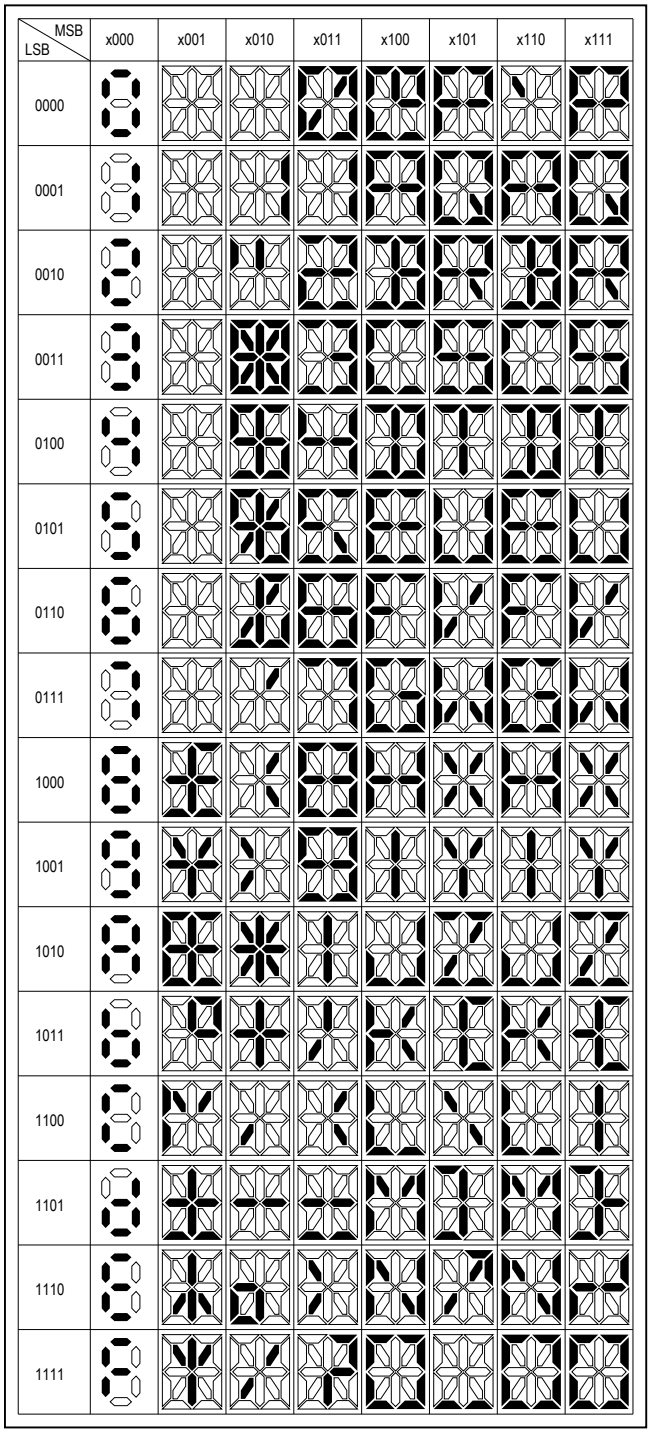


Table 8. 14-Segment Display Font Map

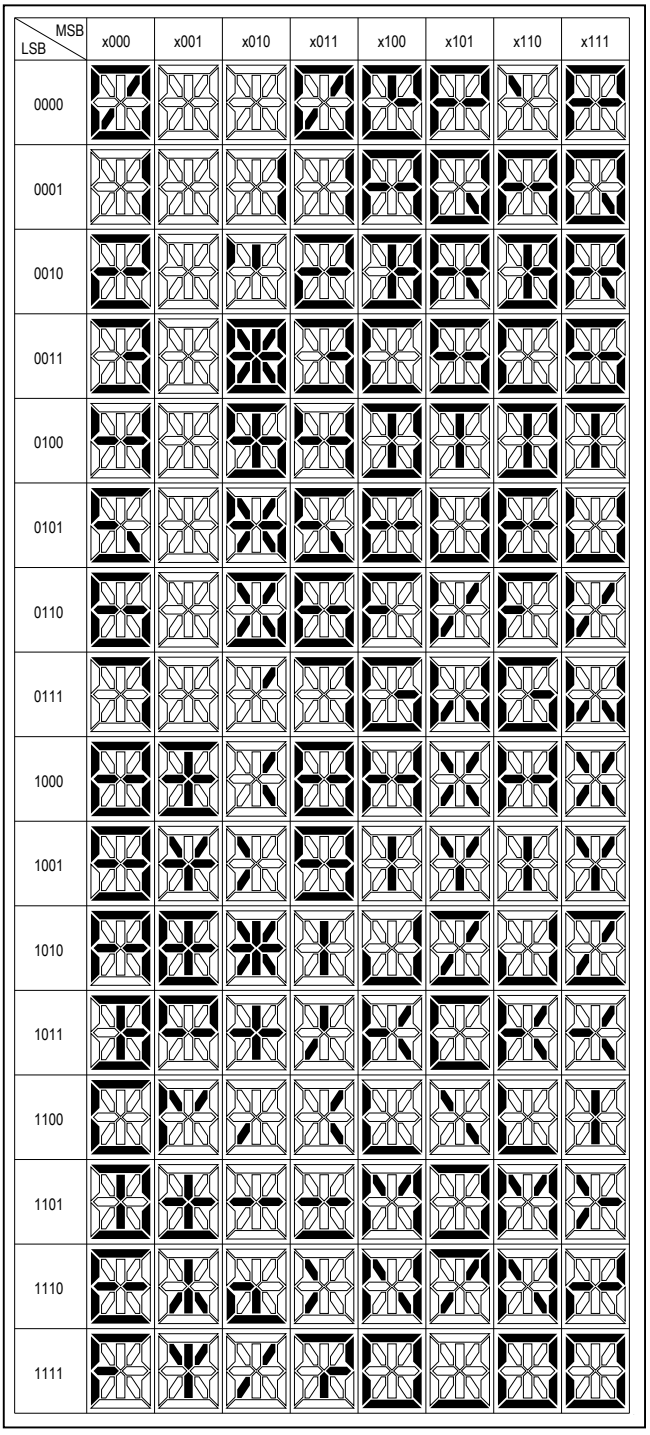


Table 9. Digit Plane Data Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
14-segment or 16-segment mode, writing digit data to use font map data with decimal place unlit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	0	Bits D6 to D0 select font characters 0 to 127						
14-segment or 16-segment mode, writing digit data to use font map data with decimal place lit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	1	Bits D6 to D0 select font characters 0 to 127						
7-segment decode mode, DP unlit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	0	0	0	0	D3 to D0			
7-segment decode mode, DP lit	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	1	0	0	0	D3 to D0			
7-segment no-decode mode	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	Direct control of 8 segments							

Table 10. Segment Decoding for 7-Segment Displays

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Segment Line	0x20 to 0x2F 0x40 to 0x4F 0x60 to 0x6F	dp	a	b	c	d	e	f	g

Table 11. 7-Segment Segment Mapping Decoder for Hexadecimal Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6, D5, D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0	—	X	0	0	0	0	—	1	1	1	1	1	1	0
1	—	X	0	0	0	1	—	0	1	1	0	0	0	0
2	—	X	0	0	1	0	—	1	1	0	1	1	0	1
3	—	X	0	0	1	1	—	1	1	1	1	0	0	1
4	—	X	0	1	0	0	—	0	1	1	0	0	1	1
5	—	X	0	1	0	1	—	1	0	1	1	0	1	1
6	—	X	0	1	1	0	—	1	0	1	1	1	1	1
7	—	X	0	1	1	1	—	1	1	1	0	0	0	0
8	—	X	1	0	0	0	—	1	1	1	1	1	1	1
9	—	X	1	0	0	1	—	1	1	1	1	0	1	1
A	—	X	1	0	1	0	—	1	1	1	0	1	1	1
B	—	X	1	0	1	1	—	0	0	1	1	1	1	1
C	—	X	1	1	0	0	—	1	0	0	1	1	1	0
D	—	X	1	1	0	1	—	0	1	1	1	1	0	1
E	—	X	1	1	1	0	—	1	0	0	1	1	1	1
F	—	X	1	1	1	1	—	1	0	0	0	1	1	1

**The decimal point is set by bit D7 = 1.*

Table 12. Digit-Type Register

DIGIT-TYPE REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Output Drive Line	0x0C	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Slot Identification		Slot 4		Slot 3		Slot 2		Slot 1	

Table 13. Example Configurations for Display Digit Combinations

DIGIT-TYPE REGISTER SETTING	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Digits 7 to 0 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	0	0	0
Digit 0 is a 14-segment digit, digits 7 to 1 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	0	0	1
Digits 2 to 0 are 14-segment digits, digits 7 to 3 are 16-segment or 7-segment digits.	0x0C	0	0	0	0	0	1	1	1
Digits 7 to 0 are 14-segment digits.	0x0C	1	1	1	1	1	1	1	1

Table 14. Decode-Mode Register Examples

DECODE MODE	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digit pairs 7 to 0.	0x01	0	0	0	0	0	0	0	0	0x00
Hexadecimal decode for digit pair 0, no decode for digit pairs 7 to 1.	0x01	0	0	0	0	0	0	0	1	0x01
Hexadecimal decode for digit pairs 2 to 0, no decode for digit pairs 7 to 3.	0x01	0	0	0	0	0	1	1	1	0x07
Hexadecimal decode for digit pairs 7 to 0.	0x01	1	1	1	1	1	1	1	1	0xFF

Table 15. Initial Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Decode Mode	Decode mode enabled	0x01	1	1	1	1	1	1	1	1
Global Intensity	1/16 (min on)	0x02	X	X	X	X	0	0	0	0
Scan Limit	Display 8 digits: 0, 1, 2, 3, 4, 5, 6, 7	0x03	X	X	X	X	X	1	1	1
Control Register	Shutdown enabled, blink speed is slow, blink disabled	0x04	0	0	X	X	0	0	0	0
GPIO Data	Outputs are low	0x05	X	X	X	0	0	0	0	0
Port Configuration	No key scanning, P0 to P4 are all inputs	0x06	0	0	0	1	1	1	1	1
Display Test	Normal operation	0x07	X	X	X	X	X	X	X	0
Key_A Mask	None of the keys cause interrupt	0x08	0	0	0	0	0	0	0	0
Key_B Mask	None of the keys cause interrupt	0x09	0	0	0	0	0	0	0	0
Key_C Mask	None of the keys cause interrupt	0x0A	0	0	0	0	0	0	0	0
Key_D Mask	None of the keys cause interrupt	0x0B	0	0	0	0	0	0	0	0
Digit Type	All are 16 segment or 7 segment	0x0C	0	0	0	0	0	0	0	0
Intensity10	1/16 (min on)	0x10	0	0	0	0	0	0	0	0
Intensity32	1/16 (min on)	0x11	0	0	0	0	0	0	0	0
Intensity54	1/16 (min on)	0x12	0	0	0	0	0	0	0	0
Intensity76	1/16 (min on)	0x13	0	0	0	0	0	0	0	0
Intensity10a	1/16 (min on)	0x14	0	0	0	0	0	0	0	0
Intensity32a	1/16 (min on)	0x15	0	0	0	0	0	0	0	0
Intensity54a	1/16 (min on)	0x16	0	0	0	0	0	0	0	0
Intensity76a	1/16 (min on)	0x17	0	0	0	0	0	0	0	0
Digit 0	Blank digit, both planes	0x60	0	0	1	0	0	0	0	0
Digit 1	Blank digit, both planes	0x61	0	0	1	0	0	0	0	0
Digit 2	Blank digit, both planes	0x62	0	0	1	0	0	0	0	0
Digit 3	Blank digit, both planes	0x63	0	0	1	0	0	0	0	0
Digit 4	Blank digit, both planes	0x64	0	0	1	0	0	0	0	0
Digit 5	Blank digit, both planes	0x65	0	0	1	0	0	0	0	0
Digit 6	Blank digit, both planes	0x66	0	0	1	0	0	0	0	0
Digit 7	Blank digit, both planes	0x67	0	0	1	0	0	0	0	0
Digit 0a	Blank digit, both planes	0x68	0	0	0	0	0	0	0	0
Digit 1a	Blank digit, both planes	0x69	0	0	0	0	0	0	0	0
Digit 2a	Blank digit, both planes	0x6A	0	0	0	0	0	0	0	0
Digit 3a	Blank digit, both planes	0x6B	0	0	0	0	0	0	0	0
Digit 4a	Blank digit, both planes	0x6C	0	0	0	0	0	0	0	0
Digit 5a	Blank digit, both planes	0x6D	0	0	0	0	0	0	0	0
Digit 6a	Blank digit, both planes	0x6E	0	0	0	0	0	0	0	0
Digit 7a	Blank digit, both planes	0x6F	0	0	0	0	0	0	0	0
Key_A Debounced	No key presses have been detected	0x88	0	0	0	0	0	0	0	0
Key_B Debounced	No key presses have been detected	0x89	0	0	0	0	0	0	0	0
Key_C Debounced	No key presses have been detected	0x8A	0	0	0	0	0	0	0	0
Key_D Debounced	No key presses have been detected	0x8B	0	0	0	0	0	0	0	0
Key_A Pressed	Keys are not pressed	0x8C	0	0	0	0	0	0	0	0
Key_B Pressed	Keys are not pressed	0x8D	0	0	0	0	0	0	0	0
Key_C Pressed	Keys are not pressed	0x8E	0	0	0	0	0	0	0	0
Key_D Pressed	Keys are not pressed	0x8F	0	0	0	0	0	0	0	0

Table 16. Configuration Register Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	P	I	R	T	E	B	X	S

Table 17. Shutdown Control (S Data Bit DO) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	P	I	R	T	E	B	X	0
Normal Operation	P	I	R	T	E	B	X	1

Table 18. Blink Rate Selection (B Data Bit D2) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Slow blinking. Segments blink on for 1s, off for 1s with f_{OSC} = 4MHz.	P	I	R	T	E	0	X	S
Fast blinking. Segments blink on for 0.5s, off for 0.5s with f_{OSC} = 4MHz.	P	I	R	T	E	1	X	S

Table 19. Global Blink Enable/Disable (E Data Bit D3) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Blink function is disabled.	P	I	R	T	0	B	X	S
Blink function is enabled.	P	I	R	T	1	B	X	S

Table 20. Digit Register Mapping with Blink Globally Enabled

SEGMENT'S BIT SETTING IN PLANE P1	SEGMENT'S BIT SETTING IN PLANE P0	SEGMENT BEHAVIOR
0	0	Segment off.
0	1	Segment on only during the 1st half of each blink period.
1	0	Segment on only during the 2nd half of each blink period.
1	1	Segment on.

Table 21. Global Blink Timing Synchronization (T Data Bit D4) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Blink timing counters are unaffected.	P	I	R	0	E	B	X	S
Blink timing counters are reset on the rising edge of $\overline{CS}$.	P	I	R	1	E	B	X	S

Table 22. Global Clear Digit Data (R Data Bit D5) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Digit data for both planes P0 and P1 are unaffected.	P	I	0	T	E	B	X	S
Digit data for both planes P0 and P1 are cleared on the rising edge of $\overline{CS}$.	P	I	1	T	E	B	X	S

Table 23. Global Intensity (I Data Bit D6) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Intensity for all digits is controlled by one setting in the global intensity register.	P	0	R	T	E	B	X	S
Intensity for digits is controlled by the individual settings in the intensity10 and intensity76 registers.	P	1	R	T	E	B	X	S

Table 24. Blink Phase Readback (P Data Bit D7) Format

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
P1 Blink Phase	0	I	R	T	E	B	X	S
P0 Blink Phase	1	I	R	T	E	B	X	S

Table 25. Scan-Limit Register Format

SCAN LIMIT	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
		D7	D6	D5	D4	D3	D2	D1	D0	
Display Digit 0 only	0x03	X	X	X	X	X	0	0	0	0x00
Display Digits 0 and 1	0x03	X	X	X	X	X	0	0	1	0x01
Display Digits 0 1 2	0x03	X	X	X	X	X	0	1	0	0x02
Display Digits 0 1 2 3	0x03	X	X	X	X	X	0	1	1	0x03
Display Digits 0 1 2 3 4	0x03	X	X	X	X	X	1	0	0	0x04
Display Digits 0 1 2 3 4 5	0x03	X	X	X	X	X	1	0	1	0x05
Display Digits 0 1 2 3 4 5 6	0x03	X	X	X	X	X	1	1	0	0x06
Display Digits 0 1 2 3 4 5 6 7	0x03	X	X	X	X	X	1	1	1	0x07

Table 26. Global Intensity Register Format

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
			D7	D6	D5	D4	D3	D2	D1	D0	
1/16 (min on)	2.5	0x02	X	X	X	X	0	0	0	0	0xX0
2/16	5	0x02	X	X	X	X	0	0	0	1	0xX1
3/16	7.5	0x02	X	X	X	X	0	0	1	0	0xX2
4/16	10	0x02	X	X	X	X	0	0	1	1	0xX3
5/16	12.5	0x02	X	X	X	X	0	1	0	0	0xX4
6/16	15	0x02	X	X	X	X	0	1	0	1	0xX5
7/16	17.5	0x02	X	X	X	X	0	1	1	0	0xX6
8/16	20	0x02	X	X	X	X	0	1	1	1	0xX7
9/16	22.5	0x02	X	X	X	X	1	0	0	0	0xX8
10/16	25	0x02	X	X	X	X	1	0	0	1	0xX9
11/16	27.5	0x02	X	X	X	X	1	0	1	0	0xXA
12/16	30	0x02	X	X	X	X	1	0	1	1	0xXB
13/16	32.5	0x02	X	X	X	X	1	1	0	0	0xXC
14/16	35	0x02	X	X	X	X	1	1	0	1	0xXD
15/16	37.5	0x02	X	X	X	X	1	1	1	0	0xXE
15/16 (max on)	37.5	0x02	X	X	X	X	1	1	1	1	0xXF

Table 27. Individual Segment Intensity Registers

REGISTER FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Intensity10 Register	0x10	Digit 1				Digit 0			
Intensity32 Register	0x11	Digit 3				Digit 2			
Intensity54 Register	0x12	Digit 5				Digit 4			
Intensity76 Register	0x13	Digit 7				Digit 6			
Intensity10a Register	0x14	Digit 1a (7 segment only)				Digit 0a (7 segment only)			
Intensity32a Register	0x15	Digit 3a (7 segment only)				Digit 2a (7 segment only)			
Intensity54a Register	0x16	Digit 5a (7 segment only)				Digit 4a (7 segment only)			
Intensity76a Register	0x17	Digit 7a (7 segment only)				Digit 6a (7 segment only)			

Table 28. Even Individual Segment Intensity Format

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
			D7	D6	D5	D4	D3	D2	D1	D0	
1/16 (min on)	2.5	0x10 to 0x17	See Table 29.				0	0	0	0	0xX0
2/16	5	0x10 to 0x17					0	0	0	1	0xX1
3/16	7.5	0x10 to 0x17					0	0	1	0	0xX2
4/16	10	0x10 to 0x17					0	0	1	1	0xX3
5/16	12.5	0x10 to 0x17					0	1	0	0	0xX4
6/16	15	0x10 to 0x17					0	1	0	1	0xX5
7/16	17.5	0x10 to 0x17					0	1	1	0	0xX6
8/16	20	0x10 to 0x17					0	1	1	1	0xX7
9/16	22.5	0x10 to 0x17					1	0	0	0	0xX8
10/16	25	0x10 to 0x17					1	0	0	1	0xX9
11/16	27.5	0x10 to 0x17					1	0	1	0	0xXA
12/16	30	0x10 to 0x17					1	0	1	1	0xXB
13/16	32.5	0x10 to 0x17					1	1	0	0	0xXC
14/16	35	0x10 to 0x17					1	1	0	1	0xXD
15/16	37.5	0x10 to 0x17					1	1	1	0	0xXE
15/16 (max on)	37.5	0x10 to 0x17					1	1	1	1	0xXF

Table 29. Odd Individual Segment Intensity Format

DUTY CYCLE	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	REGISTER DATA								HEX CODE
			D7	D6	D5	D4	D3	D2	D1	D0	
1/16 (min on)	2.5	0x10 to 0x17	0	0	0	0	See Table 28.				0x0X
2/16	5	0x10 to 0x17	0	0	0	1					0x1X
3/16	7.5	0x10 to 0x17	0	0	1	0					0x2X
4/16	10	0x10 to 0x17	0	0	1	1					0x3X
5/16	12.5	0x10 to 0x17	0	1	0	0					0x4X
6/16	15	0x10 to 0x17	0	1	0	1					0x5X
7/16	17.5	0x10 to 0x17	0	1	1	0					0x6X
8/16	20	0x10 to 0x17	0	1	1	1					0x7X
9/16	22.5	0x10 to 0x17	1	0	0	0					0x8X
10/16	25	0x10 to 0x17	1	0	0	1					0x9X
11/16	27.5	0x10 to 0x17	1	0	1	0					0xAX
12/16	30	0x10 to 0x17	1	0	1	1					0xBX
13/16	32.5	0x10 to 0x17	1	1	0	0					0xCX
14/16	35	0x10 to 0x17	1	1	0	1					0xDX
15/16	37.5	0x10 to 0x17	1	1	1	0					0xEX
15/16 (max on)	37.5	0x10 to 0x17	1	1	1	1					0xFX

Table 30. GPIO Data Register

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Write GPIO Data	0x05	X	X	X	P4	P3	P2	P1	P0
Read GPIO Data	0x85	0	0	0	P4 or IRQ status	P3	P2	P1	P0

Table 31. Port Scanning Function Allocation

KEYS SCANNED	PORTS AVAILABLE	P0	P1	P2	P3	P4
None	5 pins	GPIO	GPIO	GPIO	GPIO	GPIO
1 to 8	3 pins	Key_A	GPIO	GPIO	GPIO	IRQ
9 to 16	2 pins	Key_A	Key_B	GPIO	GPIO	IRQ
17 to 24	1 pin	Key_A	Key_B	Key_C	GPIO	IRQ
25 to 36	None	Key_A	Key_B	Key_C	Key_D	IRQ

Table 32. Port Configuration Register Format

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
GPIO Configuration Register	0x06	Set number of keys scanned			Set port direction for ports P0 to P4: 0 = output, 1 = input				
PORT ALLOCATION OPTIONS									
0 Keys Scanned	0x06	0	0	0	P4	P3	P2	P1	P0
8 Keys Scanned	0x06	0	0	1	IRQ	P3	P2	P1	Key_A
16 Keys Scanned	0x06	0	1	0	IRQ	P3	P2	Key_B	Key_A
24 Keys Scanned	0x06	0	1	1	IRQ	P3	Key_C	Key_B	Key_A
32 Keys Scanned	0x06	1	X	X	IRQ	Key_D	Key_C	Key_B	Key_A
EXAMPLE PORT CONFIGURATION SETTINGS									
No Keys Scanned, P4 and P2 Are Outputs, Others Are Inputs	0x06	0	0	0	0	1	0	1	1
8 Keys Scanned, P3 and P1 Are Outputs, P2 Is an Input	0x06	0	0	1	X	0	1	0	X
32 Keys Scanned, No GPIO Ports	0x06	1	X	X	X	X	X	X	X

Table 33. Key Mask Register Format

KEY MASK REGISTER	ADDRESS CODE (HEX	REGISTER DATA WITH APPROPRIATE SWITCH NAMED BELOW							
		D7	D6	D5	D4	D3	D2	D1	D0
Key_A Mask Register	0x08	SW_A7	SW_A6	SW_A5	SW_A4	SW_A3	SW_A2	SW_A1	SW_A0
Key_B Mask Register	0x09	SW_B7	SW_B6	SW_B5	SW_B4	SW_B3	SW_B2	SW_B1	SW_B0
Key_C Mask Register	0x0A	SW_C7	SW_C6	SW_C5	SW_C4	SW_C3	SW_C2	SW_C1	SW_C0
Key_D Mask Register	0x0B	SW_ D7	SW_D6	SW_D5	SW_D4	SW_D3	SW_D2	SW_D1	SW_D0

Table 34. Key Debounced Register Format

KEY DEBOUNCED REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Key_A Debounced Register	0x88	SW_A7	SW_A6	SW_A5	SW_A4	SW_A3	SW_A2	SW_A1	SW_A0
Key_B Debounced Register	0x89	SW_B7	SW_B6	SW_B5	SW_B4	SW_B3	SW_B2	SW_B1	SW_B0
Key_C Debounced Register	0x8A	SW_C7	SW_C6	SW_C5	SW_C4	SW_C3	SW_C2	SW_C1	SW_C0
Key_D Debounced Register	0x8B	SW_D7	SW_D6	SW_D5	SW_D4	SW_D3	SW_D2	SW_D1	SW_D0

Table 35. Key Pressed Register Format

KEY PRESSED REGISTER	ADDRESS CODE (HEX	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Key_A Pressed Register	0x8C	SW_A7	SW_A6	SW_A5	SW_A4	SW_A3	SW_A2	SW_A1	SW_A0
Key_B Pressed Register	0x8D	SW_B7	SW_B6	SW_B5	SW_B4	SW_B3	SW_B2	SW_B1	SW_B0
Key_C Pressed Register	0x8E	SW_C7	SW_C6	SW_C5	SW_C4	SW_C3	SW_C2	SW_C1	SW_C0
Key_D Pressed Register	0x8F	SW_D7	SW_D6	SW_D5	SW_D4	SW_D3	SW_D2	SW_D1	SW_D0

Table 36. Display Test Register

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	0x07	X	X	X	X	X	X	X	0
Display Test	0x07	X	X	X	X	X	X	X	1

Table 37. Slot 1 Configuration

CONFIGURATION CHOICE Common-Cathode Drive: Digit Type	CC0: 16-seg monocolor	CC1: 16-seg monocolor	CC0 and CC1: (2) 7-seg bicolor or (4) 7-seg monocolor or (1) 7-seg bicolor and (2) 7-seg monocolor*	CC0 and CC1: (1)16-seg bicolor	CC0: 16-seg monocolor	CC0: (2) 7-seg monocolor* **or** 7-seg bicolor	CC1: 14-seg monocolor	CC0: 14-seg monocolor	CC1: 16-seg monocolor	CC1: (2) 7-seg monocolor* **or** 7-seg bicolor	CC0 and CC1: (2) 14-seg monocolor or 14-seg bicolor
00	CC0	—	CC0	CC0	CC0	CC0	—	CC0	—	—	CC0
01	—	CC1	CC1	CC1	—	—	CC1	—	CC1	CC1	CC1
02	a1	a1	1a	a1	a1	1a	a	a	a1	1a	a
03	a2	a2	—	a2	a2	—	—	—	a2	—	—
04	b	b	1b	b	b	1b	b	b	b	1b	b
05	c	c	1c	c	c	1c	c	c	c	1c	c
06	d1	d1	1d	d1	d1	1d	d	d	d1	1d	d
07	d2	d2	1dp	d2	d2	1dp	—	—	d2	1dp	—
08	e	e	1e	e	e	1e	e	e	e	1e	e
09	f	f	1f	f	f	1f	f	f	f	1f	f
010	g1	g1	1g	g1	g1	1g	g1	g1	g1	1g	g1
011	g2	g2	2a	g2	g2	2a	g2	g2	g2	2a	g2
012	h	h	2b	h	h	2b	h	h	h	2b	h
013	i	i	2c	i	i	2c	i	i	i	2c	i
014	j	j	2d	j	j	2d	j	j	j	2d	j
015	k	k	2e	k	k	2e	k	k	k	2e	k
016	l	l	2f	l	l	2f	l	l	l	2f	l
017	m	m	2g	m	m	2g	m	m	m	2g	m
018	dp	dp	2dp	dp	dp	2dp	dp	dp	dp	2dp	dp
ADDRESS CODE (HEX)	0x0C										
REGISTER DATA D7	See Table 40.										
D6											
D5	See Table 39.										
D4											
D3	See Table 38.										
D2											
D1	0			1			0			1	
D0	0			0			1			1	

**7-segment digits can be replaced by directly controlled discrete LEDs according to settings in decode mode register (Table 11).*

***The highlighted row is used in Typical Operating Circuit 1 for display digits 0 and 1.*

Table 38. Slot 2 Configuration

CONFIGURATION CHOICE Common-Cathode Drive: Digit Type		CC2: 16-seg monocolor	CC3: 16-seg monocolor	CC2 and CC3: (2) 7-seg bicolor **or** (4) 7-seg monocolor **or** (1) 7-seg bicolor and (2) 7-seg monocolor*	CC2 and CC3: (1)16-seg bicolor	CC2: 16-seg monocolor	CC2: (2) 7-seg monocolor* **or** 7-seg bicolor	CC3: 14-seg monocolor	CC2: 14-seg monocolor	CC3: 16-seg monocolor	CC3: (2) 7-seg monocolor* **or** 7-seg bicolor	CC2 and CC3: (2) 14-seg monocolor or 14-seg bicolor
00		a1	a1	1a	a1	a1	1a	a	a	a1	1a	a
01		a2	a2	—	a2	a2	—	—	—	a2	—	—
02		CC2	—	CC2	CC2	CC2	CC2	—	CC2	—	—	CC2
03		—	CC3	CC3	CC3	—	—	CC3	—	CC3	CC3	CC3
04		b	b	1b	b	b	1b	b	b	b	1b	b
05		c	c	1c	c	c	1c	c	c	c	1c	c
06		d1	d1	1d	d1	d1	1d	d	d	d1	1d	d
07		d2	d2	1dp	d2	d2	1dp	—	—	d2	1dp	—
08		e	e	1e	e	e	1e	e	e	e	1e	e
09		f	f	1f	f	f	1f	f	f	f	1f	f
010		g1	g1	1g	g1	g1	1g	g1	g1	g1	1g	g1
011		g2	g2	2a	g2	g2	2a	g2	g2	g2	2a	g2
012		h	h	2b	h	h	2b	h	h	h	2b	h
013		i	i	2c	i	i	2c	i	i	i	2c	i
014		j	j	2d	j	j	2d	j	j	j	2d	j
015		k	k	2e	k	k	2e	k	k	k	2e	k
016		l	l	2f	l	l	2f	l	l	l	2f	l
017		m	m	2g	m	m	2g	m	m	m	2g	m
018		dp	dp	2dp	dp	dp	2dp	dp	dp	dp	2dp	dp
ADDRESS CODE (HEX)		0x0C										
REGISTER DATA	D7	See Table 40.										
	D6											
	D5	See Table 39.										
	D4											
	D3	0				1			0			1
	D2	0				0			1			1
	D1	See Table 37.										
	D0											

**7-segment digits can be replaced by directly controlled discrete LEDs according to settings in decode mode register (Table 11).*

***The highlighted row is used in Typical Operating Circuit 1 for display digits 2 and 3.*

Table 39. Slot 3 Configuration

CONFIGURATION CHOICE Common-Cathode Drive: Digit Type		CC4: 16-seg monocolor	CC5: 16-seg monocolor	CC4 and CC5: (2) 7-seg bicolor **or** (4) 7-seg monocolor **or** (1) 7-seg bicolor and (2) 7-seg monocolor*	CC4 and CC5: (1)16-seg bicolor	CC4: 16-seg monocolor	CC4: (2) 7-seg monocolor* **or** 7-seg bicolor	CC5: 14-seg monocolor	CC4: 14-seg monocolor	CC5: 16-seg monocolor	CC5: (2) 7-seg monocolor* **or** 7-seg bicolor	CC4 and CC5: (2) 14-seg monocolor **or** 14-seg bicolor
00		a1	a1	1a	a1	a1	1a	a	a	a1	1a	a
01		a2	a2	—	a2	a2	—	—	—	a2	—	—
02		b	b	1b	b	b	1b	b	b	b	1b	b
03		c	c	1c	c	c	1c	c	c	c	1c	c
04		CC4	—	CC4	CC4	CC4	CC4	—	CC4	—	—	CC4
05		—	CC5	CC5	CC5	—	—	CC5	—	CC5	CC5	CC5
06		d1	d1	1d	d1	d1	1d	d	d	d1	1d	d
07		d2	d2	1dp	d2	d2	1dp	—	—	d2	1dp	—
08		e	e	1e	e	e	1e	e	e	e	1e	e
09		f	f	1f	f	f	1f	f	f	f	1f	f
010		g1	g1	1g	g1	g1	1g	g1	g1	g1	1g	g1
011		g2	g2	2a	g2	g2	2a	g2	g2	g2	2a	g2
012		h	h	2b	h	h	2b	h	h	h	2b	h
013		i	i	2c	i	i	2c	i	i	i	2c	i
014		j	j	2d	j	j	2d	j	j	j	2d	j
015		k	k	2e	k	k	2e	k	k	k	2e	k
016		l	l	2f	l	l	2f	l	l	l	2f	l
017		m	m	2g	m	m	2g	m	m	m	2g	m
018		dp	dp	2dp	dp	dp	2dp	dp	dp	dp	2dp	dp
ADDRESS CODE (HEX)		0x0C										
REGISTER DATA	D7	See Table 40.										
	D6											
	D5	0				1			0			1
	D4	0				0			1			1
	D3	See Table 38.										
	D2											
	D1	See Table 37.										
	D0											

**7-segment digits can be replaced by directly controlled discrete LEDs according to settings in decode mode register (Table 11).*

***The highlighted row is used in Typical Operating Circuit 1 for display digits 4 and 5.*

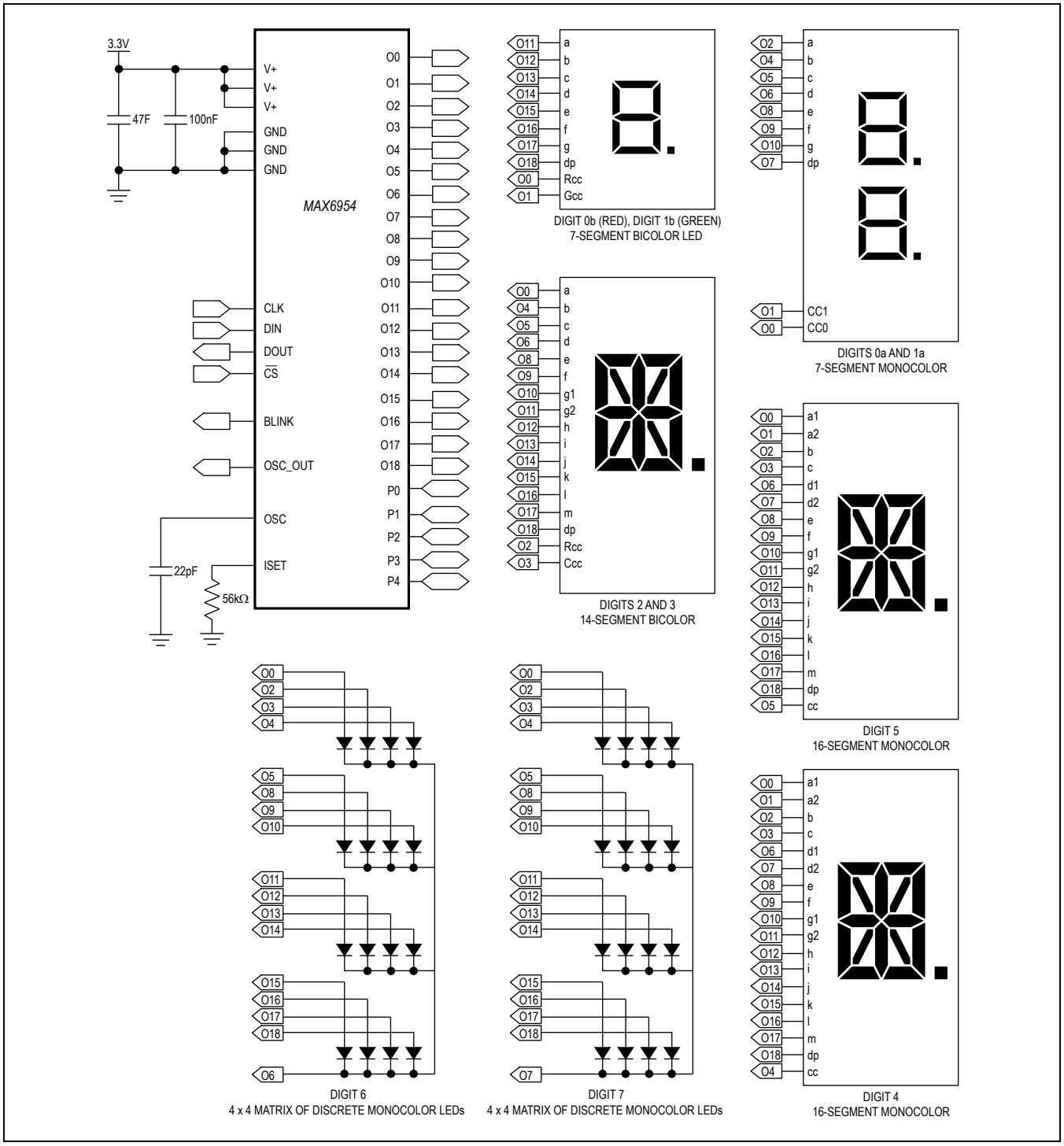
Table 40. Slot 4 Configuration

CONFIGURATION CHOICE Common-Cathode Drive: Digit Type		CC6: 16-seg monocolor	CC7: 16-seg monocolor	CC6 and CC7: (2) 7-seg bicolor **or** (4) 7-seg monocolor **or** (1) 7-seg bicolor and (2) 7-seg monocolor*	CC6 and CC7: (1)16-seg bicolor	CC6: 16-seg monocolor	CC6: (2) 7-seg monocolor* **or** 7-seg bicolor	CC7: 14-seg monocolor	CC6: 14-seg monocolor	CC7: 16-seg monocolor	CC7: (2) 7-seg monocolor* **or** 7-seg bicolor	CC6 and CC7: (2) 14-seg monocolor **or** 14-seg bicolor
00		a1	a1	1a	a1	a1	1a	a	a	a1	1a	a
01		a2	a2	—	a2	a2	—	—	—	a2	—	—
02		b	b	1b	b	b	1b	b	b	b	1b	b
03		c	c	1c	c	c	1c	c	c	c	1c	c
04		d1	d1	1d	d1	d1	1d	d	d	d1	1d	d
05		d2	d2	1dp	d2	d2	1dp	—	—	d2	1dp	—
06		CC6	—	CC6	CC6	CC6	CC6	—	CC6	—	—	CC6
07		—	CC7	CC7	CC7	—	—	CC7	—	CC7	CC7	CC7
08		e	e	1e	e	e	1e	e	e	e	1e	e
09		f	f	1f	f	f	1f	f	f	f	1f	f
010		g1	g1	1g	g1	g1	1g	g1	g1	g1	1g	g1
011		g2	g2	2a	g2	g2	2a	g2	g2	g2	2a	g2
012		h	h	2b	h	h	2b	h	h	h	2b	h
013		i	i	2c	i	i	2c	i	i	i	2c	i
014		j	j	2d	j	j	2d	j	j	j	2d	j
015		k	k	2e	k	k	2e	k	k	k	2e	k
016		l	l	2f	l	l	2f	l	l	l	2f	l
017		m	m	2g	m	m	2g	m	m	m	2g	m
018		dp	dp	2dp	dp	dp	2dp	dp	dp	dp	2dp	dp
ADDRESS CODE (HEX)		0x0C										
REGISTER DATA	D7	0				1			0			1
	D6	0				0			1			1
	D5	See Table 39.										
	D4											
	D3	See Table 38.										
	D2											
	D1	See Table 37.										
	D0											

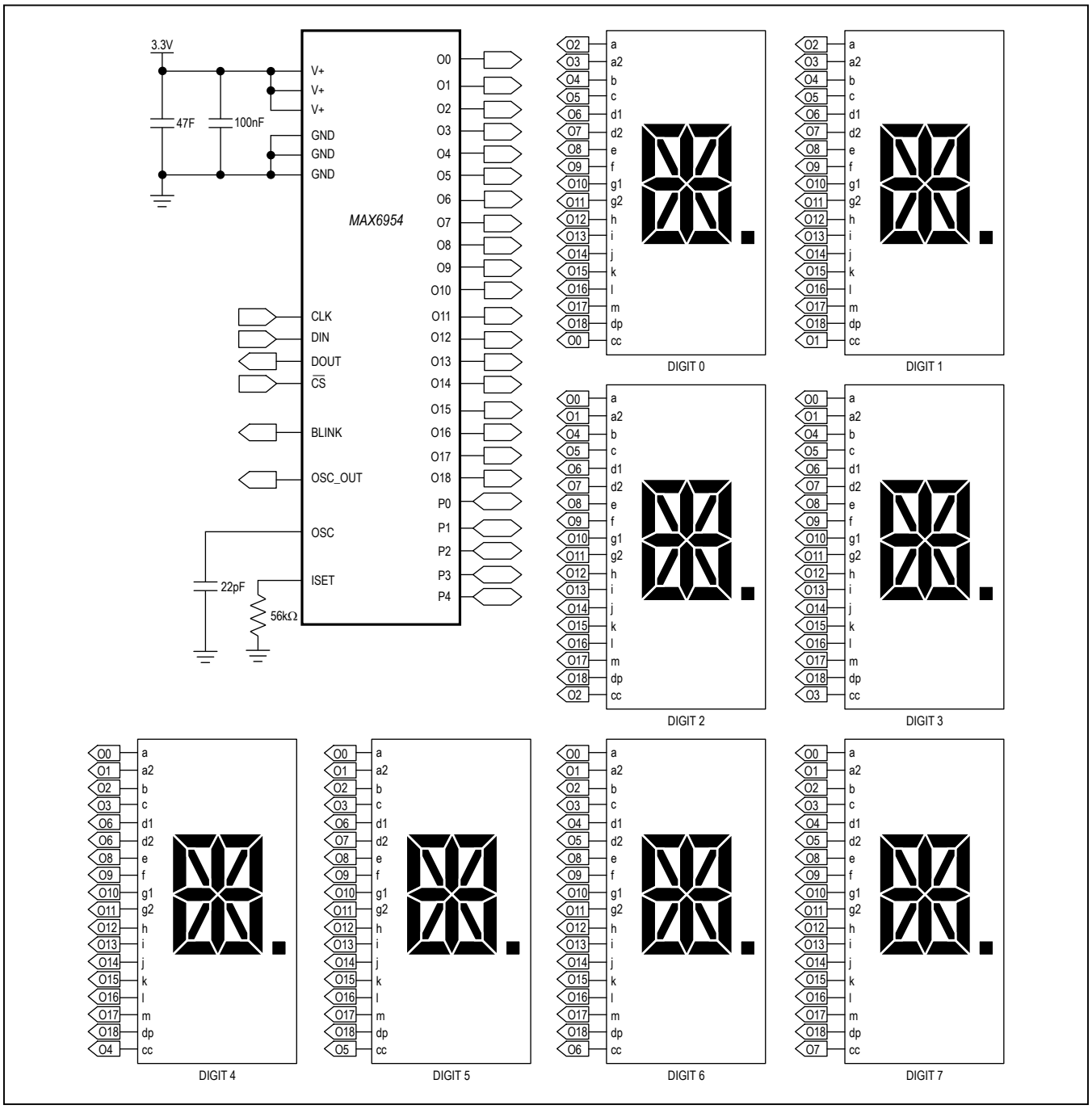
**7-segment digits can be replaced by directly controlled discrete LEDs according to settings in the decode mode register (Table 11).*

***The highlighted row is used in Typical Operating Circuit 1 for display digits 6 and 7.*

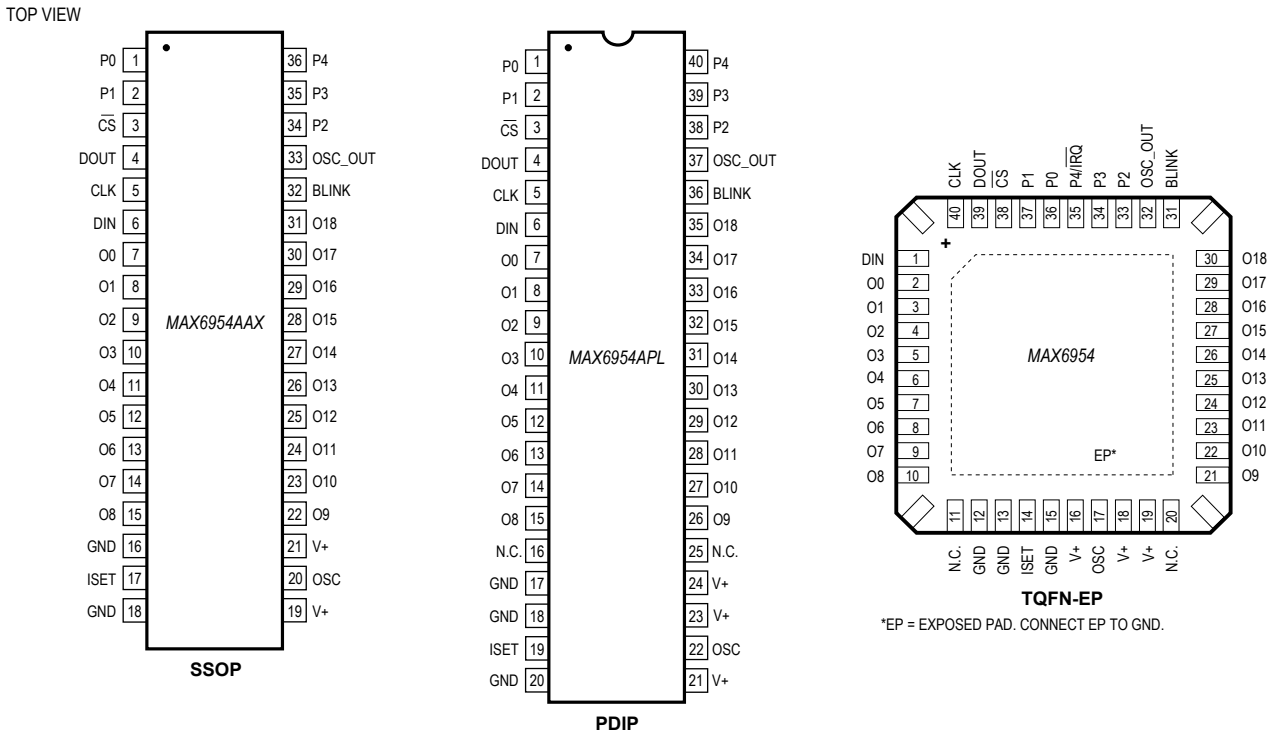
Typical Operating Circuits



Typical Operating Circuits (continued)



Pin Configurations



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
36 SSOP	A36-2	**21-0040**	**90-0098**
40 PDIP	P40-2	**21-0044**	**—**
40 TQFN-EP	T4066+5	**21-0141**	**90-0055**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	6/08	Added TQFN package option	1, 2, 6, 37
4	3/09	Corrected errors in Tables 37–40	31–34
5	7/14	Removed automotive reference from data sheet	1

