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FAIRCHILD SEMICONDUCTOR®

December 2013

FCH47N60

N-Channel SuperFET® MOSFET

600 V, 47 A, 70 mΩ

Features

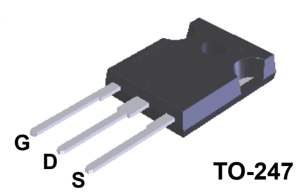
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 58 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 210 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 420 pF)
- 100% Avalanche Tested
- RoHS Compliant

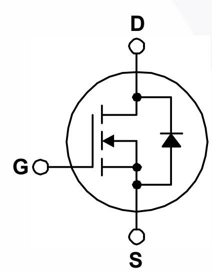
Applications

- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCH47N60_F133	Unit
V_{DSS}	Drain to Source Voltage		600	V
I_D	Drain Current	Continuous (T_C = 25°C)	47	A
		Continuous (T_C = 100°C)	29.7	
I_{DM}	Drain Current	Pulsed (Note 1)	141	A
V_{GSS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1800	mJ
I_{AR}	Avalanche Current (Note 1)		47	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		41.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	417	W
		Derate Above 25°C	3.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCH47N60_F133	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	41.7	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH47N60_F133	FCH47N60	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_C = 25°C	600	-	-	V
		V_{GS} = 0 V, I_D = 250 μA, T_C = 150°C	-	650	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 47 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, T_C = 125°C	-	-	10	μA
I_{GSS}	Gate-to-Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-to-Source On Resistance	V_{GS} = 10 V, I_D = 23.5 A	-	0.058	0.070	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 23.5 A	-	40	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	-	5900	8000	pF
C_{oss}	Output Capacitance		-	3200	4200	pF
C_{rss}	Reverse Transfer Capacitance		-	250	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1.0 MHz	-	160	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	420	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay	V_{DD} = 300 V, I_D = 47 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	-	185	430	ns
t_r	Turn-On Rise Time		-	210	450	ns
$t_{d(off)}$	Turn-Off Delay		-	520	1100	ns
t_f	Turn-Off Fall Time		-	75	160	ns
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 480 V, I_D = 47 A, V_{GS} = 10 V (Note 4)	-	210	270	nC
Q_{gs}	Gate to Source Gate Charge		-	38	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	110	-	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-to-Source Diode Forward Current		-	-	47	A
I_{SM}	Maximum Pulsed Drain-to-Source Diode Forward Current		-	-	141	A
V_{SD}	Drain-to-Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 47 A	-	-	1.4	V
t_{rr}	Reverse-Recovery Time	V_{GS} = 0 V, I_{SD} = 47 A, dI_F/dt = 100 A/μs	-	590	-	ns
Q_{rr}	Reverse-Recovery Charge		-	25	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 18 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 48 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

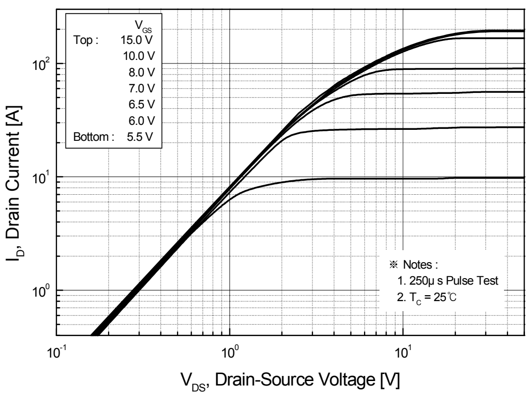


Figure 1. On-Region Characteristics

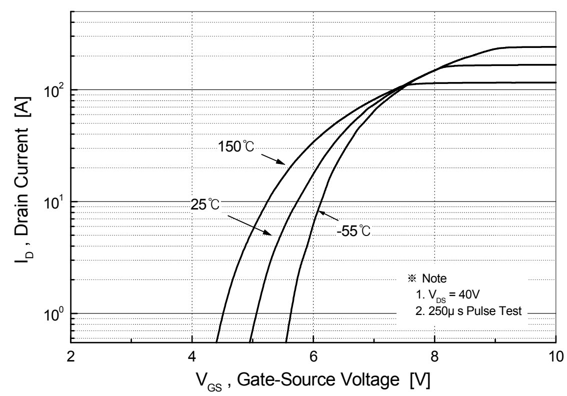


Figure 2. Transfer Characteristics

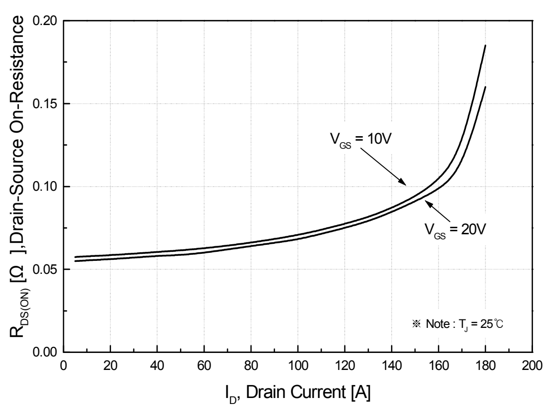


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

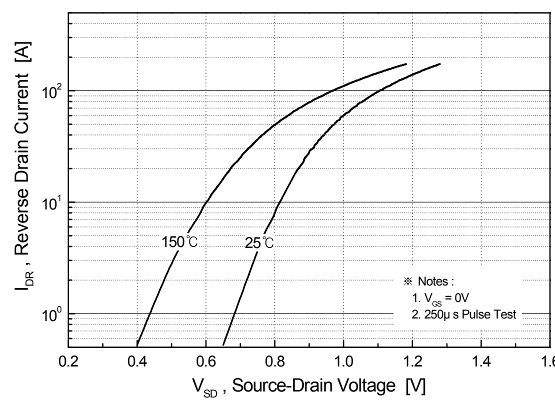


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

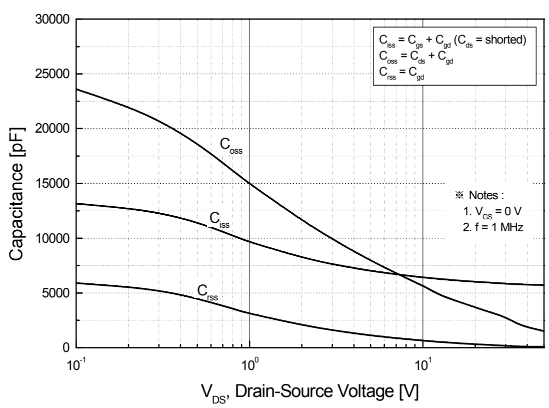


Figure 5. Capacitance Characteristics

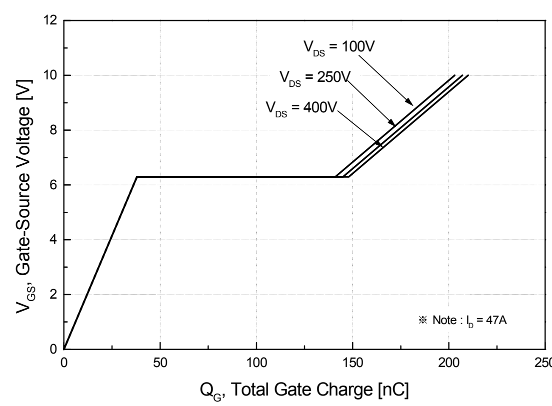


Figure 6. Gate Charge Characteristics

Typical Performance Characteristics (Continued)

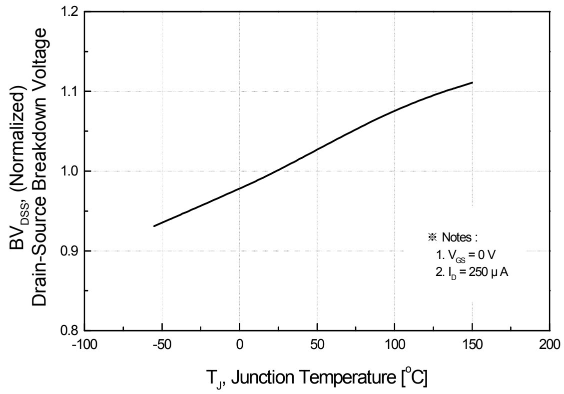


Figure 7. Breakdown Voltage Variation vs. Temperature

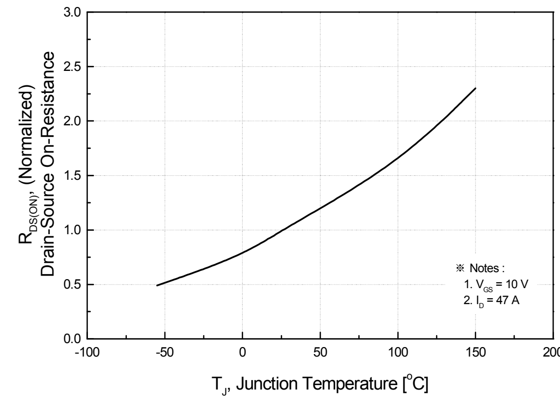


Figure 8. On-Resistance Variation vs. Temperature

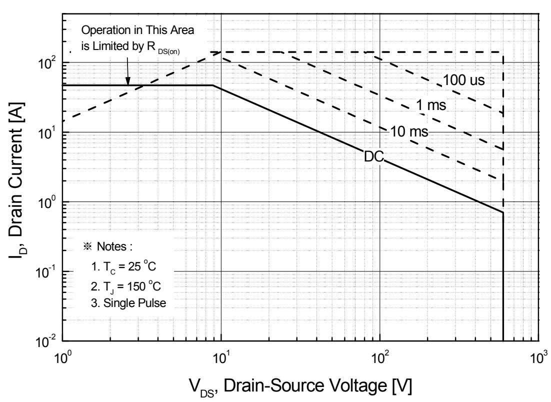


Figure 9. Safe Operating Area

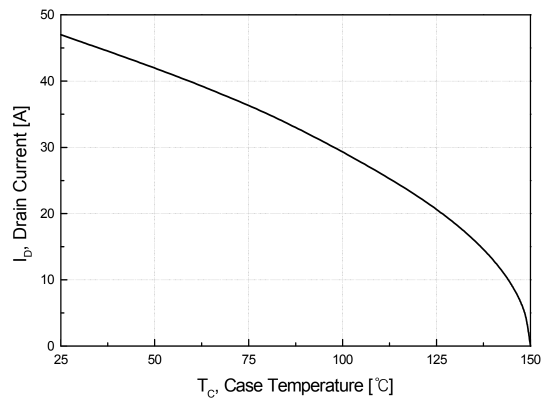


Figure 10. Maximum Drain Current vs. Case Temperature

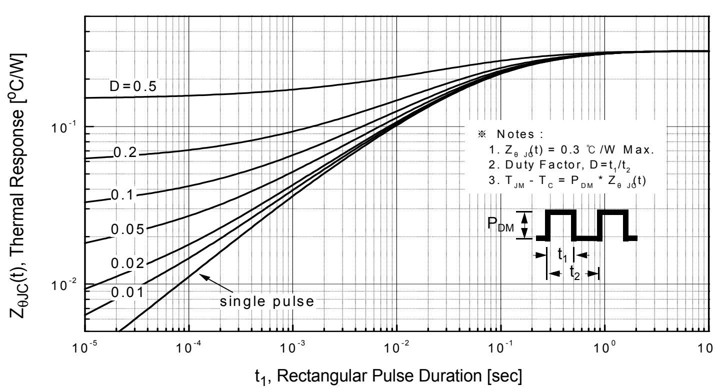


Figure 11. Transient Thermal Response Curve

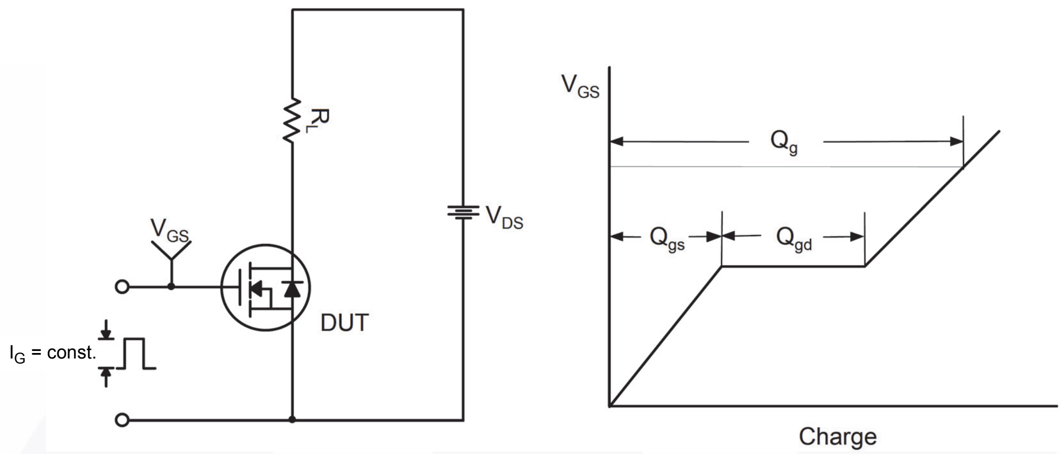


Figure 13. Gate Charge Test Circuit & Waveform

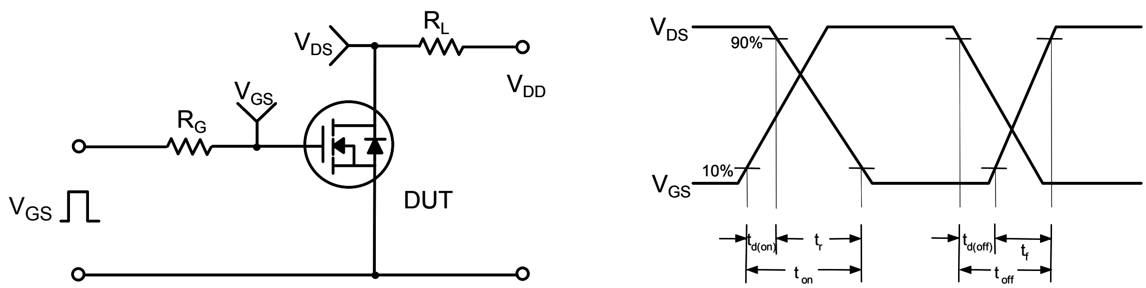


Figure 14. Resistive Switching Test Circuit & Waveforms

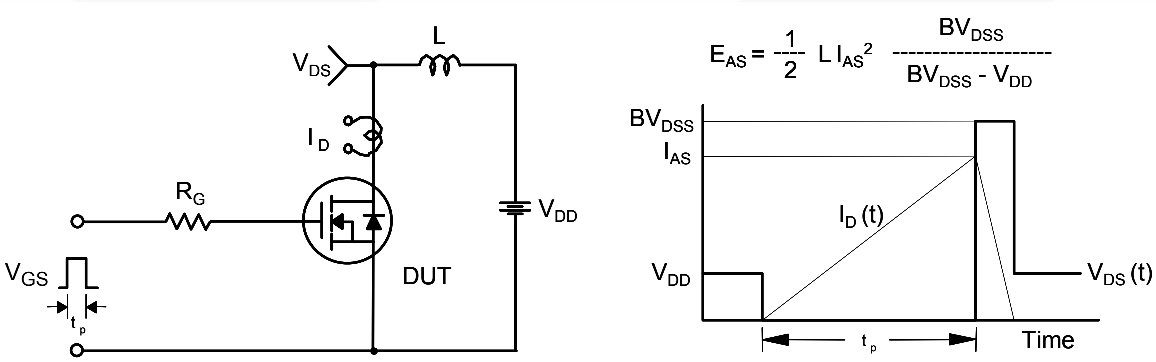


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

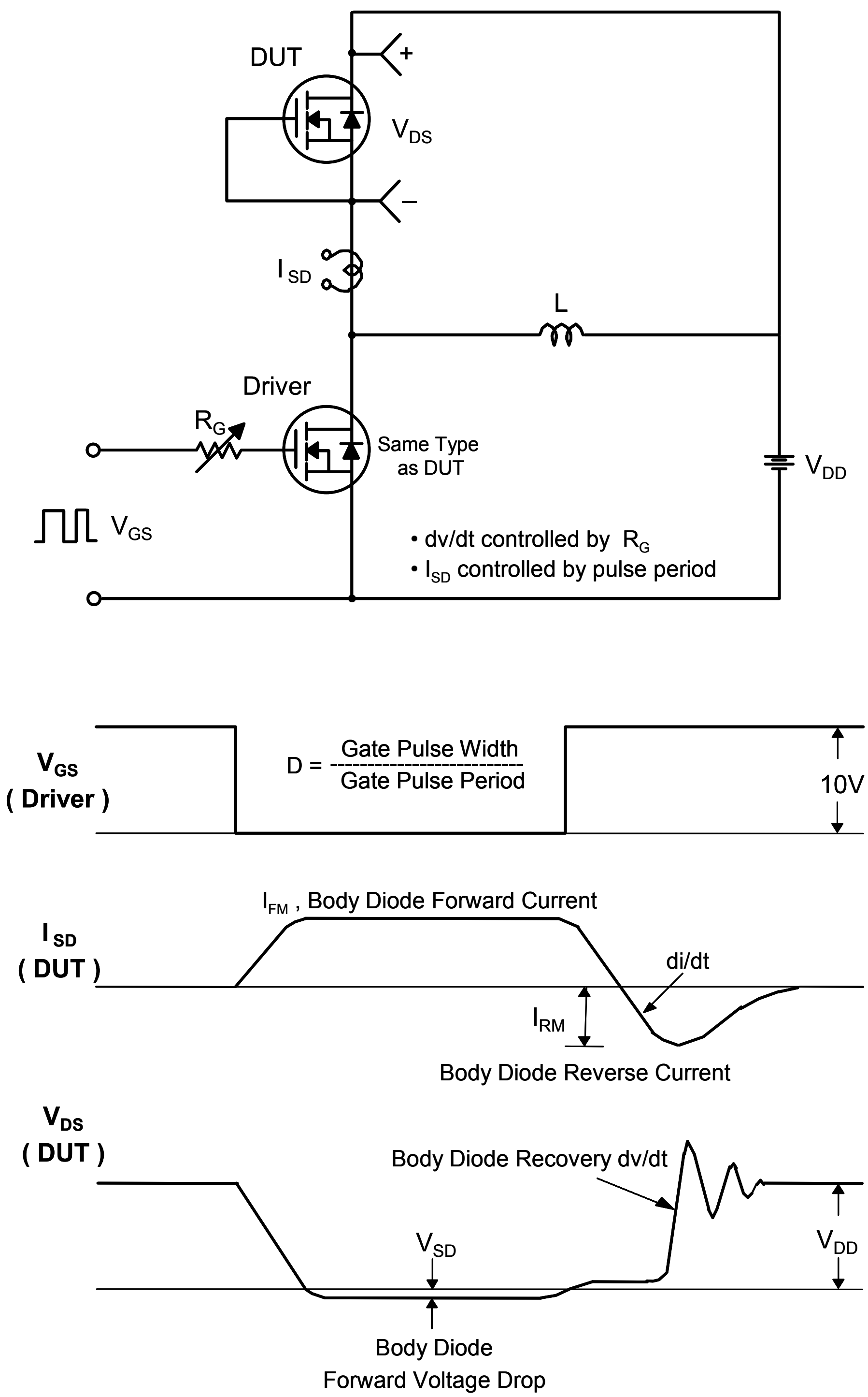


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

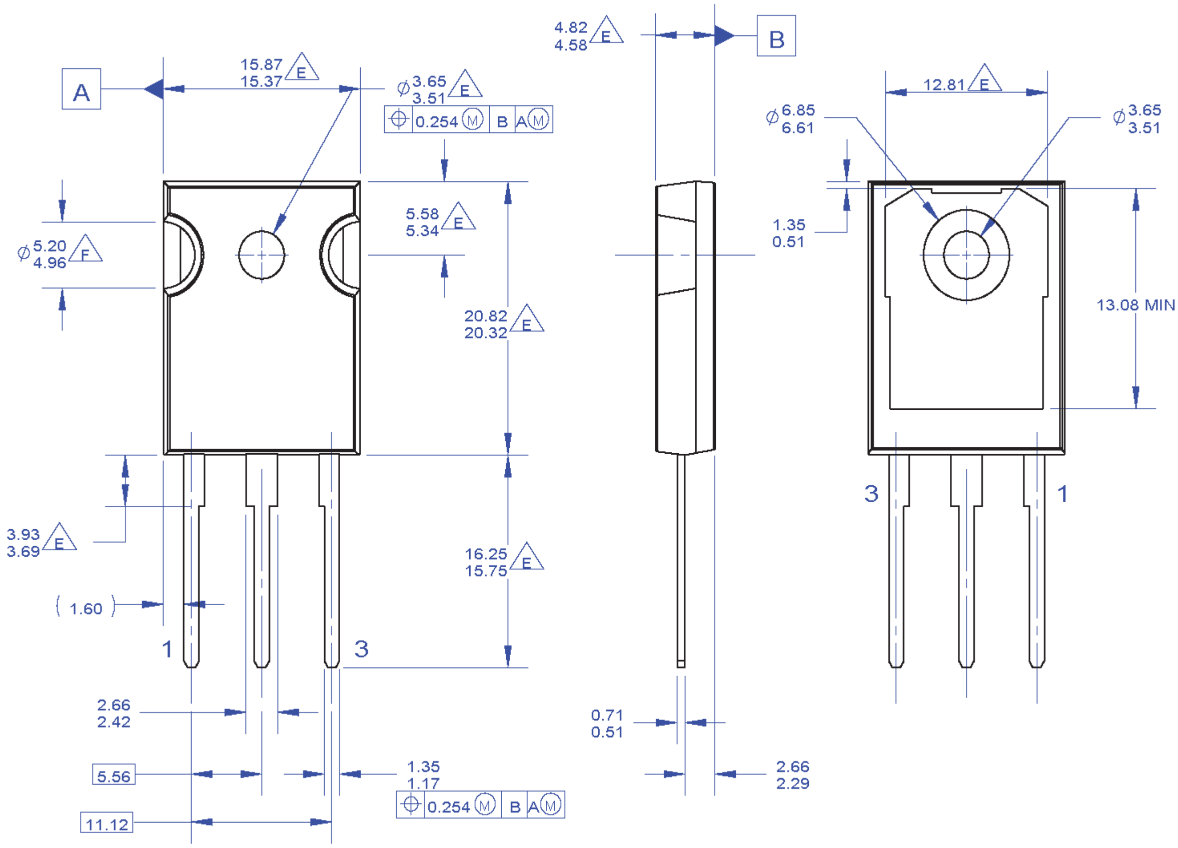


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Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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