

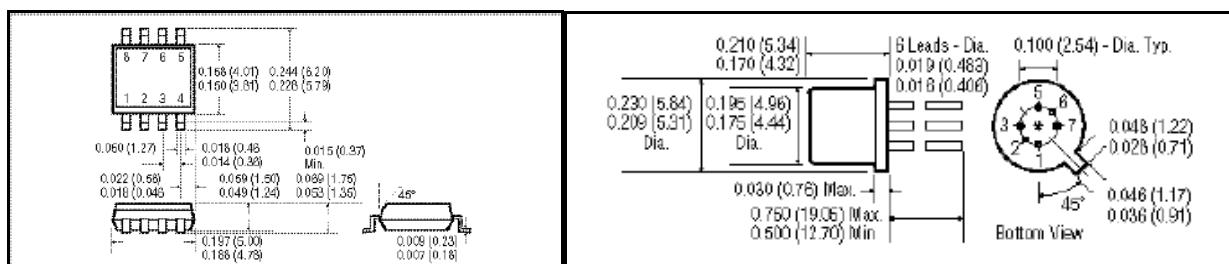
## IFN3954, IFN3955, IFN3956, IFN3957, IFN3958

### N-Channel Matched Dual Silicon Junction Field-Effect Transistor

- Improved Replacement for the 2N3954, 2N3955, 2N3456, 2N3457, & 2N3958
- Differential Inputs

Absolute maximum ratings at $T_A = 25^\circ\text{C}$	
Reverse Gate Source & Gate Drain Voltage	-50V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	250 mW
Power Derating	2.6 mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

At 25°C free air temperature Static Electrical Characteristics	3954, 3955, 3956, 3957, 3958					Process NJ16		
	Min	Typ	Max	Unit	Test Conditions			
Gate Source Breakdown Voltage	$V_{(\text{BR})\text{GSS}}$	-50		V	$I_G = -1 \mu\text{A}, V_{DS} = 0 \text{ V}$			
Gate Reverse Current	$I_{\text{GSS}}$			pA nA	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$		125°C	
Gate Current	$I_G$			pA nA	$V_{DS} = 20 \text{ V}, I_D = 200 \mu\text{A}$		125°C	
Gate Source Cutoff Voltage	$V_{GS(\text{OFF})}$	-1		V	$V_{DS} = 20 \text{ V}, I_G = 1 \text{ nA}$			
Drain Saturation Current (pulsed)	$I_{\text{DSS}}$	0.5		mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			
Gate Source Voltage	$V_{GS}$			V	$V_{DS} = 20 \text{ V}, I_D = 50 \mu\text{A}$ $V_{DS} = 20 \text{ V}, I_D = 200 \mu\text{A}$			
Gate Source Forward Voltage	$V_{GS(F)}$			V	$V_{DS} = 0 \text{ V}, I_G = 1 \text{ mA}$			
Dynamic Electrical Characteristics								
Common-Source Forward Transconductance	$g_{fs}$	1	1	mS	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		1 kHz 200 MHz	
Common-Source Output Conductance	$g_{os}$			$\mu\text{S}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		f = 1 kHz	
Common-Source Input Capacitance	$C_{iss}$			pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		f = 1 MHz	
Common-Source Reverse Transfer Capacitance	$C_{rss}$			pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		f = 1 MHz	
Noise Factor $R_G = 10 \text{ M}\Omega$	NF		0.5	dB	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		f = 1 kHz	
	3954	3955	3956	3957	3958	Unit	Test Conditions	$T_A$
	Max	Max	Max	Max	Max			
Differential Gate-Source Voltage	$ V_{GS1}-V_{GS2} $	5	10	15	20	25	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	
Differential Gate Source Voltage with Temperature	$\Delta  V_{GS1}-V_{GS2} $	0.8 1.0	2 2.5	4 5	6 7	8 10	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	25°C to -55°C 25°C to 125°C
Differential Gate Current	$ I_{G1}-I_{G2} $	10	10	10	10	10	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	125°C
	Min	Min	Min	Min	Min			
Saturation Drain Source Ratio	$I_{\text{DSS1}}/I_{\text{DSS2}}$	0.95	0.95	0.95	0.90	0.85	$V_{DG} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	
Transconductance Ratio	$g_{fs1}/g_{fs2}$	0.97	0.97	0.95	0.90	0.85	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	1 kHz

Dimensions  
in Inches (mm)

#### SOIC-8 Package

SMP3954, SMP3955, SMP3956,  
SMP3957, SMP3958

#### Pin Configuration

1-G1, 2-D1, 3-S1, 4-G2,  
5-G2, 6-D2, 7-S2, 8-G1

#### TO-71:

IFN3954, IFN3955, IFN3956,  
IFN3957, IFN3958

#### Pin Configuration

1-S1, 2-D1, 3-G1,  
4-S2, 5-D2, 6-G2

715 N. Glenville Dr., Ste. 400

Richardson, TX 75081

(972) 238-9700 Fax (972) 238-5338

[www.interfet.com](http://www.interfet.com)