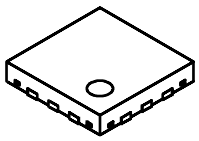
HIGH POWER SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1802K51 is a GaAs SPDT switch MMIC suitable for LTE/UMTS/CDMA/GSM applications. The NJG1802K51 features very low insertion loss, high isolation and excellent linearity performance down to 1.8V control voltage at high frequency up to 2.7GHz. In addition, this switch is able to handle high power signals.

For saving current consumption, the NJG1802K51 has a shutdown mode. The NJG1802K51 has ESD protection devices to achieve excellent ESD performances. No DC Blocking capacitors are required for all RF ports unless DC is biased externally. And the ultra small & ultra thin QFN12-51 package is adopted.

■ PACKAGE OUTLINE



NJG1802K51

■ APPLICATIONS

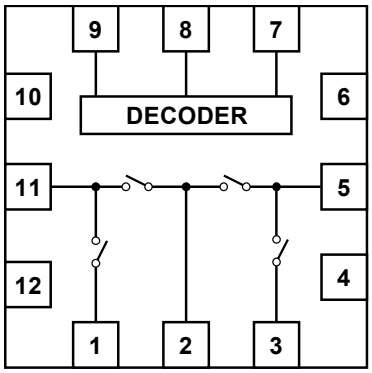
LTE, UMTS, CDMA, GSM applications
Post PA Switching, Antenna Switching and Bands Switching applications
General Purpose Switching applications

■ FEATURES

● Low voltage logic control	$V_{CTL(H)}$=1.8V typ.
● Low voltage operation	V_{DD}=2.7V typ.
● Low distortion	IIP3=+73dBm typ. @f=829+849MHz, P_{IN}=24dBm
	IIP3=+73dBm typ. @f=1870+1910MHz, P_{IN}=24dBm
	2nd/3rd harmonics=-90dBc/ 90dBc typ. @f=0.9GHz, P_{IN}=35dBm
● Linearity	$P_{-0.1dB}$=+36dBm min.
● Low insertion loss	0.18dB/ 0.20dB/ 0.23dB typ. @f=0.9GHz/ 1.9GHz/ 2.7GHz
● Ultra small & ultra thin package	QFN12-51 (Package size: 2.0 x 2.0 x 0.375mm.)
● RoHS compliant and Halogen Free, MSL1	

■ PIN CONFIGURATION

(TOP VIEW)



Pin connection

1. GND	7. VCTL1
2. PC	8. VCTL2
3. GND	9. VDD
4. NC (GND)	10. GND
5. P1	11. P2
6. NC (GND)	12. NC (GND)

Exposed PAD: GND

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

VCTL1	VCTL2	Path
Don't care	L	Shutdown
H	H	PC-P2
L	H	PC-P1

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V, on-state ports	37	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (101.5x114.5mm), T_j=150°C	1190	mW
Operating Temp.	T_{opr}		-40~+85	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: T_a=+25°C, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD Terminal	2.5	2.7	5.0	V
Operating Current	I_{DD}	No RF input, V_{DD}=2.7V	-	100	200	μA
Shutdown Current	I_{OFF}	Shutdown mode	-	8	20	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1, VCTL2 Terminal	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1, VCTL2 Terminal	1.35	1.8	5.0	V
Control Current	I_{CTL}	$V_{CTL(H)}$=1.8V	-	4	10	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF)

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=0.9GHz, P_{IN}=35dBm	-	0.18	0.33	dB
Insertion Loss 2	LOSS2	f=1.9GHz, P_{IN}=33dBm	-	0.20	0.40	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=27dBm	-	0.23	0.43	dB
Isolation 1	ISL1	f=0.9GHz, P_{IN}=35dBm	45	50	-	dB
Isolation 2	ISL2	f=1.9GHz, P_{IN}=33dBm	33	38	-	dB
Isolation 3	ISL3	f=2.7GHz, P_{IN}=27dBm	28	33	-	dB
Input Power at 0.1dB Compression Point	$P_{-0.1dB}$	f=0.9GHz, 1.9GHz, 2.7GHz	36	-	-	dBm
2nd Harmonics 1	2fo(1)	f=0.9GHz, P_{IN}=35dBm	-	-90	-70	dBc
2nd Harmonics 2	2fo(2)	f=1.9GHz, P_{IN}=33dBm	-	-100	-70	dBc
2nd Harmonics 3	2fo(3)	f=2.7GHz, P_{IN}=27dBm	-	-100	-70	dBc
3rd Harmonics 1	3fo(1)	f=0.9GHz, P_{IN}=35dBm	-	-90	-70	dBc
3rd Harmonics 2	3fo(2)	f=1.9GHz, P_{IN}=33dBm	-	-85	-70	dBc
3rd Harmonics 3	3fo(3)	f=2.7GHz, P_{IN}=27dBm	-	-90	-70	dBc
Input 3rd order intercept point1	IIP3(1)	f=829+849MHz, P_{IN}=24dBm each	+65	+73	-	dBm
Input 3rd order intercept point2	IIP3(2)	f=1870+1910MHz, P_{IN}=24dBm each	+65	+73	-	dBm
VSWR	VSWR	on-state ports, f=2.7GHz	-	1.1	1.4	
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF	-	1	5	μs
Wake Up Time	T_{WK}	Shutdown state to any RF switch state	-	-	20	μs

*1: IIP3 are defined by the following equations.
IIP3=(3 x Pout-IM3)/2+LOSS

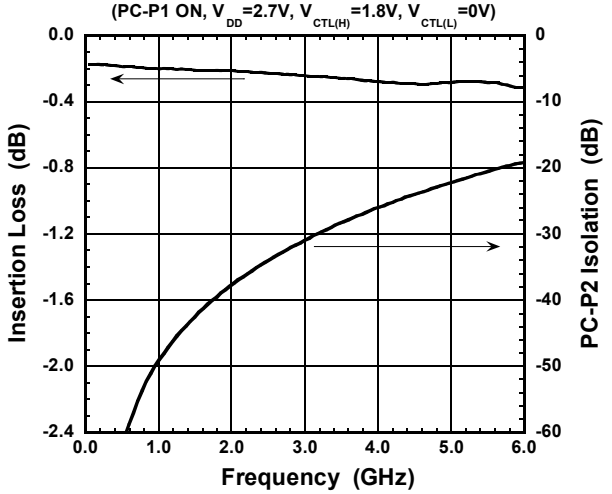
■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
2	PC	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally. Please connect an inductor with GND terminal for ESD protection.
3	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
4	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.
5	P1	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally.
6	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.
7	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).
8	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35~+5.0V) or Low-Level (0~+0.45V).
9	VDD	Positive voltage supply terminal. The positive voltage (+2.5~+5V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	P2	RF transmitting/receiving port. No DC blocking capacitor is required for this port unless DC is biased externally.
12	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.
Exposed Pad	GND	Ground terminal. Please connect Exposed Pad with ground plane as close as possible for excellent RF performance.

■ ELECTRICAL CHARACTERISTICS

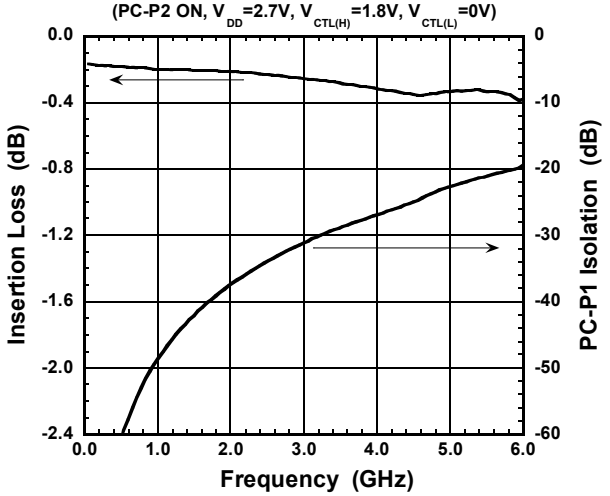
Loss, ISL vs Frequency

(PC-P1 ON, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



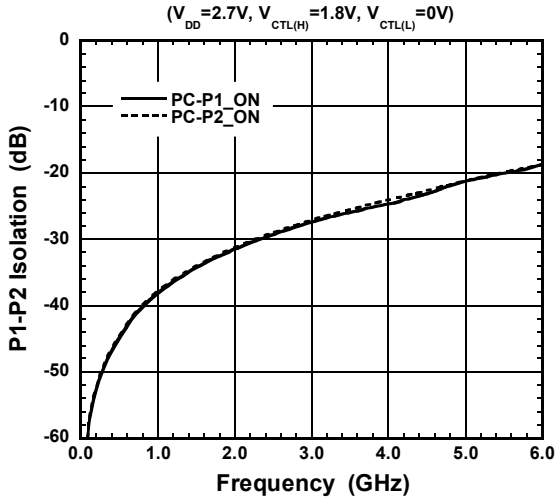
Loss, ISL vs Frequency

(PC-P2 ON, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



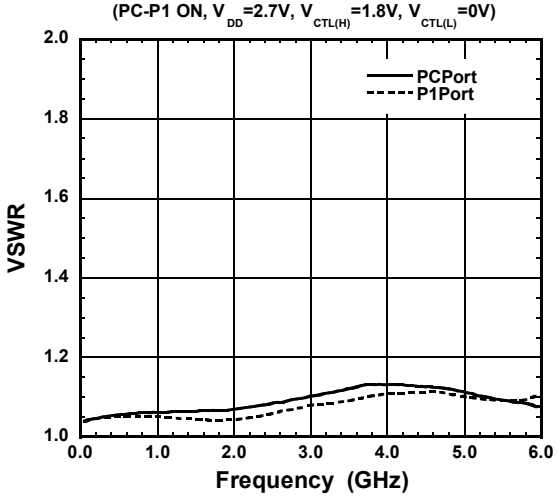
ISL vs Frequency

(V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



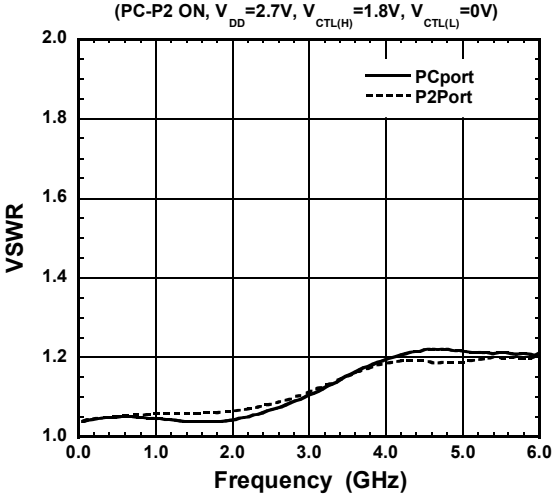
VSWR vs Frequency

(PC-P1 ON, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



VSWR vs Frequency

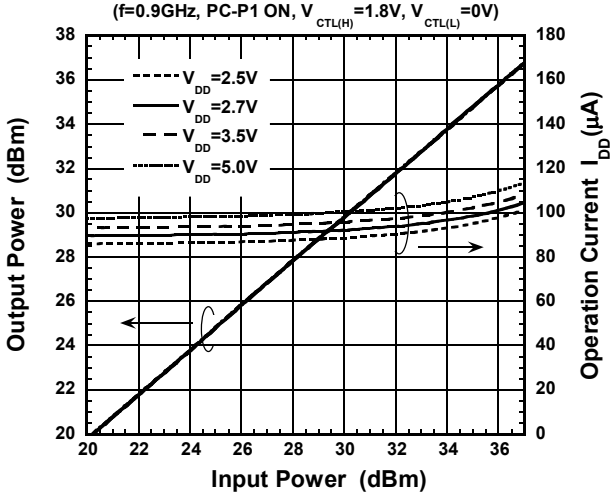
(PC-P2 ON, V_{DD}=2.7V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



■ ELECTRICAL CHARACTERISTICS

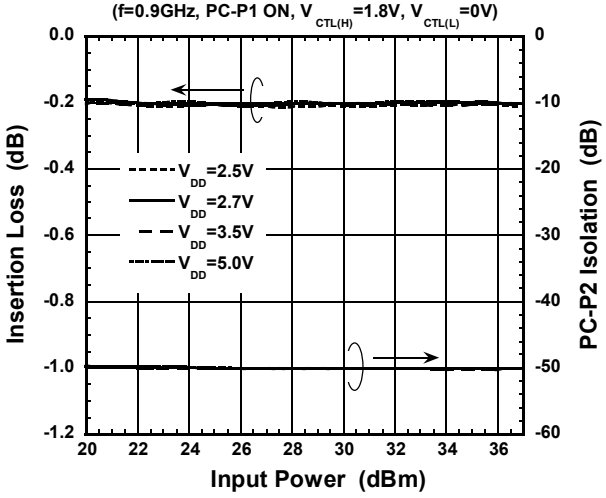
Output Power, I_{DD} vs Input Power

(f=0.9GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



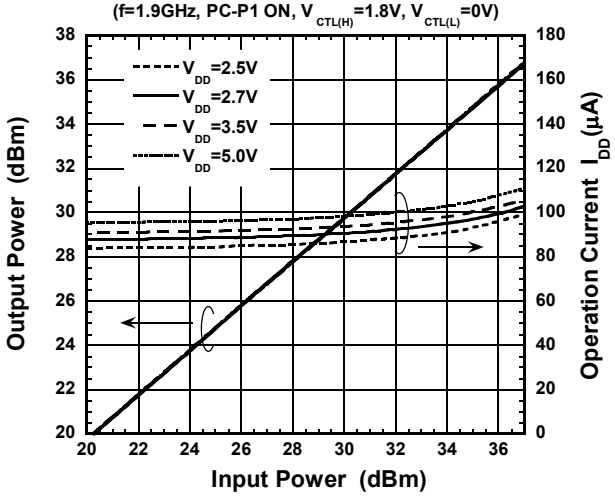
Loss, ISL vs Input Power

(f=0.9GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



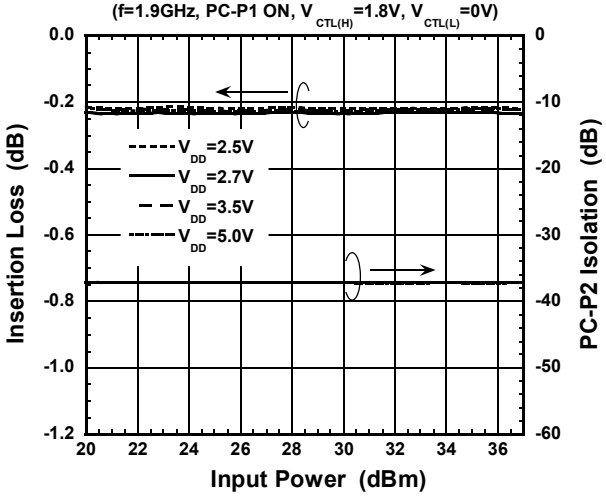
Output Power, I_{DD} vs Input Power

(f=1.9GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



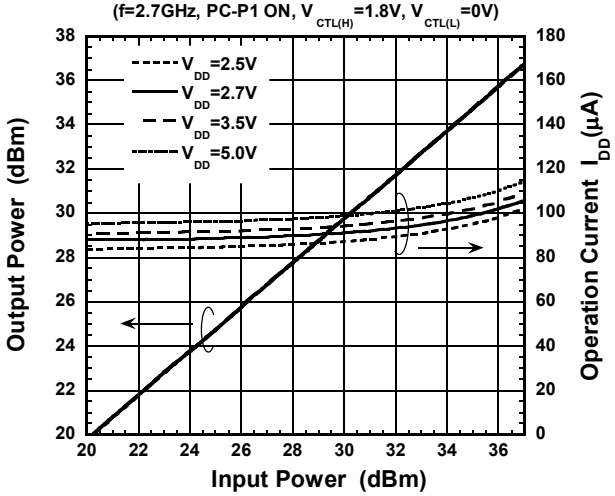
Loss, ISL vs Input Power

(f=1.9GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



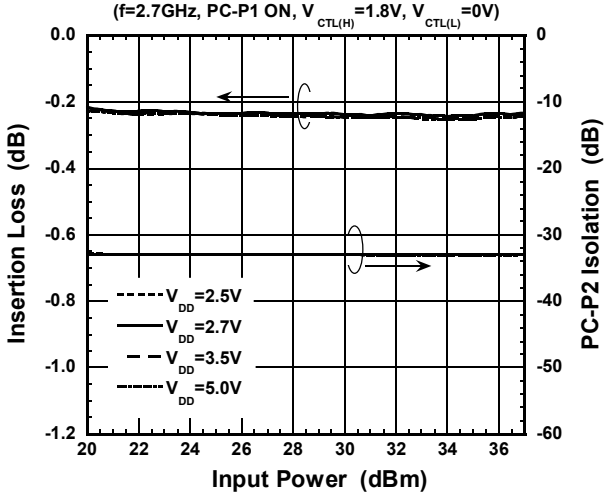
Output Power, I_{DD} vs Input Power

(f=2.7GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



Loss, ISL vs Input Power

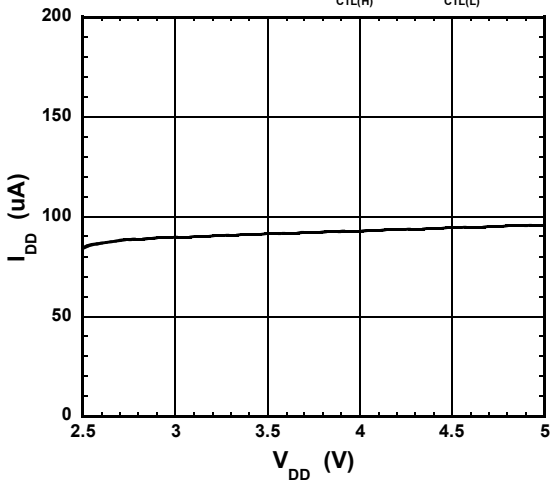
(f=2.7GHz, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



■ ELECTRICAL CHARACTERISTICS

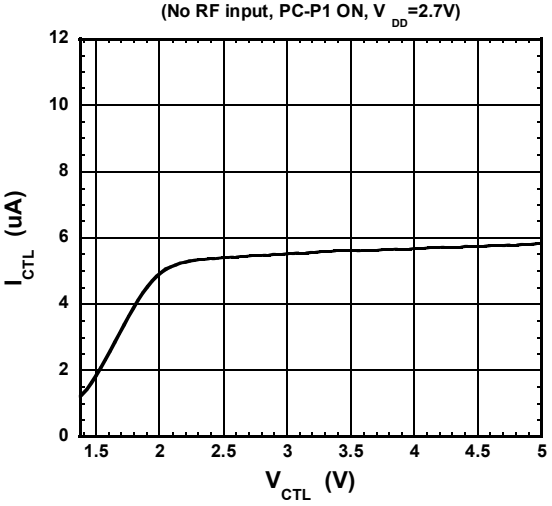
I_{DD} vs V_{DD}

(No RF input, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



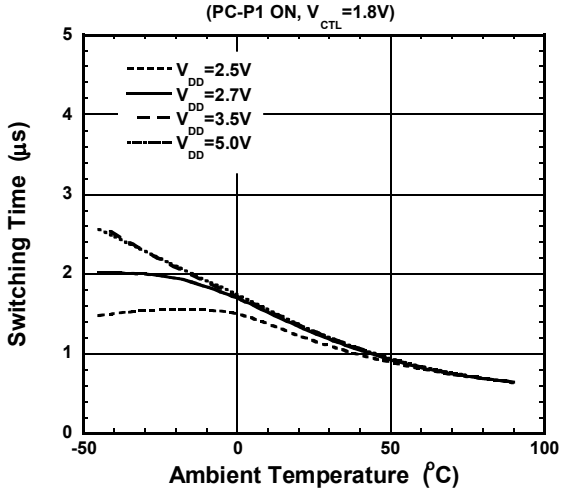
I_{CTL} vs V_{CTL}

(No RF input, PC-P1 ON, V_{DD}=2.7V)



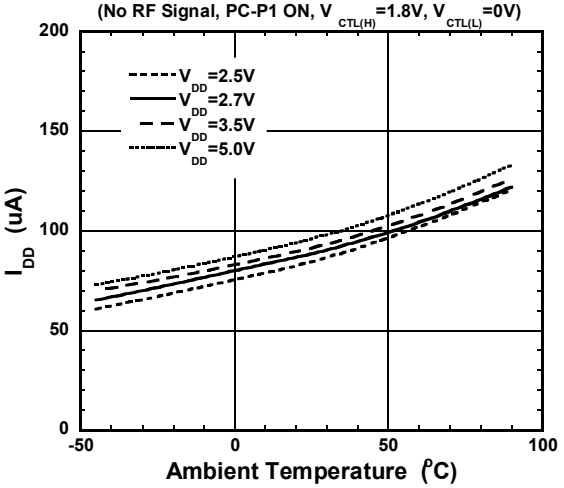
Switching Time vs Ambient Temperature

(PC-P1 ON, V_{CTL}=1.8V)



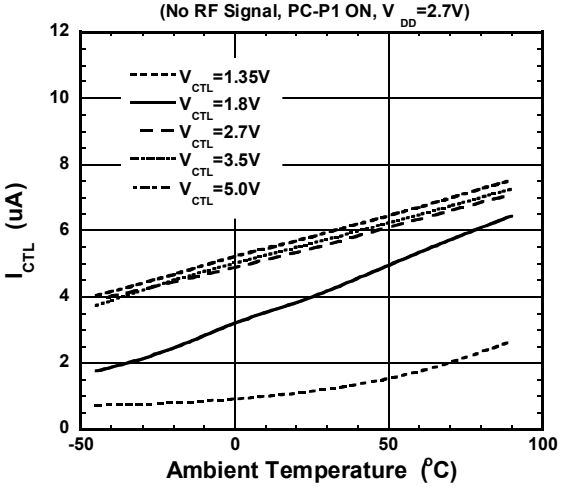
I_{DD} vs Ambient Temperature

(No RF Signal, PC-P1 ON, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V)



I_{CTL} vs Ambient Temperature

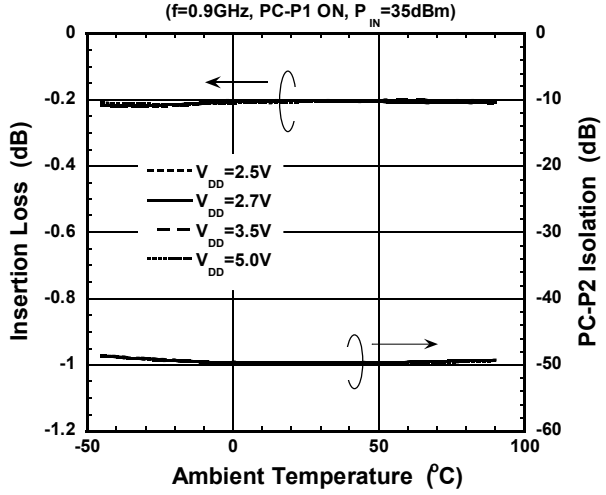
(No RF Signal, PC-P1 ON, V_{DD}=2.7V)



■ ELECTRICAL CHARACTERISTICS

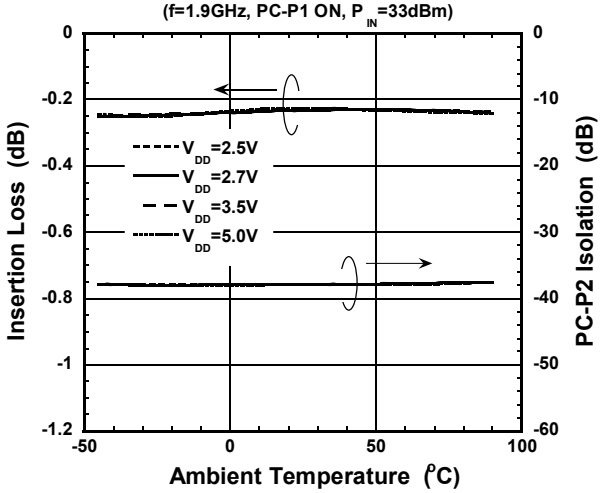
Loss, ISL vs Ambient Temperature

(f=0.9GHz, PC-P1 ON, P_{IN}=35dBm)



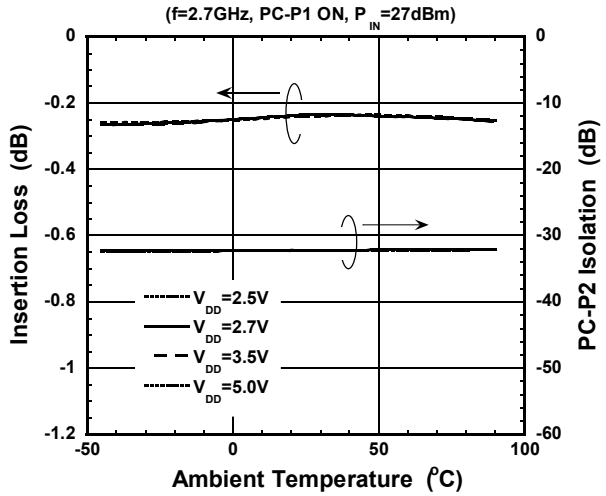
Loss, ISL vs Ambient Temperature

(f=1.9GHz, PC-P1 ON, P_{IN}=33dBm)



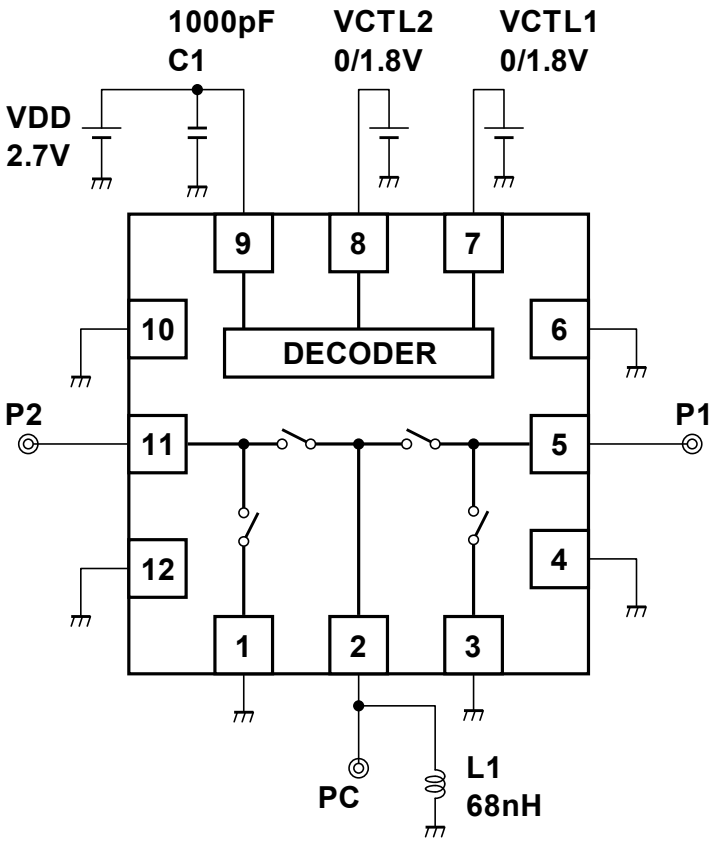
Loss, ISL vs Ambient Temperature

(f=2.7GHz, PC-P1 ON, P_{IN}=27dBm)



■ APPLICATION CIRCUIT

(TOP VIEW)



No DC blocking capacitors are required on all RF ports, unless DC is biased externally.

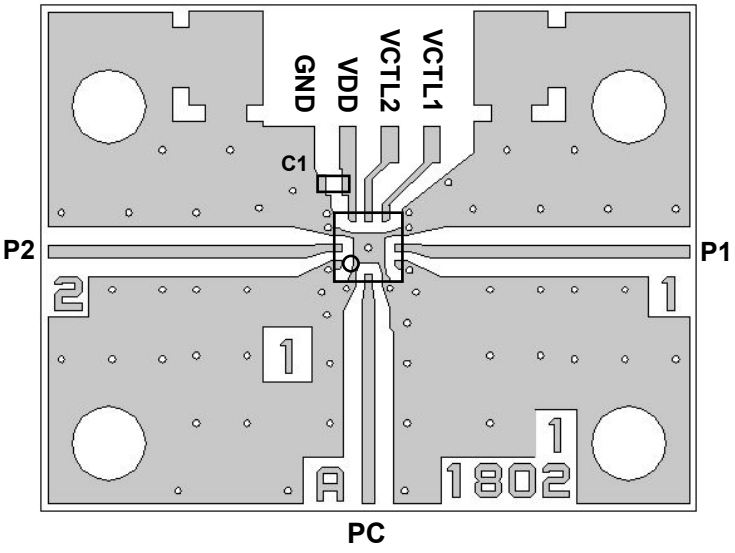
* The Inductor L1 is required for enhancing ESD protection level.
  The inductor L1 is recommended in order to keep the DC bias level of each RF port at 0 V level tightly.

■ PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)
L1	68nH	TAIYO-YUDEN (HK1005)

■ PCB LAYOUT

(TOP VIEW)



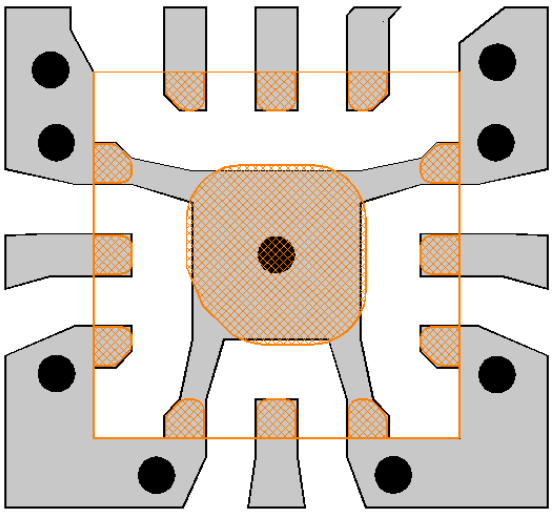
PCB SIZE: 19.4 x 15.0 mm
PCB: FR-4, t=0.2mm
Capacitor size: 1005
MICROSTRIP LINE WIDTH: 0.38mm

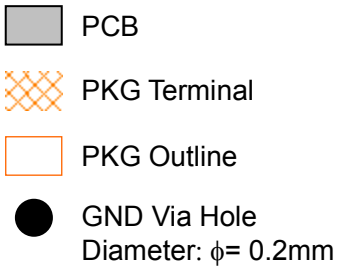
Losses of PCB and connectors, Ta=+25°C

Frequency (GHz)	Loss (dB)
0.9	0.15
1.9	0.25
2.7	0.32

■ PCB LAYOUT (QFN12-51)

(TOP VIEW)





■ PCB LAYOUT PRECAUTIONS

[1] No DC blocking capacitors are required at each RF port normally. When the other device is biased at certain voltage and connected to the NJG1802K51, a DC block capacitor is required between the device and the switch IC. This is because the each RF port of NJG1802K51 is biased at 0 V (GND).
[2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal
[3] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through - holes for GND should be placed the IC near.
[4] Please connect Exposed PAD to PCB ground plane of substrate, and through - holes for GND should be placed under the IC.

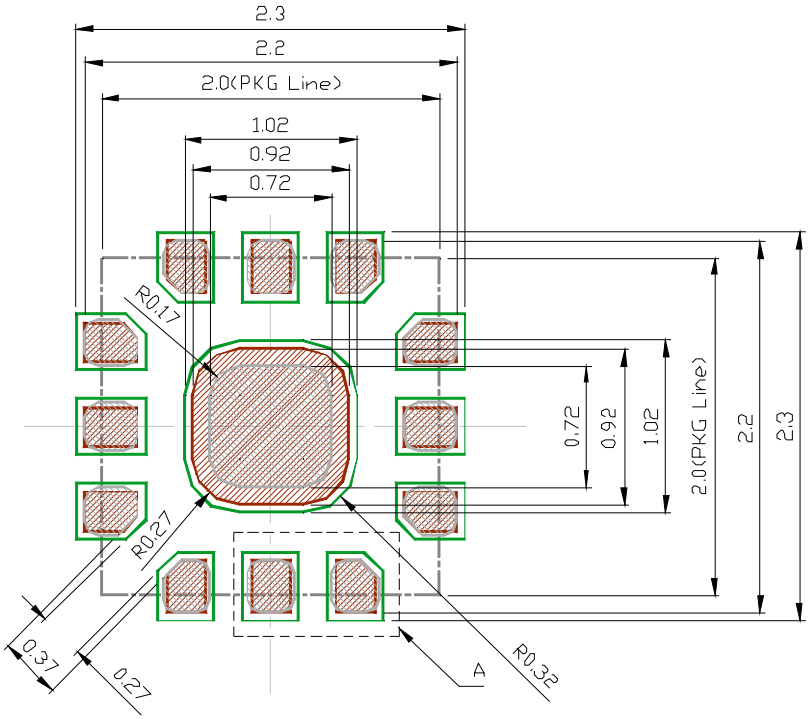
■ RECOMMENDED FOOTPRINT PATTERN (QFN12-51 PACKAGE Reference)

PKG: 2.0mm x 2.0mm
Pin pitch: 0.5mm

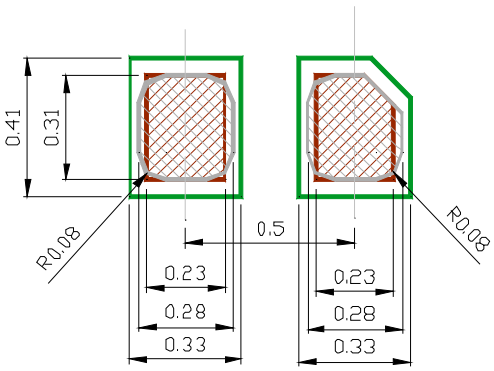
: Land

: Mask (Open area) *Metal mask thickness: 100um

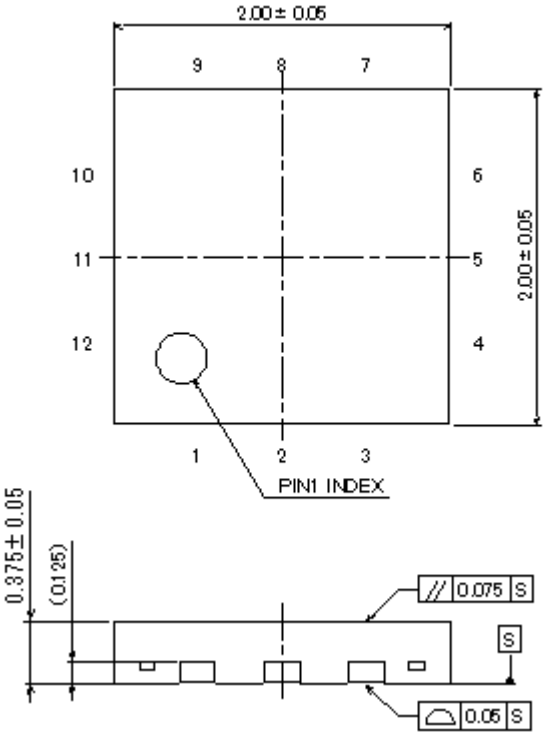
: Resist (Open area)



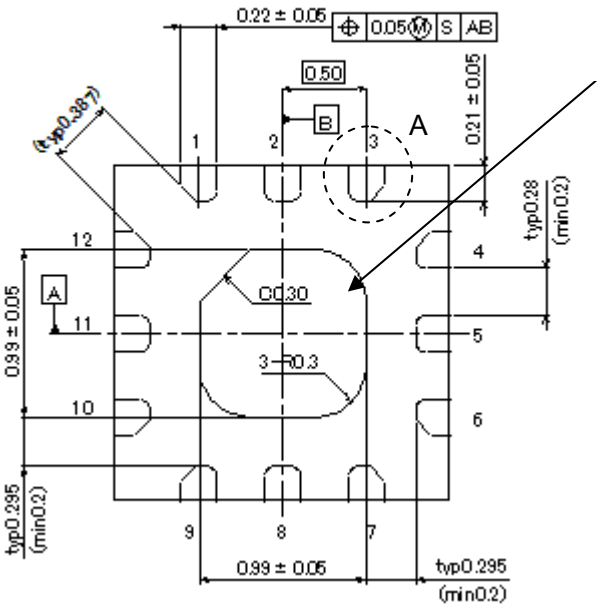
Detail A



■ PACKAGE OUTLINE (QFN12-51)

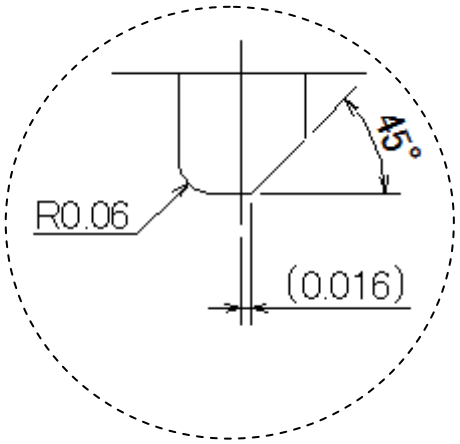


Unit	: mm
Board	: Copper
Terminal Treat	: Ni/Pd/Au
Molding Material	: Epoxy resin
Weight	: 4.7mg



Exposed PAD
Ground connection is required.

Details of “A” part



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NJR:

NJG1802K51 NJG1802K51-TE1