MP4601

White LED Driver For Large Size TV Backlighting

The Future of Analog IC Technology

DESCRIPTION

The MP4601 is an integrated white LED driver. It can be applied with MPS patent pending technology to drive up to 60 inch or larger size LCD TV backlighting, in which the LED string voltage can be up to 350V. The novel technology can leverage the LED drive power by regulating only small portion of the LED drive voltage. As a result, working together with a fixed high voltage source, a low voltage LED driver can be used to drive the high voltage LED strings with super high power density, high efficiency and low cost due to the low voltage stress, high switching frequency, and smaller size of passive components.

MP4601 is a current mode controlled buck-boost regulator. With a 12V input V_{INL} and a high voltage source V_{INH}, it can deliver a regulated voltage (V_{INH} to V_{INH}+63V) to drive a LED string with up to 100 LEDs. It can drive an external switch, which is in series with the LED string, to achieve over 1:1000 dimming ratio. Analog dimming can be applied in the same time to further improve the dimming ratio. Fault protection includes LED open strings protection, output short circuit protection, cycle-by-cycle peak current limiting, and thermal shutdown.

MP4601 is available in TSSOP16-EP and SOIC16 packages.

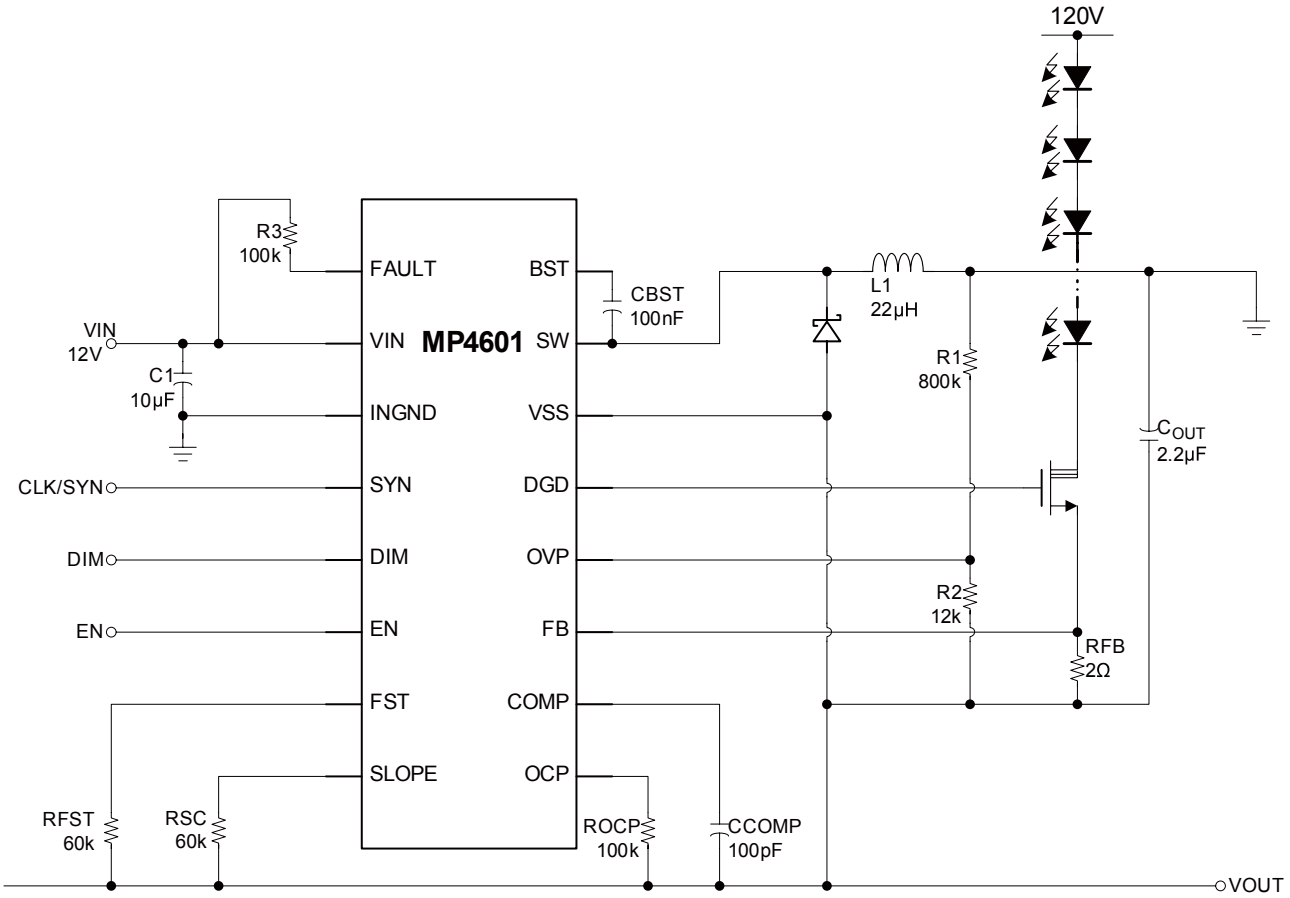
FEATURES

- Novel Power Leverage Control Technology
- Unique Step-up/down Operation
- Up to 99.5% Efficiency
- 0.5Ω Internal Power MOSFET Switch
- Switching Frequency Synchronization
- Over 1:1000 Dimming Ratio
- Analog and PWM Dimming
- ±5% 200mV Reference Voltage
- 850μA Quiescent Current
- 10μA Shutdown Mode
- Programmable Cycle-by-Cycle Over Current Protection
- Thermal Shutdown Protection
- LED String Open and Short Protection
- FAULT Output for Short LED Protection
- Output Short Circuit Protection
- Available in TSSOP16-EP and SOIC16 Packages

APPLICATIONS

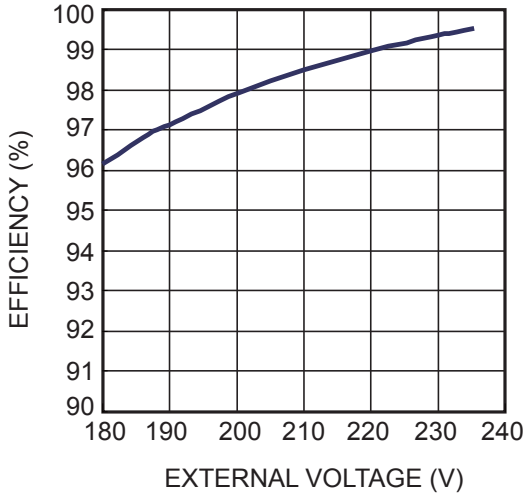
- TV Backlighting
- Large LCD Panels Backlighting

TYPICAL APPLICATION



Efficiency vs.
External Bus Voltage

V_{INL}=12V, V_{LED}=240V, I_{LED}=100mA,
External bus voltage, V_{INH}=180~236V

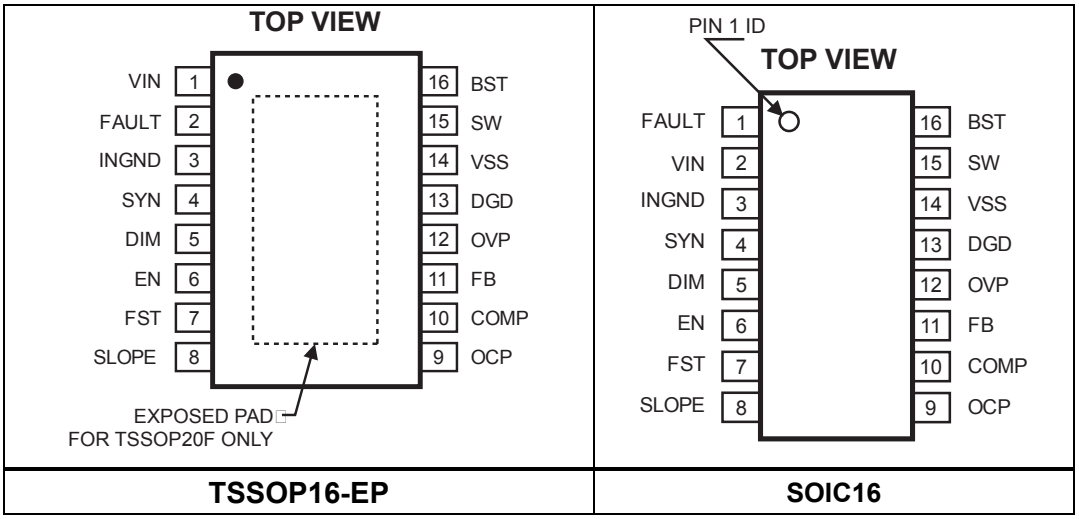


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP4601EF*	TSSOP16-EP	MP4601EF	-20°C to +85°C
MP4601ES	SOIC16	MP4601ES	

* For Tape & Reel, add suffix –Z (e.g. MP4601EF–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP4601EF–LF–Z)

PACKAGE REFERENCE



TSSOP16-EP	SOIC16

ABSOLUTE MAXIMUM RATINGS (1)

V_{VIN} – V_{SS} .....-0.3V to 85V
V_{INGND} – V_{SS}.....-0.3V to 85V
V_{SW} – V_{SS} ..... -0.3V to V_{VIN} + 0.3V
V_{BST} ..... V_{SW} + 6V
V_{DGD} – V_{SS} .....-0.3V to +12V
V_{SLOPE}, V_{OCP} – V_{SS} .....-0.3V to +6V
V_{OVP}, V_{FB}, V_{COM}, V_{FST} – V_{SS} .....-0.3V to +6V
V_{FAULT}, V_{DIM}, V_{SYN}, V_{EN} – V_{INGND} .....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
TSSOP16-EP..... 2.7W
SOIC16 ..... 1.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{VIN} – V_{SS} .....4.5V to 75V
V_{DIM}, V_{EN}, V_{SYN} – V_{INGND}.....0V to 5V
Operating Junct. Temp (T_J)..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP16-EP	45	10...	°C/W
SOIC16	80	30...	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device function is not guaranteed outside of the recommended operating conditions.
4) Measured on JESD5 1-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{VIN} = 12V, PWM and AD Pins floating, R_{FST}=51kΩ, T_A = +25°C, V_{VSS}=V_{INGND}=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
FB Feedback Voltage	V_{FB}		190	200	210	mV
FB Input Current	I_{FB}	V_{FB} = 0.2V	-0.1		0.1	μA
VIN UVLO Rising	V_{VINTH}		2.7	3.5	4.1	V
VIN UVLO Hysteresis	V_{VINHYS}			70		mV
Shut Down Current	I_{off}	V_{EN}=0V		10		μA
Supply Current (Quiescent)	I_Q	V_{PWM} = 0V, V_{FB} = 250mV		850	1000	μA
Switch-On Resistance	$R_{DS(ON)}$			0.5		Ω
Switch Leakage	I_{SWLK}	V_{VIN}=80V, V_{EN}=0V, V_{PWM}=0V, V_{SW}=0V			10	μA
Switch Current Limit	I_{S_MAX}	OCP pin open		2.5		A
OCP Output Voltage	V_{OCP}		1.1	1.2	1.3	V
Oscillator Frequency	f_{SW}	FST pin open	0.8	0.95	1.2	MHz
		RFST = 200kΩ	200	280	390	kHz
FST Output Voltage	V_{FST}		1	1.1	1.2	V
Fold-back Frequency	f_{SWFB}	V_{FB} = V_{OVP} = 0V, FST pin open		160		kHz
		V_{FB} = V_{OVP} = 0V, RFST = 200kΩ		36		
Slope Compensation	S_{SLOPE}	SLOPE pin open	1	1.2	1.4	V/μs
		R_{SLOPE} = 200kΩ	0.3	0.39	0.47	
SLOPE Pin Output Voltage	V_{SLOPE}		1	1.1	1.2	V
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.15V,FST pin open		95		%
Minimum On-Time	t_{ON}			100		ns
SYN Input Current	I_{SYN}	V_{SYN} = 3.3V		400		μA
		V_{SYN} = 0V		-700		
Frequency Synchronization Range (5)	f_{SW_SYN}	R_{FST}>620kΩ	0.1		2	MHz
PWM Dimming OFF Threshold	V_{DIML}	V_{DIM} Falling	0.6			V
PWM Dimming ON Threshold	V_{DIMH}	V_{DIM} Rising			1.7	V
DIM Input Current		V_{DIM} = 3.3V		36		μA
		V_{DIM} = 0V		-3.5		
PWM Dimming Frequency			100		50k	Hz
Minimum Analog Dimming Threshold	V_{ADMIN}	V_{FB} = 5mV		0.7		V
Maximum Analog Dimming Threshold	V_{ADMAX}	V_{FB} = 200mV		1.5		V
EN OFF Threshold	V_{ENL}	V_{EN} Falling	0.6			V
EN ON Threshold	V_{ENH}	V_{EN} Rising			1.7	V
EN Input Current	I_{EN}	V_{EN} = 3.3V		3.8		μA
Dim Gate Driver Sourcing Current	I_{DGD+}	V_{DGD}-V_{SS}=10V, V_{DIM}=0V		-25		mA
Dim Gate Driver Sinking Current	I_{DGD-}	V_{DGD}-V_{SS}=0V V_{DIM}=2V		45		mA

ELECTRICAL CHARACTERISTICS (*continued*)

V_{VIN} = 12V, PWM and AD Pins floating, R_{FST}=51kΩ, T_A = +25°C, V_{VSS}=V_{INGND}=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LED Open OV Threshold	V_{OVPTH}			1.2		V
LED Open OV Hysteresis	V_{OVPHYS}			0.1		V
LED Short Threshold for Immediate Latch-off	V_{FBS}			600		mV
LED Short Delay for Latch-off	T_{D_FBS}	300mV < V_{FBS} < 600mV		480		µs
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				20		°C

Note:
5) Guaranteed by design.

PIN FUNCTIONS

Pin # SOIC16	Pin # TSSOP 16-EP	Name	Description
2	1	VIN	Positive Voltage Input Pin. A decoupling cap is needed to prevent large voltage spikes from appearing at the input.
1	2	FAULT	Fault condition output, open drain with reference to INGND. FAULT is high-Z during normal operation, and pulled to INGND when short LED protection is triggered.
3	3	INGND	Input Ground Reference. This pin is the reference for the EN/DIM signal.
4	4	SYN	Frequency Synchronization Input Pin. The switching frequency can be synchronized with an external clock, which frequency is higher than the set frequency with FST resistor. Multiple ICs' frequencies can also be synchronized without the external clock by connecting all SYN pins together. They follow the highest set frequency.
5	5	DIM	PWM Dimming and Analog Dimming Input Pin. For digital dimming, apply a 100Hz to 50kHz square wave signal with amplitude greater than 1.5V to DIM pin. For analog dimming, apply a voltage between 0.7V and 1.5V to DIM pin. When DIM voltage changes from 0.7V to 1.5V, the internal reference for FB regulation changes from 0 to 200mV. A voltage higher than 1.5V at this pin doesn't modify the internal reference anymore. For combined PWM and analog dimming to get a further high dimming ratio, apply a 100Hz to 50kHz square wave signal with amplitude from 0.7V to 1.5V to DIM pin. DIM pin voltage is high (about 3.3V) if it is floating.
6	6	EN	Enable Input Pin. A voltage greater than 0.6V will turn on the chip.
7	7	FST	Frequency Setting Pin. A resistor from FST to VSS setting the switching frequency if there is no SYN input. If left open, switching frequency will be set to internal default value.
8	8	SLOPE	Programmable Slope Compensation pin. Connect a resistor from SLOPE pin to VSS sets slope compensation peak amplitude. If left open, slope compensation will be set internal default value.
9	9	OCP	Over Current Protection Pin. Connect a resistor R_{OCP} from OCP pin to VSS sets the cycle-by-cycle current limit of the inside power FET. If left open, the current limit is the default value of 2.5A.
10	10	COMP	Output of error amplifier. Connect a 1nF or larger capacitor on COMP pin to VSS to improve the stability and to provide a soft on at start up or PWM dimming.
11	11	FB	LED Current Feedback Input. MP4601 regulates the voltage across the current sensing resistor between FB and VSS with 200mV. If FB voltage is higher than 300mV for 480us or FB voltage is higher than 600mV, it triggers the LED short protection.
12	12	OVP	Over Voltage Protection Pin. Use one external resistor voltage divider across INGND and VSS to program OVP threshold. Its voltage is referred to VSS. When the OVP pin voltage reaches 1.2V threshold, the switch is turned off and will recover when OVP voltage decreases below 1.1V. When the OVP pin voltage is lower than 0.4V and FB pin voltage is lower than 0.1V, the chip frequency will be folded back. Program the OVP pin voltage from 0.4V to 1.2V for normal operation.

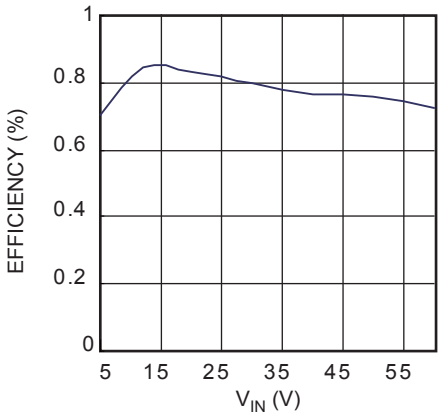
PIN FUNCTIONS *(continued)*

Pin # SOIC16	Pin # TSSOP 16-EP	Name	Description
13	13	DGD	LED Dimming Switch Gate Drive Output Pin.
14	14	VSS	Negative Voltage Output Pin. This pin is the voltage reference for OVP, FB, COMP, SC, DGD and FST pins. This node should be placed away from switching noise sources.
15	15	SW	Switch Output. SW is the source of the internal MOSFET switch. Connect to the power inductor and cathode of the Schottky rectifier.
16	16	BST	Bootstrap. A capacitor is connected between SW and BST pins to form a floating supply across the power switch driver.

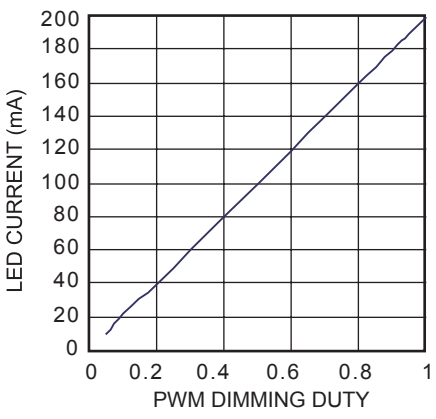
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=20V, I_{LED}=200mA, fPWM=200Hz, OVP point=25V, T_A=+25°C, unless otherwise noted.

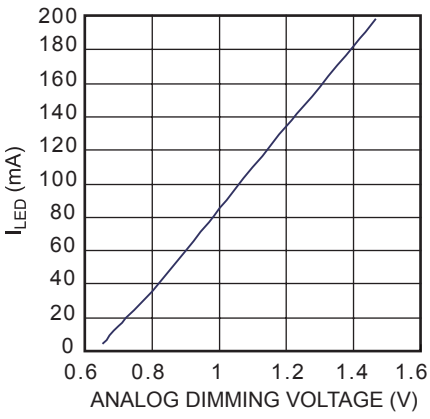
Efficiency vs. V_{IN}



PWM Dimming Curve



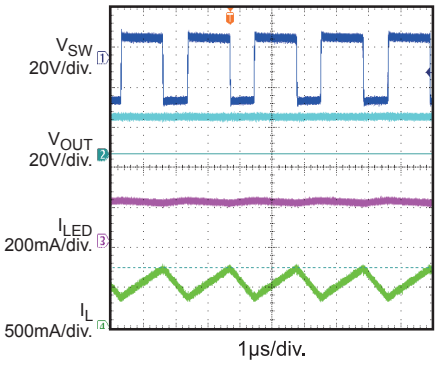
Analog Dimming Curve



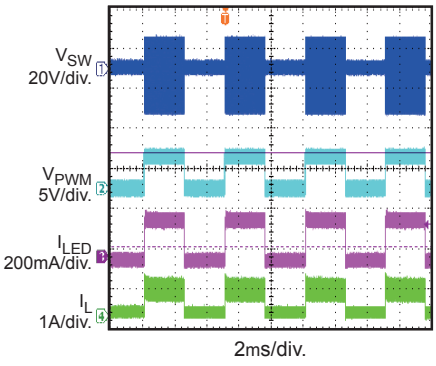
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=20V, I_{LED}=200mA, fPWM=200Hz, OVP point=25V, T_A=+25°C, unless otherwise noted.

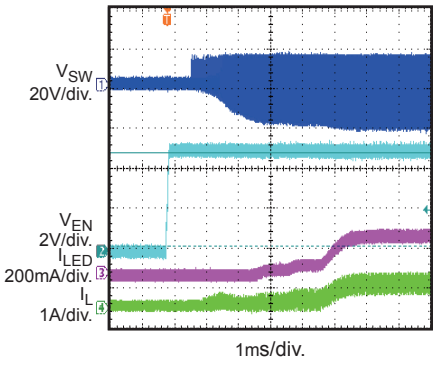
Steady State



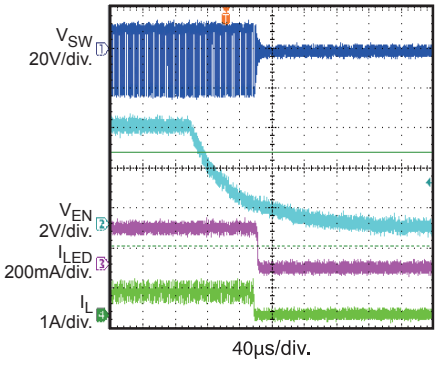
PWM Dimming



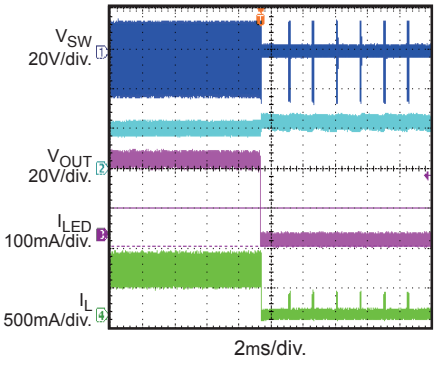
EN ON



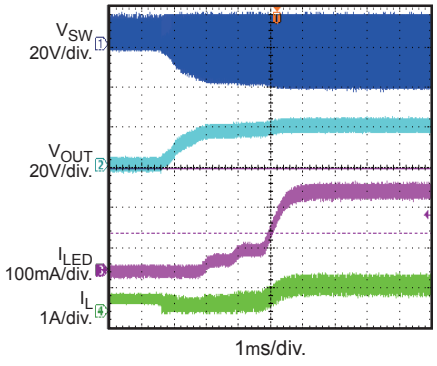
EN OFF



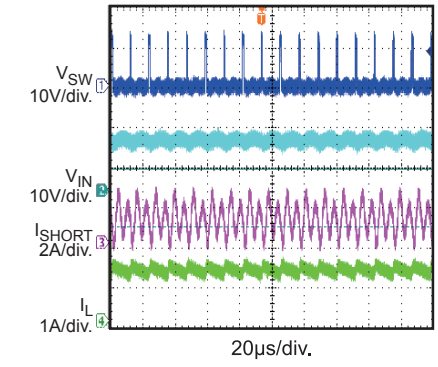
OVP



Short LED+ to LED- (short recover)



Short LED+ to VSS



BLOCK DIAGRAM

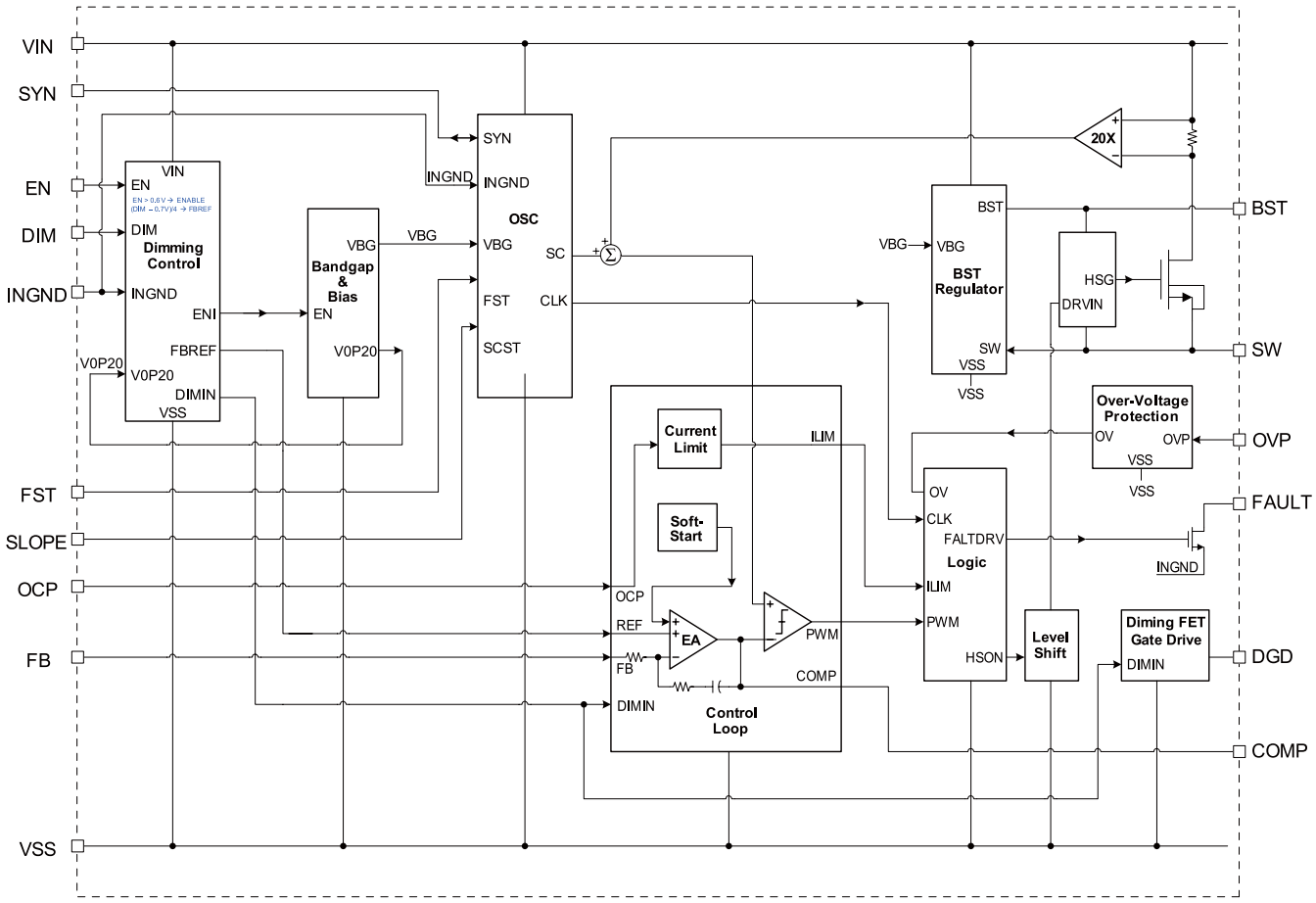


Figure 1—Functional Block Diagram

OPERATION

The MP4601 is a current mode regulator. The sensing resistor senses the LED current and feeds it back to an error amplifier, which regulates it to 200mV with an inside compensation network. The COMP pin is the output of the error amplifier. The inductor peak current is proportional to the COMP pin voltage. An increase of the COMP voltage increases the current delivered to the output.

LED Open Protection

If the LED is open, there is no voltage on the FB pin. The duty cycle will increase until V_{OVP}-V_{VSS} reaches the shutdown threshold. The top switch will turn off until the voltage V_{OVP}-V_{VSS} decreases sufficiently. System enjoys auto-recovery for the LED open protection.

LED Short Protection

If the FB voltage is higher than 600mV, immediately IC is latched off and DGD is pulled low. If FB voltage is higher than 300mV for 480μs, IC is also latched off and DGD is pulled low. The EN needs reset to restart the IC. The Fault pin is pulled low when IC is latched off.

Dimming Control

The MP4601 allows both Analog and PWM dimming. For analog dimming, when the voltage on DIM is from 0.7V to1.5V, the LED current will change from 0% to 100% of the maximum LED current. If the voltage on DIM pin is higher than 1.5V or DIM pin is floated, maximum LED current will be generated.

For PWM dimming, a PWM signal with 100Hz to 50kHz frequency, amplitude over 1.5V should be applied to DIM pin.

For combined PWM and analog dimming to get a further high dimming ratio, apply a 100Hz to 50kHz PWM signal with its amplitude from 0.7V to 1.5V to DIM pin.

DIM pin floated will deliver the maximum LED current.

At PWM dimming off interval, an internal switch disconnects the COMP pin capacitor from the output of the error amplifier. Therefore, the COMP voltage is hold at PWM off interval. This feature improves the response speed of the LED current and helps to achieve high dimming ratio.

Digital dimming can achieve over 1:1000 dimming ratio with DIM frequency less than 200Hz.

APPLICATION INFORMATION

MP4601 is a Buck-boost mode LED driver. Its novel power leverage control technology provides a high efficiency, low cost solution for TV LED driver. With a high bus voltage V_{INH} and a low supply voltage V_{INL} (typical 12V or 24V, not recommend higher than 60V), MP4601 can drive over 60 inch or larger size panel for over 350V LED string voltage.

Setting the LED Current

An external resistor R_{FB} is used to set the maximum LED current through the use of the equation:

$$R_{FB} = \frac{0.200V}{I_{LED}}$$

Setting the Switching Frequency

An external resistor R_{FST} can be used to set the switching frequency f_S through the use of the equation:

$$f_S = 0.95MHz \cdot \frac{60k}{R_{FST}}$$

The equation is effective only for 200kHz to 2MHz frequency programming range.

If FST pin is floating or R_{FST} is larger than 500kΩ, the setting frequency is the default value 0.95MHz.

Setting the Current Limit

An external resistor R_{OCP} can be used to set the cycle-to-cycle current limit I_{LIM} through the use of the equation:

$$I_{LIM} = 4.1A \cdot \frac{100k}{R_{OCP}} - 1.1A$$

The equation is effective only for a range from 30k to 500k for the programming resistor R_{OCP}.

If OCP pin is floating or R_{OCP} is larger than 500kΩ, the current limit is the default value of 2.5A.

Setting the Slope Compensation

MP4601 employs peak current mode control, which will need slope compensation to avoid sub-harmonic oscillation when duty cycle exceeds 50%.

The current loop has effective sense resistor of 0.4Ω. Given a desired input, output voltage relationship, one can estimate the sense current ramp down slope as:

$$S_{DOWN} = \frac{V_L}{L} \cdot 0.4\ V/\mu s$$

Where VL is the voltage across the inductor, and L is the inductor value.

To ensure current loop stability, a compensation slope of at least half of the ramp down slope is needed:

$$S_{SC} >= \frac{1}{2} S_{DOWN}$$

An external resistor R_{SLOPE} can be used to set the slope compensation for the current loop through the use of the equation:

$$S_{SC} = 1.2 V/\mu s \cdot \frac{60k}{R_{SLOPE}}$$

The equation is effective only for a range from 20k to 500k for the programming resistor R_{SLOPE}.

If SLOPE pin is floating or R_{SLOPE} is larger than 500kΩ, the slope compensation is set to default value of 1.2V/μs.

FAULT condition output

MP4601 has an open drain output to indicate FAULT condition. During normal operation, FAULT is high-Z output and user can pull it up to any desired voltage with an external resistor. However, if for some reason, FB is greater than 600mV above VSS, or FB is greater than 300mV above VSS for a pre-determined time of ~480μs, FAULT will be pulled low to INGND level. The Rdson for this pull down switch is ~100Ω.

Selecting the Inductor

Inductor selection is related to the input voltage, output voltage, and LED current. Select the inductor to make the circuit always operate in continuous current mode (CCM). The inductance is designed as:

$$L = \frac{V_{IN} \cdot V_{OUT}}{f_S \cdot (V_{IN} + V_{OUT}) \cdot \Delta I_L}$$

Where ΔI_L is the inductor peak-to-peak current ripple. Design ΔI_L as about 40% to 60% of the inductor average current, which is:

$$I_{L\_AVG} = I_{LED} \cdot (1 + \frac{V_{OUT}}{V_{IN}}).$$

Make sure the inductor is not saturated at the maximum peak current, which is:

$$I_{L\_PK} = I_{L\_AVG} + 0.5 \cdot \Delta I_L .$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Enough capacitance is required for limited input voltage ripple ΔV_{IN}, which should be normally less than 5~10% of the DC value.

$$C_{IN} > \frac{I_{L\_AVG} \cdot V_{OUT}}{f_s \cdot \Delta V_{IN} \cdot (V_{IN} + V_{OUT})}$$

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple ΔV_{OUT} small (normally less than 1~5% of the DC value) and ensures feedback loop stable. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR characteristics.

$$C_{OUT} > \frac{I_{LED} \cdot V_{OUT}}{f_s \cdot \Delta V_{OUT} \cdot (V_{IN} + V_{OUT})}$$

PC Board Layout

The high current paths (VSS, VDD and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the VDD and VSS pins. The external feedback resistors should be placed next to the FB pin. Keep the switch node traces short and away from the feedback network.

TYPICAL APPLICATION CIRCUITS

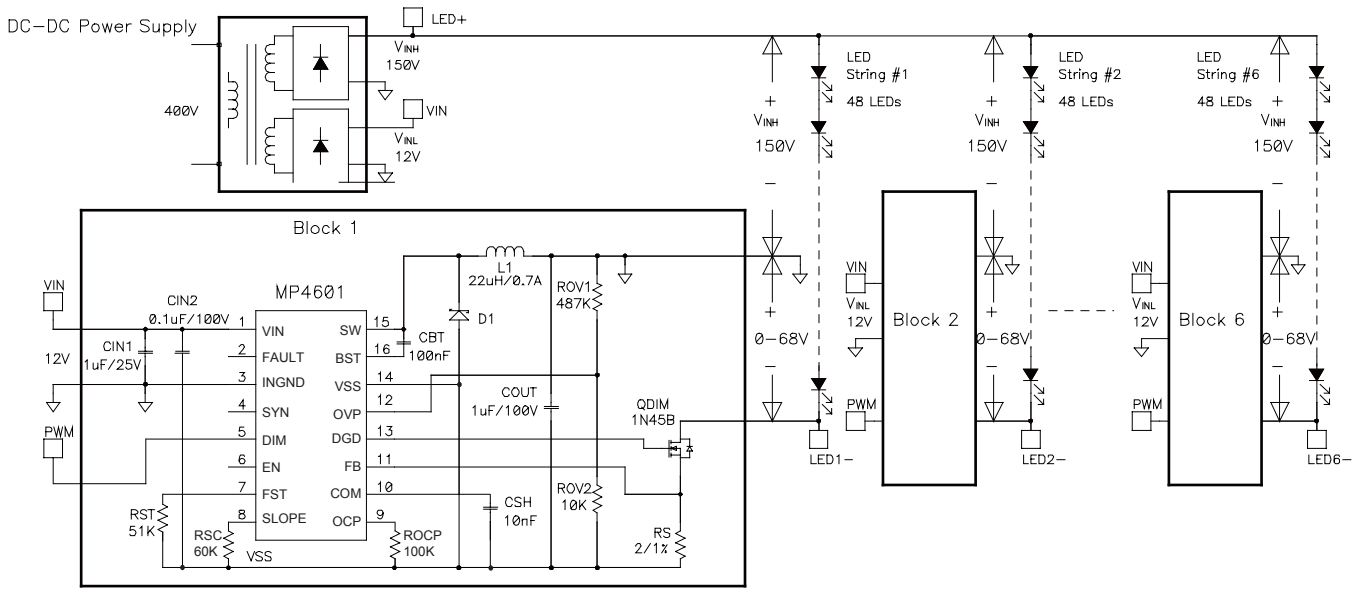
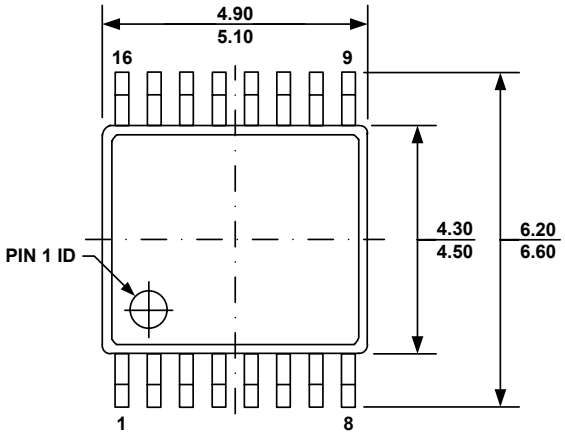


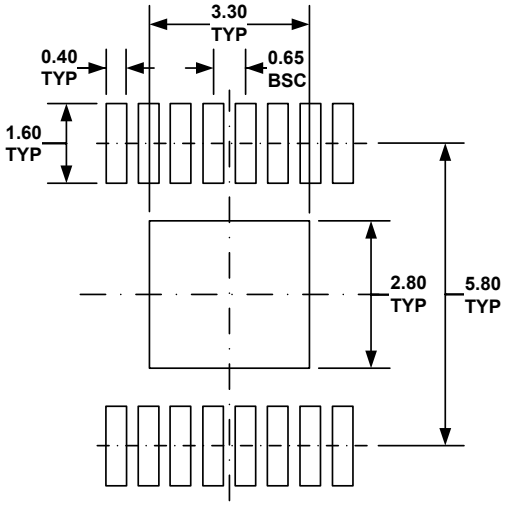
Figure 2—White LED Driver Application for TV Applications

PACKAGE INFORMATION

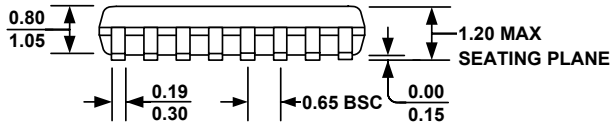
TSSOP16-EP



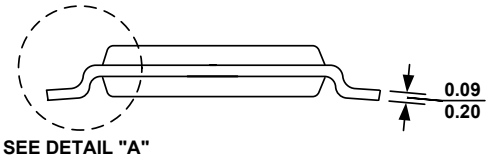
TOP VIEW



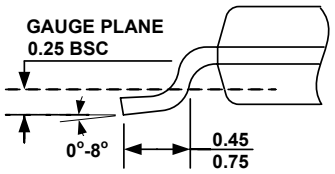
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE.

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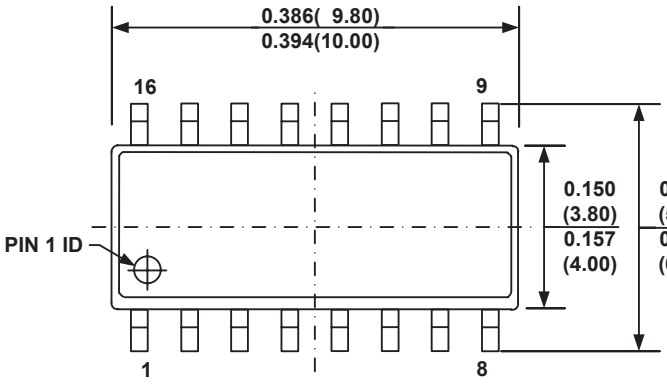
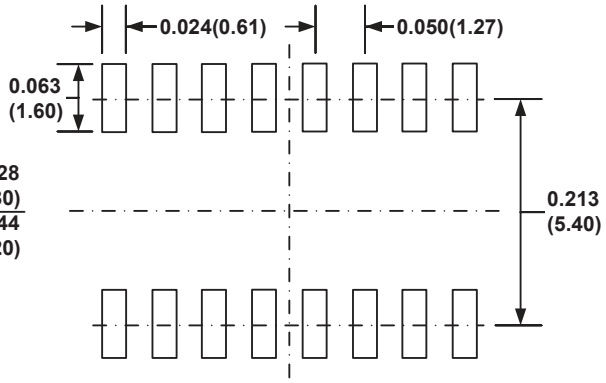
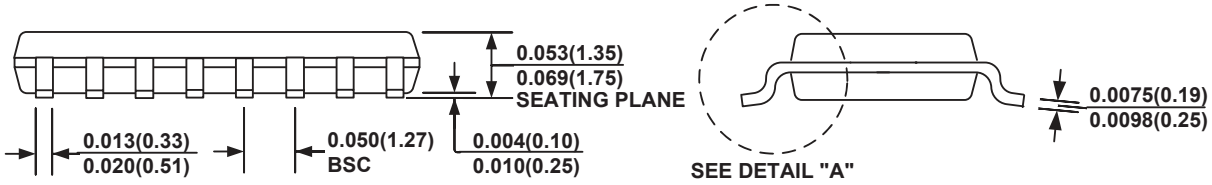


TOP VIEW

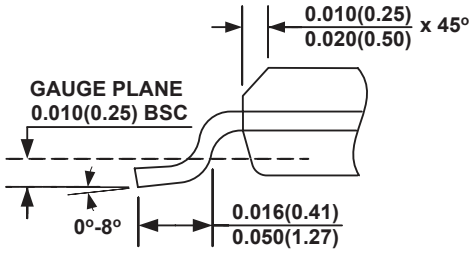


RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.