SPREAD SPECTRUM CLOCK SYNTHESIZER

IDT5P50911/2/3/4

Description

The IDT5P50911/2/3/4 is a family of 1.8V/2.5V/3.3V low power, spread spectrum clock generators capable of reducing EMI radiation from an input clock. Spread spectrum technique is capable of reducing the harmonic frequency amplitude peaks by several dB.

Ordering Information

Output Frequency

5 to 15 MHz - 5P50911NBGI/5P50911DVGI
10 to 30 MHz - 5P50912NBGI/5P50912DVGI
20 to 60 MHz - 5P50913NBGI/5P50913DVGI
40 to 120 MHz - 5P50914NBGI/5P50914DVGI

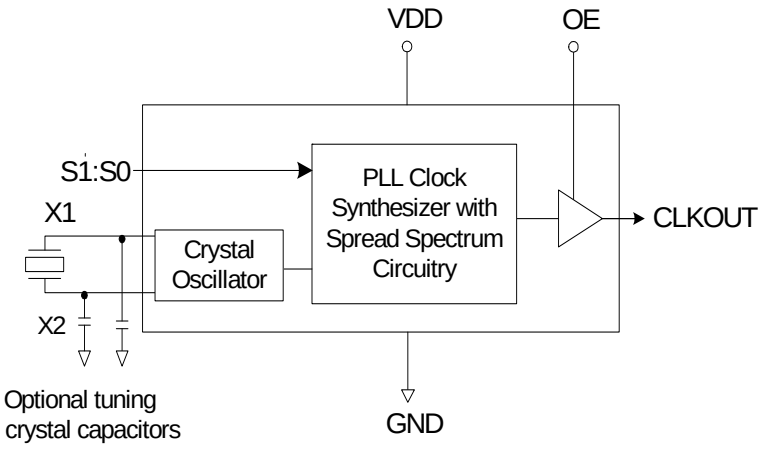
Features

- 8-pin DFN package (2x2mm)
  8-pin MSOP package (3x4.9mm)
- Provides a spread spectrum output clock
- Crystal input frequency range of 10 to 30 MHz
- Output frequency range of 10 to 120 MHz
- Center and down spread
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- Operating voltage of 1.8 V, 2.5 or 3.3V
- RoHS 6 compliant package

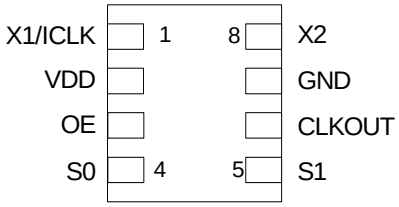
Spread Modulation Frequency Table

Part Number	Output Multiply	Input (MHz)	Modulation (kHz)	Input (MHz)	Modulation (kHz)	Modulation Frequency (kHz)
5P50911	1/2x	10	27	30	81	Input frequency *27/10000
5P50912	1x					
5P50913	2x					
5P50914	4x					

Block Diagram



Pin Assignment



8-pin DFN
8 -pin MSOP

Spread Direction and Percentage Select Table

S1	S0	Spread Direction	Spread Percentage
0	0	OFF	--
0	1	Center	±0.5
1	0	Center	±1.5
1	1	Down	-0.5

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Crystal input. Connect this pin to a crystal.
2	VDD	Power	Voltage supply. Connect to 1.8 V ±0.1 V, 2.5 V ±10% or 3.3 V ±10%,
3	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up.
4	S0	Input	Function select 0 input. Selects spread amount and direction per table above. Internal pull-down resistor.
5	S1	Input	Function select 1 input. Selects spread amount and direction per table above. Internal pull-down resistor.
6	CLKOUT	Output	Clock output. Weal pull-down when OE low.
7	GND	Power	Connect to ground.
8	X2	XO	Crystal output. Connect this pin to a crystal.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the IDT5P50911/2/3/4 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -12 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF [(16-12) x 2 = 8].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

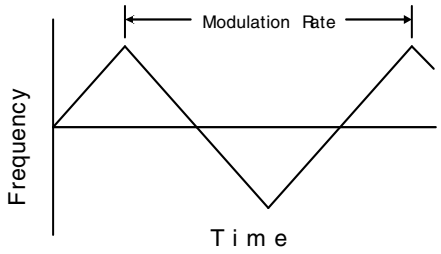
3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDT5P50911/2/3/4. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Spread Spectrum Profile

The IDT5P50911/2/3/4 is a low EMI clock generator using an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices.

The modulation rate is directly relate to the input crystal frequency.

For input frequency ICLK, then use the modulation frequency indicated for the part below.



Modulation Frequency = Input Frequency/10000

Ex. Input Frequency = 20 MHz
Modulation Frequency = 20 MHz/10000 = 2 kHz

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P50911/2/3/4. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7.0 V
All Inputs	-0.5 V to VDD +0.5 V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-50 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage VDD (measured in respect to GND)	+1.7	+1.8	+1.9	V
	+2.25	+2.5	+2.75	V
	+2.97	+3.3	+3.63	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 1.8 V ±0.1 V.** Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.7	1.8	1.9	V
Input High Voltage	V_{IH}	ICLK, S2:S0	VDD x 0.8		VDD + 0.3	V
Input Low Voltage	V_{IL}	ICLK, S2:S0	GND		VDD x 0.2	V
Output High Voltage	V_{OH}	I_{OH} = -18 mA	VDD x 0.9	VDD		V
Output Low Voltage	V_{OL}	I_{OL} = 18 mA		GND	VDD x 0.1	V
IDD		No load		TBD		
Input Capacitance				5		pF
Load Capacitance				5		pF
Internal Pull-up Resistor	R_{PU}	OE		400	520	kΩ
Internal Pull-down Resistor	R_{PD}	S1:S0, CLKOUT		400	520	kΩ

Unless stated otherwise, **VDD = 2.5 V ±10%.** Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.25	2.5	2.75	V
Input High Voltage	V_{IH}	ICLK, S2:S0	VDD x 0.8		VDD + 0.3	V
Input Low Voltage	V_{IL}	ICLK, S2:S0	GND		VDD x 0.2	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	VDD x 0.9	VDD		V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA		GND	VDD x 0.1	V
IDD		No load		TBD		
Input Capacitance				5		pF
Load Capacitance				5		pF
Internal Pull-up Resistor	R_{PU}	OE		300	390	kΩ
Internal Pull-down Resistor	R_{PD}	S1:S0, CLKOUT		300	390	kΩ

Unless stated otherwise, **VDD = 3.3 V ±10%.** Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.97	3.3	3.63	V
Input High Voltage	V_{IH}	ICLK, S2:S0	VDD x 0.8		VDD + 0.3	V
Input Low Voltage	V_{IL}	ICLK, S2:S0	GND		VDD x 0.2	V
Output High Voltage	V_{OH}	I_{OH} = -33 mA	VDD x 0.9	VDD		V
Output Low Voltage	V_{OL}	I_{OL} = 33 mA		GND	VDD x 0.1	V
IDD		No load		TBD		
Input Capacitance				5		pF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Load Capacitance				5		pF
Internal Pull-up Resistor	R_{PU}	OE		200	260	kΩ
Internal Pull-down Resistor	R_{PD}	S1:S0, CLKOUT		200	260	kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 1.8 V ±0.1 V, 2.5 V ±10% or 3.3 V ±10%.** Ambient Temperature -40 to +85°C

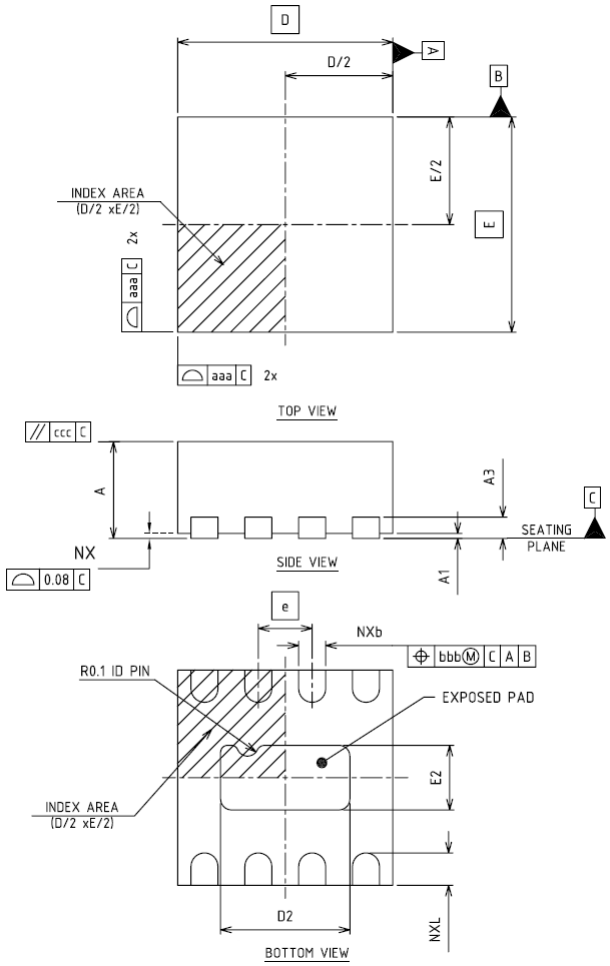
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Duty Cycle			45	50	55	%
Output Rise Time	t_{OR}	20% to 80%, Note 1		1.2		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1.2		ns
Spread Spectrum Modulation Rate		5 to 15 MHz output (IDT5P50911)	27		81	kHz
		10 to 30 MHz output (IDT5P50912)	27		81	kHz
		20 to 60 MHz output (IDT5P50913)	27		81	kHz
		40 to 120 MHz output (IDT5P50914)	27		81	kHz
Jitter Cycle to Cycle		Cycle to cycle jitter		150		ps
Output Settling Time		Note 2			3.0	ms

Note 1: Measured with 5 pF load

Note 2: Time between VDD rising above minimum operating voltage and stable frequency output

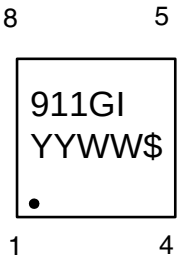
Package Outline and Package Dimensions (8-pin DFN 2x2mm, 0.5mm pitch)

Package dimensions are kept current with JEDEC Publication No. 95,



	Millimeters	
Symbol	**Min**	**Max**
A	0.80	1.00
A1	0	0.05
A3	0.20 Reference	
b	0.20	0.30
N	8	
N_D	4	
N_E	0	
D	2.00 BASIC	
E	2.00 BASIC	
e	0.50 BASIC	
D2	1.05	1.25
E2	0.45	0.65
L	0.20	0.40
aaa	0.15	
bbb	0.10	
ccc	0.10	

Marking Diagram (8DFN)

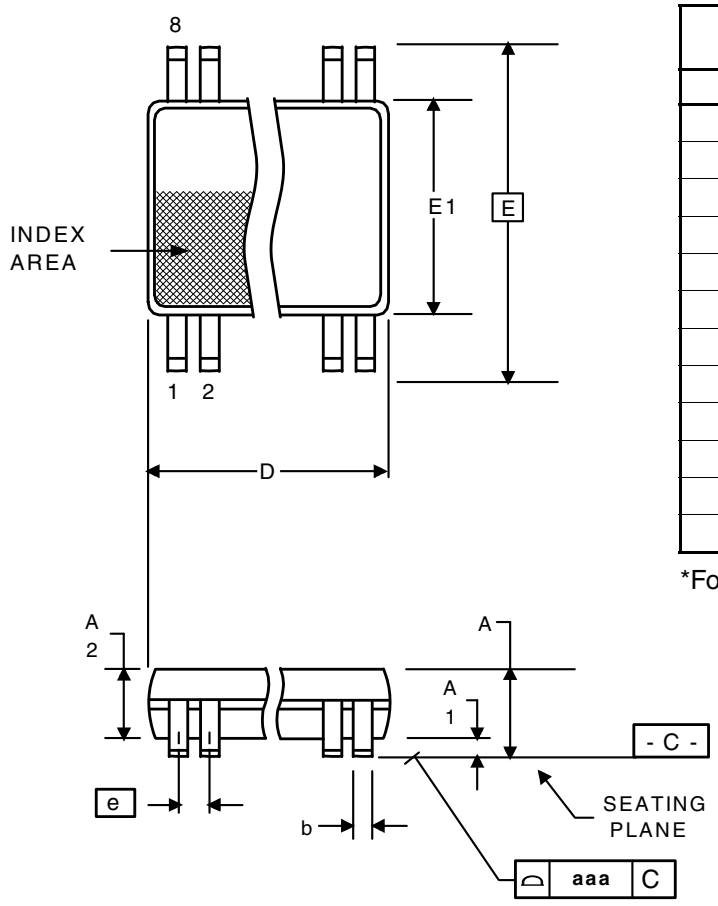


Notes:

1. Line 1: truncated part number (format to be the same for 912, 913, and 914 devices).
2. “G” designates Pb (lead) free package.
3. “I” denotes industrial temperature range.
4. “YYWW” is the last two digits of the year and week that the part was assembled.
5. “$” is the mark code.
6. Bottom marking: country of origin.

Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

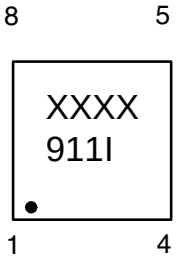
Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.10	--	0.043
A1	0	0.15	0	0.006
A2	0.79	0.97	0.031	0.038
b	0.22	0.38	0.008	0.015
C	0.08	0.23	0.003	0.009
D	3.00 BASIC		0.118 BASIC	
E	4.90 BASIC		0.193 BASIC	
E1	3.00 BASIC		0.118 BASIC	
e	0.65 Basic		0.0256 Basic	
L	0.40	0.80	0.016	0.032
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.

Marking Diagram (8 MSOP)



Notes:

1. “XXXX” is the lot sequence number.
2. Line 2: truncated part number (format to be the same for 912, 913, and 914 devices).
3. “I” denotes industrial temperature range.
4. Bottom marking: country of origin.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5P50911NBGI8	see pages 7,8	Tape and Reel	8-pin DFN	-40°C to +85°C
5P50911DVGI		Tube	8-pin MSOP	-40°C to +85°C
5P50911DVGI8		Tape and Reel	8-pin MSOP	-40°C to +85°C
5P50912NBGI8		Tape and Reel	8-pin DFN	-40°C to +85°C
5P50912DVGI		Tube	8-pin MSOP	-40°C to +85°C
5P50912DVGI8		Tape and Reel	8-pin MSOP	-40°C to +85°C
5P50913NBGI8		Tape and Reel	8-pin DFN	-40°C to +85°C
5P50913DVGI		Tube	8-pin MSOP	-40°C to +85°C
5P50913DVGI8		Tape and Reel	8-pin MSOP	-40°C to +85°C
5P50914NBGI8		Tape and Reel	8-pin DFN	-40°C to +85°C
5P50914DVGI		Tube	8-pin MSOP	-40°C to +85°C
5P50914DVGI8		Tape and Reel	8-pin MSOP	-40°C to +85°C

"G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	R. WIllner	11/10/11	Initial release.
B	R. Willner	12/5/11	Revised pinout and modulation rate.
C	R. Willner	4/6/12	1. Crystal input only. 2. Added marking diagrams.
D	S. Sharma	7/02/14	Changed Modulation Frequency formula and example (pg. 3) input frequency from 400MHz to 10000MHz.

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