LPC54018JxM/LPC54S018JxM

32-bit ARM Cortex-M4 microcontroller; 4MB on-chip Quad SPI Serial Flash; 360 kB SRAM; High-speed USB device/host + PHY; Full-speed USB device/host; Ethernet AVB; LCD; EMC; SPIFI; CAN FD, SDIO; 12-bit 5 Msamples/s ADC; DMIC subsystem

Rev. 1.1 — 27 January 2019 Product data sheet

1. General description

The LPC54018JxM/LPC54S018JxM is a family of ARM Cortex-M4 based microcontrollers for embedded applications featuring a rich peripheral set with very low power consumption and enhanced debug features.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated into the core.

The LPC54018JxM/LPC54S018JxM family includes 4 MB of on-chip Quad SPI Serial Flash (connected on SPIFI interface), 360 KB of on-chip SRAM, one high-speed and one full-speed USB host and device controller, Ethernet AVB, LCD controller, Smart Card Interfaces, SD/MMC, CAN FD, an External Memory Controller (EMC), a DMIC subsystem with PDM microphone interface and I^2S, five general-purpose timers, SCTimer/PWM, RTC/alarm timer, Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), ten flexible serial communication peripherals (USART, SPI, I^2S, I^2C interface), Secure Hash Algorithm (SHA), AES-256 engine, Physical Unclonable Function (PUF), secure boot features, 12-bit 5.0 Msamples/sec ADC, and a temperature sensor.

2. Features and benefits

- ARM Cortex-M4 core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 180 MHz.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug (SWD) with six instruction breakpoints, two literal comparators, and four watch points. Includes Serial Wire Output and ETM Trace for enhanced debug capabilities, and a debug timestamp counter.
  - System tick timer.

- On-chip memory:
  - Up to 4 MB of on-chip Quad SPI Serial Flash (connected on SPIFI interface).
  - Up to 360 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 192 KB SRAM on the I&D buses. 8 KB of SRAM bank intended for USB traffic.
  - General-purpose One-Time Programmable (OTP) memory for user application specific data and for AES keys.
- ROM API support:
  - In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU).
  - Supports serial interface booting (UART, I2C, SPI) from an application processor, automated booting from NOR flash (SPI, quad SPIFI, 8/16/32-bit external parallel flash), and USB booting (full-speed, high-speed).
  - FRO API for selecting FRO output frequency.
  - OTP API for programming OTP memory.
  - Random Number Generator (RNG) API.
  - RSA API calls (LPC54S018Jx only).
- Execute in place (XIP) from internal serial flash (in quad, dual SPIFI mode or single-bit SPI mode), and parallel NOR flash.
- Secure Boot features on LPC54S018Jx devices:
  - Supports boot image authentication using RSASSA-PKCS1-v1_5 signature verification with 2048-bit public keys (2048-bit modulus, 32-bit exponent).
  - Supports Root of Trust (RoT) establishment by comparing the SHA-256 hash digest of the RoT public key with OTP memory contents.
  - Supports secure anti-rollback of images through revocation of image key certificate. Supports up to 8 revocations through OTP fuses.
  - Supports boot of AES-GCM encrypted images with a 128-bit symmetric key stored in OTP memory or a 256-bit symmetric key stored using on-chip SRAM PUF.
  - Secure Authentication Only Boot. Enforce booting of RSA-2048 signed images only.
  - Encrypted Image Boot. Enforce booting of AES-GCM encrypted images only.
  - Enhanced Image Boot. Enforce booting of encrypted then signed images only.
- Security features:
  - AES-256 encryption/decryption engine with keys stored in polyfuse OTP (LPC54S018Jx only).
  - Random number generator can be used to create keys with DMA support.
  - Secure Hash Algorithm (SHA1/SHA2) module supports boot with dedicated DMA controller.
  - Physical Unclonable Function (PUF) root key using dedicated SRAM for silicon fingerprint. PUF can generate, store, and reconstruct key sizes from 64 to 4096 bits (LPC54S018Jx only).

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- Serial interfaces:
  - Flexcomm Interface contains up to 11 serial peripherals. Each Flexcomm Interface (except flexcomm 10, which is dedicated for SPI) can be selected by software to be a USART, SPI, or I2C interface. Two Flexcomm Interfaces also include an I2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I2C pads also support High Speed Mode (3.4 Mbit/s) as a slave.
  - Two ISO 7816 Smart Card Interfaces with DMA support.
  - USB 2.0 high-speed host/device controller with on-chip high-speed PHY.
  - USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00033 for more details.
  - SPIFI with XIP feature connected to on-chip Quad SPI Serial Flash.
  - Ethernet MAC with MII/RMII interface with Audio Video Bridging (AVB) support and dedicated DMA controller.
  - Two CAN FD modules with dedicated DMA controller.
- Digital peripherals:
  - DMA controller with 30 channels and up to 24 programmable triggers, able to access all memories and DMA-capable peripherals.
  - LCD Controller supporting both Super-Twisted Nematic (STN) and Thin-Film Transistor (TFT) displays. It has a dedicated DMA controller, selectable display resolution (up to 1024 x 768 pixels), and supports up to 24-bit true-color mode.
  - External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, in addition to dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 100 MHz. EMC bus width (bit) supports up to 8/16 data line wide static memory.
  - Secured digital input/output (SD/MMC and SDIO) card interface with DMA support.
  - CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
  - Up to 137 General-Purpose Input/Output (GPIO) pins.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
  - Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem includes a dual-channel PDM microphone interface with decimators, filtering, and hardware voice activity detection. The processed output data can be routed directly to an I^2S interface if needed.

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- Timers:
  - Five 32-bit general purpose timers/counters. All five timers support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
  - One SCTimer/PWM with eight input and ten output functions (including capture and match). Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 16 match/captures, 16 events, and 16 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog Oscillator (WDTOSC) with a frequency range of 6 kHz to 1.5 MHz.
  - 32.768 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate and can run from the main oscillator, the internal FRO, the watchdog oscillator or the 32.768 KHz RTC oscillator.
  - Two additional PLLs for USB clock and audio subsystem.
  - Independent clocks for the SPIFI interface, ADC, USBs, and the audio subsystem.
  - Clock output function with divider.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.
  - Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- Single power supply 2.7 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.

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- Operating temperature range −40 °C to +105 °C.
- Available in TFBGA180 package.

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3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54018J2MET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54018J4MET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54S018J2MET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54S018J4MET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3

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3.1 Ordering options

Table 2. Ordering options

Type number	Package Name	Serial Flash/MB	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	EMC data bus width (bit)	Flexcomm Interface	GPIO	SHA	AES	PUF
LPC54018Jx devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, LCD, SHA)															
LPC54018J2MET180	TFBGA180	2	360	yes	yes	yes	yes	yes	yes	8/16	11	137	yes	-	-
LPC54018J4MET180	TFBGA180	4	360	yes	yes	yes	yes	yes	yes	8/16	11	137	yes	-	-
LPC54S018Jx devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, LCD, SHA, AES, PUF)															
LPC54S018J2MET180	TFBGA180	2	360	yes	yes	yes	yes	yes	yes	8/16	11	137	yes	yes	yes
LPC54S018J4MET180	TFBGA180	4	360	yes	yes	yes	yes	yes	yes	8/16	11	137	yes	yes	yes

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4. Marking

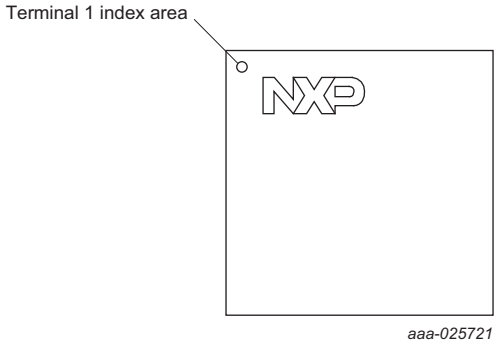

Fig 1. TFBGA180 marking

The LPC54018JxM/LPC54S018JxM TFBGA180 package have the following top-side marking:

- First line: LPC54018JxM/LPC54S018JxM
- Second line: ET180
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1B	Initial device revision with Boot ROM version 21.1

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5. Block diagram

Figure 2 shows the LPC54018JxM/LPC54S018JxM block diagram. In this figure, orange shaded blocks support general purpose DMA and yellow shaded blocks include dedicated DMA control.

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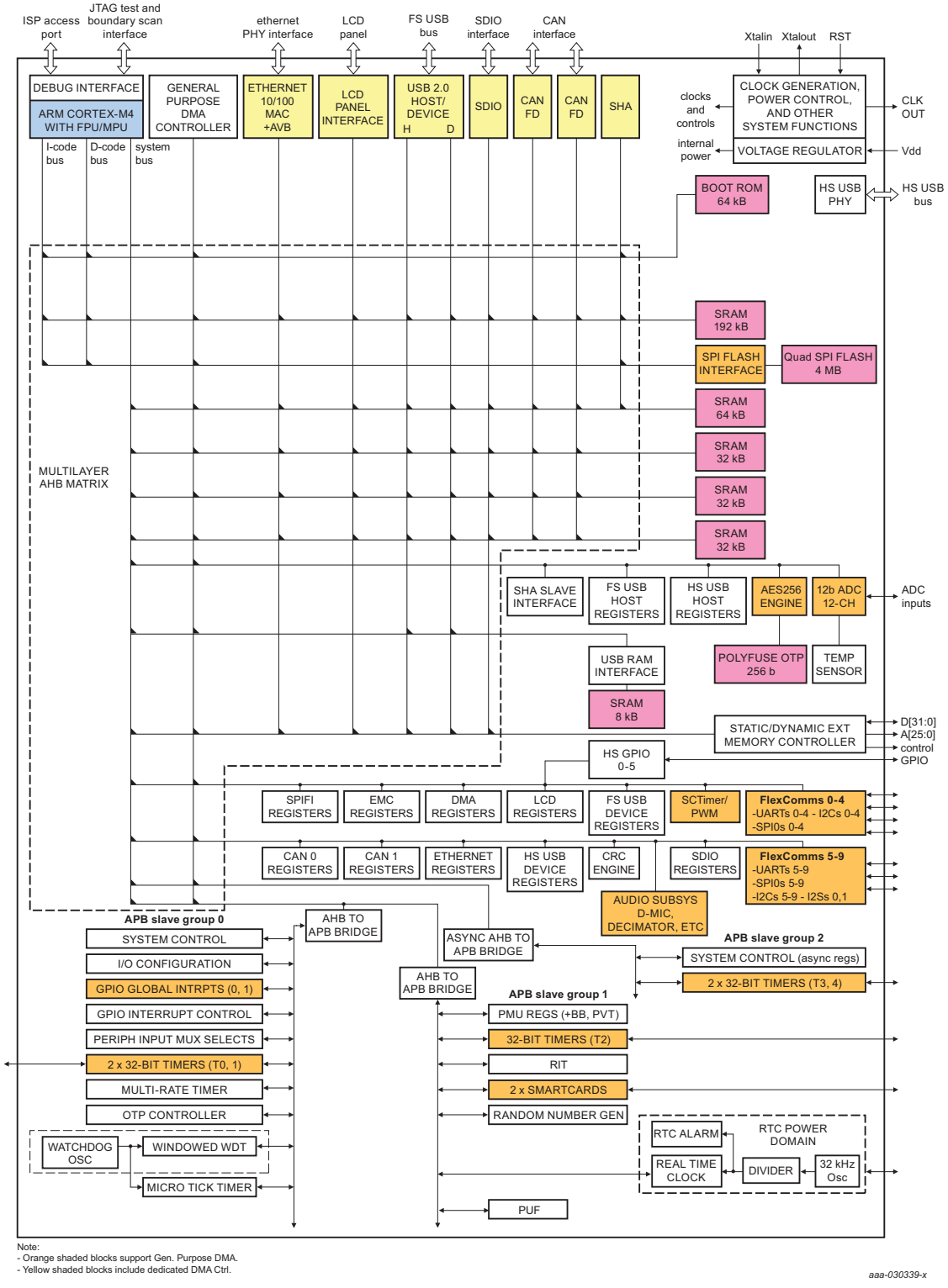

Fig 2. LPC54018JxM/LPC54S018JxM Block diagram

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6. Pinning information

6.1 Pinning

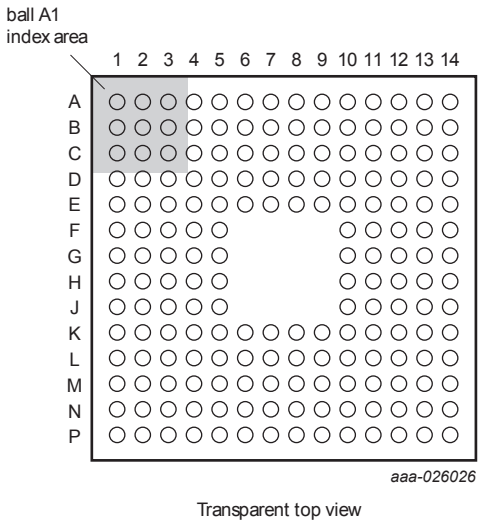

Fig 3. TFBGA 180 Pin configuration

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6.2 Pin description

On the LPC54018JxM/LPC54S018JxM, digital pins are grouped into several ports. Each digital pin can support several different digital functions (including General Purpose I/O (GPIO)) and an additional analog function.

Table 4. Pin description

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_0	D6	[2]	Z	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
				I	**CAN1_RD —** Receiver input for CAN 1.
				I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
				O	**CTimer_MAT0 —** Match output 0 from Timer 0.
				I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
				O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
PIO0_1	A1	[2]	Z	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SSEL0 function.
				O	**CAN1_TD —** Transmitter output for CAN 1.
				I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**CT0_CAP0 —** Capture input 0 to Timer 0.
				I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
				I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
PIO0_2/ TRST	E9	[2]	Z	I/O	**PIO0_2 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
				I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I	**CT0_CAP1 —** Capture input 1 to Timer 0.
				O	**SCT0_OUT0 —** SCTimer/PWM output 0.
				I	**SCT0_GPI[2] —** Pin input 2 to SCTimer/PWM.
				I/O	**EMC_D[0] —** External Memory interface data [0].

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_3/ TCK	A10	[2]	Z	I/O	**PIO0_3 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
				I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**CT0_MAT1 —** Match output 1 from Timer 0.
				O	**SCT0_OUT1 —** SCTimer/PWM output 1.
				I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
					R — Reserved.
				I/O	**EMC_D[1] —** External Memory interface data [1].
PIO0_4/ TMS	C8	[2]	Z	I/O	**PIO0_4 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** The state of this pin at Reset in conjunction with PIO0_5 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
				I	**CAN0_RD —** Receiver input for CAN 0.
				I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
				I	**CT3_CAP0 —** Capture input 0 to Timer 3.
				I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
					R — Reserved.
				I/O	**EMC_D[2] —** External Memory interface data [2].
				O	**ENET_MDC —** Ethernet management data clock.
PIO0_5/ TDI	E7	[2]	Z	I/O	**PIO0_5 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
				O	**CAN0_TD —** Transmitter output for CAN 0.
				I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**CT3_MAT0 —** Match output 0 from Timer 3.
				I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
					R — Reserved.
				I/O	**EMC_D[3] —** External Memory interface data [3].
				I/O	**ENET_MDIO —** Ethernet management data I/O.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_6/ TDO	A5	[2]	Z	I/O	**PIO0_6 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_5 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
				I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
				I	**CT3_CAP1 —** Capture input 1 to Timer 3.
				O	**CT4_MAT0 —** Match output 0 from Timer 4.
				I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
					R — Reserved.
				I/O	**EMC_D[4] —** External Memory interface data [4].
				I	**ENET_RX_DV —** Ethernet receive data valid.
PIO0_7	H12	[2]	Z	I/O	**PIO0_7 —** General-purpose digital input/output pin.
				I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
				O	**SD_CLK —** SD/MMC clock.
				I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
				I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
				O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
				I/O	**EMC_D[5] —** External Memory interface data [5].
				I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
PIO0_8	H10	[2]	Z	I/O	**PIO0_8 —** General-purpose digital input/output pin.
				I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
				I/O	**SD_CMD —** SD/MMC card command I/O.
				I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**SWO —** Serial Wire Debug trace output.
				I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
				I/O	**EMC_D[6] —** External Memory interface data [6].
PIO0_9	G12	[2]	Z	I/O	**PIO0_9 —** General-purpose digital input/output pin.
				I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
				O	**SD_POW_EN —** SD/MMC card power enable.
				I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
				I/O	**EMC_D[7] —** External Memory interface data [7].

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_10/ ADC0_0	P2	[4]	Z	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
				I	**CT2_CAP2 —** Capture input 2 to Timer 2.
				O	**CT2_MAT0 —** Match output 0 from Timer 2.
				I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	L3	[4]	Z	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
				O	**CT2_MAT2 —** Match output 2 from Timer 2.
				I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
					R — Reserved.
					R — Reserved.
				I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.
PIO0_12/ ADC0_2	M3	[4]	Z	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
					R — Reserved.
				I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_13	F11	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
				I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
				I	**CT0_CAP0 —** Capture input 0 to Timer 0.
				I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
					R — Reserved.
					R — Reserved.
				I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	E13	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
				I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
				I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
				I	**CT0_CAP1 —** Capture input 1 to Timer 0.
				I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
					R — Reserved.
					R — Reserved.
				I	**ENET_RXD1 —** Ethernet receive data 1.
PIO0_15/ ADC0_3	L4	[4]	Z	I/O; AI	**PIO0_15/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
				I	**CT4_CAP0 —** Capture input 4 to Timer 0.
				O	**SCT0_OUT2 —** SCTimer/PWM output 2.
					R — Reserved.
				O	**EMC_WEN —** External memory interface Write Enable (active low).
				O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_16/ ADC0_4	M4	[4]	Z	I/O; AI	**PIO0_16/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.ws
				I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
				O	**CLKOUT —** Output of the CLKOUT function.
				I	**CT1_CAP0 —** Capture input 0 to Timer 1.
					R — Reserved.
					R — Reserved.
				O	**EMC_CSN[0] —** External memory interface static chip select 0 (active low).
				O	**ENET_TXD0 —** Ethernet transmit data 0.
PIO0_17	E14	[2]	Z	I/O	**PIO0_17 —** General-purpose digital input/output pin.
				I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
				I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
				O	**SCT0_OUT0 —** SCTimer/PWM output 0.
					R — Reserved.
				O	**EMC_OEN —** External memory interface output enable (active low)
				O	**ENET_TXD1 —** Ethernet transmit data 1.
PIO0_18	C14	[2]	Z	I/O	**PIO0_18 —** General-purpose digital input/output pin.
				I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**SD_WR_PRT —** SD/MMC write protect.
				O	**CT1_MAT0 —** Match output 0 from Timer 1.
				O	**SCT0_OUT1 —** SCTimer/PWM output 1.
				O	**SCI1_SCLK —** SmartCard Interface 1 clock.
				O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C6	[2]	Z	I/O	**PIO0_19 —** General-purpose digital input/output pin.
				I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
				I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
				O	**CT0_MAT2 —** Match output 2 from Timer 0.
				O	**SCT0_OUT2 —** SCTimer/PWM output 2.
					R — Reserved.
				O	**EMC_A[1] —** External memory interface address 1.
				I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_20	D13	[2]	Z	I/O	**PIO0_20 —** General-purpose digital input/output pin.
				I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**CT1_MAT1 —** Match output 1 from Timer 1.
				I	**CT3_CAP3 —** Capture input 3 to Timer 3.
				I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
				I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
				O	**EMC_A[2] —** External memory interface address 2.
				I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	C13	[2]	Z	I/O	**PIO0_21 —** General-purpose digital input/output pin.
				I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
				I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
				O	**CT3_MAT3 —** Match output 3 from Timer 3.
				I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
				O	**SCI0_SCLK —** SmartCard Interface 0 clock.
				O	**EMC_A[3] —** External memory interface address 3.
				I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
PIO0_22	B12	[2][8]	Z	I/O	**PIO0_22 —** General-purpose digital input/output pin.
				I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
				I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
				I	**CT3_CAP3 —** Capture input 3 to Timer 3.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
					R — Reserved.
					R — Reserved.
				I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
PIO0_29	B13	[2]	Z	I/O	**PIO0_29 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART RXD function.
				I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
				O	**CT2_MAT3 —** Match output 3 from Timer 2.
				O	**SCT0_OUT8 —** SCTimer/PWM output 8.
				O	**TRACEDATA[2] —** Trace data bit 2.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO0_30	A2	[2]	Z	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
				I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				O	**CT0_MAT0 —** Match output 0 from Timer 0.
				O	**SCT0_OUT9 —** SCTimer/PWM output 9.
				O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	M5	[4]	Z	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I/O	**SD_D[2] —** SD/MMC data 2.
				O	**CT0_MAT1 —** Match output 1 from Timer 0.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
				O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	N3	[4]	Z	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**SD_D[3] —** SD/MMC data 3.
				I	**CT0_CAP2 —** Capture 2 input to Timer 0.
				I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
				O	**TRACECLK —** Trace clock.
PIO1_1	K12	[2]	Z	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
				I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
				I	**CT0_CAP3 —** Capture 3 input to Timer 0.
				I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
					R — Reserved.
				I/O	**FC10_MOSI —** Flexcomm 10: SPI master-out/slave-in data.
				I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_2	L14	[2]	Z	I/O	**PIO1_2 —** General-purpose digital input/output pin.
				O	**CAN0_TD —** Transmitter output for CAN0.
					R — Reserved.
				O	**CT0_MAT3 —** Match output 3 from Timer0.
				I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
				O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
				I/O	**FC10_MISO —** Flexcomm 10: SPI master-in/slave-out data.
				O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_3	J13	[2]	Z	I/O	**PIO1_3 —** General-purpose digital input/output pin.
				I	**CAN0_RD —** Receiver input for CAN0.
					R — Reserved.
					R — Reserved.
				O	**SCT0_OUT4 —** SCTimer/PWM output 4.
				I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
				O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
					R — Reserved.
				I/O	**FC10_SCK —** Flexcomm 10: SPI clock.
PIO1_4	D4	[2]	Z	I/O	**PIO1_4 —** General-purpose digital input/output pin.
				I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
				I/O	**SD_D[0] —** SD/MMC data 0.
				O	**CT2_MAT1 —** Match output 1 from Timer 2.
				O	**SCT0_OUT0 —** SCTimer/PWM output 0.
				I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
				I/O	**EMC_D[11]) —** External Memory interface data [11].
PIO1_5	E4	[2]	Z	I/O	**PIO1_5 —** General-purpose digital input/output pin.
				I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				I/O	**SD_D[2] —** SD/MMC data 2.
				O	**CT2_MAT0 —** Match output 0 from Timer 2.
				I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
					R — Reserved.
				O	**EMC_A[4] —** External memory interface address 4.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_6	G4	[2]	Z	I/O	**PIO1_6 —** General-purpose digital input/output pin.
				I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I/O	**SD_D[3] —** SD/MMC data 3.
				O	**CT2_MAT1 —** Match output 1 from Timer 2.
				I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
					R — Reserved.
				O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	N1	[2]	Z	I/O	**PIO1_7 —** General-purpose digital input/output pin.
				I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**SD_D[1] —** SD/MMC data 1.
				O	**CT2_MAT2 —** Match output 2 from Timer 2.
				I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
					R — Reserved.
				O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	P8	[2]	Z	I/O	**PIO1_8 —** General-purpose digital input/output pin.
				I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**SD_CLK —** SD/MMC clock.
					R — Reserved.
				O	**SCT0_OUT1 —** SCTimer/PWM output 1.
				I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
				O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K6	[2]	ZZ	I/O	**PIO1_9 —** General-purpose digital input/output pin.
				O	**ENET_TXD0 —** Ethernet transmit data 0.
				I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
				I	**CT1_CAP0 —** Capture 0 input to Timer 1.
				O	**SCT0_OUT2 —** SCTimer/PWM output 2.
				I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**EMC_CASN —** External memory interface column access strobe (active low).

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_10	N9	[2]	Z	I/O	**PIO1_10 —** General-purpose digital input/output pin.
				O	**ENET_TXD1 —** Ethernet transmit data 1.
				I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**CT1_MAT0 —** Match output 0 from Timer 1.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
					R — Reserved.
				O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	[2][8]	Z	I/O	**PIO1_11 —** General-purpose digital input/output pin.
				O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
				I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I	**CT1_CAP1 —** Capture 1 input to Timer 1.
				I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
					R — Reserved.
				O	**EMC_CLK[0] —** External memory interface clock 0.
PIO1_12	K9	[2]	Z	I/O	**PIO1_12 —** General-purpose digital input/output pin.
				I	**ENET_RXD0 —** Ethernet receive data 0.
				I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
				O	**CT1_MAT1 —** Match output 1 from Timer 1.
				O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
				O	**EMC_DYCSN[0] —** External Memory interface SDRAM chip select 0 (active low).
PIO1_13	G10	[2]	Z	I/O	**PIO1_13 —** General-purpose digital input/output pin.
				I	**ENET_RXD1 —** Ethernet receive data 1.
				I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
				I	**CT1_CAP2 —** Capture 2 input to Timer 1.
				I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
				O	**USB0_FRAME —** USB0 frame toggle signal.
				O	**EMC_DQM[0] —** External memory interface data mask 0.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_14	C12	[2]	Z	I/O	**PIO1_14 —** General-purpose digital input/output pin.
				I	**ENET_RX_DV —** Ethernet receive data valid.
				I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
				O	**CT1_MAT2 —** Match output 2 from Timer 1.
				I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**USB0_LEDN —** USB0-configured LED indicator (active low).
				O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	A11	[2]	Z	I/O	**PIO1_15 —** General-purpose digital input/output pin.
				I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
				I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
				I	**CT1_CAP3 —** Capture 3 input to Timer 1.
				I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
				O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B7	[2]	Z	I/O	**PIO1_16 —** General-purpose digital input/output pin.
				O	**ENET_MDC —** Ethernet management data clock.
				I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
				O	**CT1_MAT3 —** Match output 3 from Timer 1.
				I/O	**SD_CMD —** SD/MMC card command I/O.
					R — Reserved.
				O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	N12	[2]	Z	I/O	**PIO1_17 —** General-purpose digital input/output pin.
				I/O	**ENET_MDIO —** Ethernet management data I/O.
				I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
				O	**SCT0_OUT4 —** SCTimer/PWM output 4.
				O	**CAN1_TD —** Transmitter output for CAN 1.
				O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_18	D1	[2]	Z	I/O	**PIO1_18 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				O	**SCT0_OUT5 —** SCTimer/PWM output 5.
				I	**CAN1_RD —** Receiver input for CAN 1.
				O	**EMC_BLSN[1] —** External memory interface byte lane select 1 (active low).
PIO1_19	L1	[2]	Z	I/O	**PIO1_19 —** General-purpose digital input/output pin.
				I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
				O	**SCT0_OUT7 —** SCTimer/PWM output 7.
				O	**CT3_MAT1 —** Match output 1 from Timer 3.
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
				I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
				I/O	**EMC_D[8] —** External Memory interface data [8].
PIO1_20	M1	[2]	Z	I/O	**PIO1_20 —** General-purpose digital input/output pin.
				I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
					R — Reserved.
				I	**CT3_CAP2 —** Capture 2 input to Timer 3.
					R — Reserved.
				I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	N8	[2]	Z	I/O	**PIO1_21 —** General-purpose digital input/output pin.
				I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
					R — Reserved.
				O	**CT3_MAT2 —** Match output 2 from Timer 3.
					R — Reserved.
				I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				I/O	**EMC_D[10] —** External Memory interface data [10].

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_22	P11	[2]	Z	I/O	**PIO1_22 —** General-purpose digital input/output pin.
				I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**SD_CMD —** SD/MMC card command I/O.
				O	**CT2_MAT3 —** Match output 3 from Timer 2.
				I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
				I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
				O	**EMC_CKE[1] —** External memory interface SDRAM clock enable 1.
PIO1_23	M10	[2]	Z	I/O	**PIO1_23 —** General-purpose digital input/output pin.
				I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
				O	**SCT0_OUT0 —** SCTimer/PWM output 0.
					R — Reserved.
				I/O	**ENET_MDIO —** Ethernet management data I/O.
				I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
				O	**EMC_A[11] —** External memory interface address 11.
PIO1_24	N14	[2]	Z	I/O	**PIO1_24 —** General-purpose digital input/output pin.
				I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**SCT0_OUT1 —** SCTimer/PWM output 1.
					R — Reserved.
					R — Reserved.
				I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
				O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	M12	[2]	Z	I/O	**PIO1_25 —** General-purpose digital input/output pin.
				I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
				O	**SCT0_OUT2 —** SCTimer/PWM output 2.
					R — Reserved.
				I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
					R — Reserved.
				O	**EMC_A[13] —** External memory interface address 13.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_26	J10	[2]	Z	I/O	**PIO1_26 —** General-purpose digital input/output pin.
				I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
				I	**CT0_CAP3 —** Capture 3 input to Timer 0.
				I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
					R — Reserved.
				O	**EMC_A[8] —** External memory interface address 8.
PIO1_27	F10	[2]	Z	I/O	**PIO1_27 —** General-purpose digital input/output pin.
				I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**SD_D[4] —** SD/MMC data 4.
				O	**CT0_MAT3 —** Match output 3 from Timer 0.
				O	**CLKOUT —** Output of the CLKOUT function.
					R — Reserved.
				O	**EMC_A[9] —** External memory interface address 9.
PIO1_28	E12	[2]	Z	I/O	**PIO1_28 —** General-purpose digital input/output pin.
				I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
				I/O	**SD_D[5] —** SD/MMC data 5.
				I	**CT0_CAP2 —** Capture 2 input to Timer 0.
					R — Reserved.
					R — Reserved.
				I/O	**EMC_D[12] —** External Memory interface data [12].
PIO1_29	C11	[2][8]	Z	I/O	**PIO1_29 —** General-purpose digital input/output pin.
				I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
				I/O	**SD_D[6] —** SD/MMC data 6.
				I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
				O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
				O	**USB1_FRAME —** USB1 frame toggle signal.
				I/O	**EMC_D[13] —** External Memory interface data [13].

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO1_30	A8	[2]	Z	I/O	**PIO1_30 —** General-purpose digital input/output pin.
				I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
				I/O	**SD_D[7] —** SD/MMC data 7.
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
				I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
				O	**USB1_LEDN —** USB1-configured LED indicator (active low).
				I/O	**EMC_D[14] —** External Memory interface data [14].
PIO1_31	C5	[2]	Z	I/O	**PIO1_31 —** General-purpose digital input/output pin.
				I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
					R — Reserved.
				O	**CT0_MAT2 —** Match output 2 from Timer 0.
				O	**SCT0_OUT6 —** SCTimer/PWM output 6.
				I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I/O	**EMC_D[15] —** External Memory interface data [15].
PIO2_0/ ADC0_7	P3	[4]	Z	I/O; AI	**PIO2_0/ADC0_7 —** General-purpose digital input/output pin. ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					R — Reserved.
				I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
				O	**CT1_CAP0 —** Capture input 0 to Timer 1.
PIO2_1/ ADC0_8	P4	[4]	Z	I/O; AI	**PIO2_1/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					R — Reserved.
				I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
				O	**CT1_MAT0 —** Match output 0 from Timer 1.
PIO2_2	C3	[2]	Z	I/O	**PIO2_2 —** General-purpose digital input/output pin.
				I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
				I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
				O	**SCT0_OUT6 —** SCTimer/PWM output 6.
				O	**CT1_MAT1 —** Match output 1 from Timer 1.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO2_3	B1	[2]	Z	I/O	**PIO2_3 —** General-purpose digital input/output pin.
				O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
				O	**SD_CLK —** SD/MMC clock.
				I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	D3	[2]	Z	I/O	**PIO2_4 —** General-purpose digital input/output pin.
				O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
				I/O	**SD_CMD —** SD/MMC card command I/O.
				I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
				O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	C1	[2]	Z	I/O	**PIO2_5 —** General-purpose digital input/output pin.
				O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
				O	**SD_POW_EN —** SD/MMC card power enable
				I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	F3	[2]	Z	I/O	**PIO2_6 —** General-purpose digital input/output pin.
				I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
				I/O	**SD_D[0] —** SD/MMC data 0.
				I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
				I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	J2	[2]	Z	I/O	**PIO2_7 —** General-purpose digital input/output pin.
				I	**ENET_COL —** Ethernet Collision detect (MII interface).
				I/O	**SD_D(1) —** SD/MMC data 1.
				I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
				I	**CT0_CAP1 —** Capture input 1 to Timer 0.
PIO2_8	F4	[2]	Z	I/O	**PIO2_8 —** General-purpose digital input/output pin.
				I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
				I/O	**SD_D[2] —** SD/MMC data 2.
					R — Reserved.
				O	**CT0_MAT0 —** Match output 0 from Timer 0.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO2_9	K2	[2]	Z	I/O	**PIO2_9 —** General-purpose digital input/output pin.
				I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
				I/O	**SD_D[3] —** SD/MMC data 3.
					R — Reserved.
				O	**CT0_MAT1 —** Match output 0 from Timer 1.
PIO2_10	P1	[2]	Z	I/O	**PIO2_10 —** General-purpose digital input/output pin.
				I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
				I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
PIO2_11	K3	[2]	Z	I/O	**PIO2_11 —** General-purpose digital input/output pin.
				O	**LCD_PWR —** LCD panel power enable.
				O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
					R — Reserved.
					R — Reserved.
				I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
PIO2_12	M2	[2]	Z	I/O	**PIO2_12 —** General-purpose digital input/output pin.
				O	**LCD_LE —** LCD line end signal.
				O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
				I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
					R — Reserved.
				I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_13	P7	[2]	Z	I/O	**PIO2_13 —** General-purpose digital input/output pin.
				O	**LCD_DCLK —** LCD panel clock.
				O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
					R — Reserved.
					R — Reserved.
				I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO2_14	L7	[2][8]	Z	I/O	**PIO2_14 —** General-purpose digital input/output pin.
				O	**LCD_FP —** LCD frame pulse (STN). Vertical synchronization pulse (TFT).
				O	**USB0_FRAME —** USB0 frame toggle signal.
				O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
				O	**CT0_MAT2 —** Match output 2 from Timer 0.
				I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO2_15	M8	[2]	Z	I/O	**PIO2_15 —** General-purpose digital input/output pin.
				O	**LCD_AC —** LCD STN AC bias drive or TFT data enable output.
				O	**USB0_LEDN —** USB0-configured LED indicator (active low).
				I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
				O	**CT0_MAT3 —** Match output 3 from Timer 0.
				I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
PIO2_16	L8	[2][8]	Z	I/O	**PIO2_16 —** General-purpose digital input/output pin.
				O	**LCD_LP —** LCD line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
				O	**USB1_FRAME —** USB1 frame toggle signal.
				O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
				O	**CT1_MAT3 —** Match output 3 from Timer 1.
				I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
PIO2_17	P10	[2]	Z	I/O	**PIO2_17 —** General-purpose digital input/output pin.
				I	**LCD_CLKIN —** LCD clock input.
				O	**USB1_LEDN —** USB1-configured LED indicator (active low).
				I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
				I	**CT1_CAP1 —** Capture 1 input to Timer 1.
				I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_18	N10	[2]	Z	I/O	**PIO2_18 —** General-purpose digital input/output pin.
				O	**LCD_VD[0] —** LCD Data [0].
				I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
				O	**CT3_MAT0 —** Match output 0 from Timer 3.
PIO2_19	P12	[2]	Z	I/O	**PIO2_19 —** General-purpose digital input/output pin.
				O	**LCD_VD[1] —** LCD Data [1].
				I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
				O	**CT3_MAT1 —** Match output 1 from Timer 3.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO2_20	P13	[2]	Z	I/O	**PIO2_20 —** General-purpose digital input/output pin.
				O	**LCD_VD[2] —** LCD Data [2].
				I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
				O	**CT3_MAT2 —** Match output 2 from Timer 3.
				I	**CT4_CAP0 —** Capture input 4 to Timer 0.
PIO2_21	L10	[2]	Z	I/O	**PIO2_21 —** General-purpose digital input/output pin.
				O	**LCD_VD[3] —** LCD Data [3].
				I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
				O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	K10	[2]	Z	I/O	**PIO2_22 —** General-purpose digital input/output pin.
				O	**LCD_VD[4] —** LCD Data [4].
				O	**SCT0_OUT7 —** SCTimer/PWM output 7.
					R — Reserved.
				I	**CT2_CAP0 —** Capture input 0 to Timer 2.
					R — Reserved.
					FC10_SSEL1 — Flexcomm 10: SPI Slave Select 1.
PIO2_23	M14	[2]	Z	I/O	**PIO2_23 —** General-purpose digital input/output pin.
				O	**LCD_VD[5] —** LCD Data [5].
				O	**SCT0_OUT8 —** SCTimer/PWM output 8.
					R — Reserved.
					R — Reserved.
					R — Reserved.
				I/O	**FC10_SSEL2 —** Flexcomm 10: SPI Slave Select 2.
PIO2_24	K14	[2]	Z	I/O	**PIO2_24 —** General-purpose digital input/output pin.
				O	**LCD_VD[6] —** LCD Data [6].
				O	**SCT0_OUT9 —** SCTimer/PWM output 9.
					R — Reserved.
					R — Reserved.
					R — Reserved.
				I/O	**FC10_SSEL3 —** Flexcomm 10: SPI Slave Select 3.
PIO2_25	J11	[2][8]	Z	I/O	**PIO2_25 —** General-purpose digital input/output pin.
				O	**LCD_VD[7] —** LCD Data [7].
				I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO2_26	H11	[2]	Z	I/O	**PIO2_26 —** General-purpose digital input/output pin.
				O	**LCD_VD[8] —** LCD Data [8].
					R — Reserved.
				I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
				I	**CT2_CAP1 —** Capture input 1 to Timer 2.
PIO2_27	H14	[2]	Z	I/O	**PIO2_27 —** General-purpose digital input/output pin.
				O	**LCD_VD[9] —** LCD Data [9].
				I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
				I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
PIO2_28	G13	[2]	Z	I/O	**PIO2_28 —** General-purpose digital input/output pin.
				O	**LCD_VD[10]) —** LCD Data [10].
				I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
					R — Reserved
				I	**CT2_CAP2 —** Capture input 2 to Timer 2.
PIO2_29	G11	[2]	Z	I/O	**PIO2_29 —** General-purpose digital input/output pin.
				O	**LCD_VD[11] —** LCD Data [11].
				I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I	**CT2_CAP3 —** Capture 3 input to Timer 2.
				O	**CLKOUT —** Output of the CLKOUT function.
PIO2_30	F12	[2]	Z	I/O	**PIO2_30 —** General-purpose digital input/output pin.
				O	**LCD_VD[12] —** LCD Data [12].
					R — Reserved.
					R — Reserved.
				O	**CT2_MAT2 —** Match output 2 from Timer 2.
PIO2_31	D14	[2]	Z	I/O	**PIO2_31 —** General-purpose digital input/output pin.
				O	**LCD_VD[13] —** LCD Data [13].
PIO3_0	D12	[2]	Z	I/O	**PIO3_0 —** General-purpose digital input/output pin.
				O	**LCD_VD[14] —** LCD Data [14].
				O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					R — Reserved.
				O	**CT1_MAT0 —** Match output 0 from Timer 1.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_1	D11	[2]	Z	I/O	**PIO3_1 —** General-purpose digital input/output pin.
				O	**LCD_VD[15] —** LCD Data [15].
				I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
					R — Reserved.
				O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO3_2	C10	[2]	Z	I/O	**PIO3_2 —** General-purpose digital input/output pin.
				O	**LCD_VD[16] —** LCD Data [16].
				I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
				O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO3_3	A13	[2]	Z	I/O	**PIO3_3 —** General-purpose digital input/output pin.
				O	**LCD_VD[17] —** LCD Data [17].
				I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_4	B11	[2]	Z	I/O	**PIO3_4 —** General-purpose digital input/output pin.
				O	**LCD_VD[18] —** LCD Data [18].
					R — Reserved.
				I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**CT4_CAP1 —** Capture input 4 to Timer 1.
PIO3_5	B10	[2]	Z	I/O	**PIO3_5 —** General-purpose digital input/output pin.
				O	**LCD_VD[19] —** LCD Data [19].
					R — Reserved.
				I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
				O	**CT4_MAT1 —** Match output 1 from Timer 4.
PIO3_6	C9	[2]	Z	I/O	**PIO3_6 —** General-purpose digital input/output pin.
				O	**LCD_VD[20] —** LCD Data [20].
				O	**LCD_VD[0] —** LCD Data [0].
					R — Reserved.
				O	**CT4_MAT2 —** Match output 2 from Timer 4.
PIO3_7	B8	[2]	Z	I/O	**PIO3_7 —** General-purpose digital input/output pin.
				O	**LCD_VD[21] —** LCD Data [21].
				O	**LCD_VD[1] —** LCD Data [1].
					R — Reserved.
				I	**CT4_CAP2 —** Capture input 2 to Timer 4.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_8	A7	[2]	Z	I/O	**PIO3_8 —** General-purpose digital input/output pin.
				O	**LCD_VD[22] —** LCD Data [22].
				O	**LCD_VD[2] —** LCD Data [2].
					R — Reserved.
				I	**CT4_CAP3 —** Capture input 3 to Timer 4.
PIO3_9	C7	[2]	Z	I/O	**PIO3_9 —** General-purpose digital input/output pin.
				O	**LCD_VD[23] —** LCD Data [23].
				O	**LCD_VD[3] —** LCD Data [3].
					R — Reserved.
				I	**CT0_CAP2 —** Capture input 2 to Timer 0.
PIO3_10	A3	[2]	Z	I/O	**PIO3_10 —** General-purpose digital input/output pin.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
					R — Reserved.
				O	**CT3_MAT0 —** Match output 0 from Timer 3.
					R — Reserved.
					R — Reserved.
				O	**EMC_DYCSN[1] —** External Memory interface SDRAM chip select 1(active low).
				O	**TRACEDATA[0] —** Trace data bit 0.
PIO3_11	B2	[2]	Z	I/O	**PIO3_11 —** General-purpose digital input/output pin.
				I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
				I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
				I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
					R — Reserved.
					R — Reserved.
					R — Reserved.
				O	**TRACEDATA[3] —** Trace data bit 3.
PIO3_12	L2	[2]	Z	I/O	**PIO3_12 —** General-purpose digital input/output pin.
				O	**SCT0_OUT8 —** SCTimer/PWM output 8.
					R — Reserved.
				I	**CT3_CAP0 —** Capture input 0 to Timer 3.
					R — Reserved.
				O	**CLKOUT —** Output of the CLKOUT function.
				O	**EMC_CLK[1] —** External memory interface clock 1.
				O	**TRACECLK —** Trace clock.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_13	H4	[2]	Z	I/O	**PIO3_13 —** General-purpose digital input/output pin.
				O	**SCT0_OUT9 —** SCTimer/PWM output 9.
				I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**CT3_CAP1 —** Capture input 1 to Timer 3.
					R — Reserved.
					R — Reserved.
				I	**EMC_FBCK —** External memory interface feedback clock.
				O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	E3	[2]	Z	I/O	**PIO3_14 —** General-purpose digital input/output pin.
				O	**SCT0_OUT4 —** SCTimer/PWM output 4.
				I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
				O	**CT3_MAT1 —** Match output 1 from Timer 3.
					R — Reserved.
					R — Reserved.
					R — Reserved.
				O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	D2	[2]	Z	I/O	**PIO3_15 —** General-purpose digital input/output pin.
				I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
				I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	E1	[2]	Z	I/O	**PIO3_16 —** General-purpose digital input/output pin.
				I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	K1	[2]	Z	I/O	**PIO3_17 —** General-purpose digital input/output pin.
				I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	M6	[2]	Z	I/O	**PIO3_18 —** General-purpose digital input/output pin.
				I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I/O	**SD_D[6] —** SD/MMC data 6.
				O	**CT4_MAT0 —** Match output 0 from Timer 4.
				O	**CAN0_TD —** Transmitter output for CAN 0.
				O	**SCT0_OUT5 —** SCTimer/PWM output 5.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_19	J3	[2]	Z	I/O	**PIO3_19 —** General-purpose digital input/output pin.
				I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
				I/O	**SD_D[7] —** SD/MMC data 7.
				O	**CT4_MAT1 —** Match output 1 from Timer 4.
				I	**CAN0_RD —** Receiver input for CAN 0.
				O	**SCT0_OUT6 —** SCTimer/PWM output 6.
PIO3_20	N2	[2]	Z	I/O	**PIO3_20 —** General-purpose digital input/output pin.
				I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
				I	**SD_CARD_INT_N —**
				O	**CLKOUT —** Output of the CLKOUT function.
					R — Reserved.
				O	**SCT0_OUT7 —** SCTimer/PWM output 7.
PIO3_21/ ADC0_9	P5	[4]	Z	I/O; AI	**PIO3_21/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
				O	**CT4_MAT3 —** Match output 3 from Timer 4.
				I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO3_22/ ADC0_10	N5	[4]	Z	I/O; AI	**PIO3_22/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
				I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_23	C2	[3]	Z	I/O	**PIO3_23 —** General-purpose digital input/output pin.
				I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
					R — Reserved.
				I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
PIO3_24	E2	[3]	Z	I/O	**PIO3_24 —** General-purpose digital input/output pin.
				I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
				I	**CT4_CAP0 —** Capture input 4 to Timer 0.
				I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_25	P9	[2]	Z	I/O	**PIO3_25 —** General-purpose digital input/output pin.
					R — Reserved.
				I	**CT4_CAP2 —** Capture input 2 to Timer 4.
				I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[14] —** External memory interface address 14.
PIO3_26	K5	[2]	Z	I/O	**PIO3_26 —** General-purpose digital input/output pin.
					R — Reserved.
				O	**SCT0_OUT0 —** SCTimer/PWM output 0.
				I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[15] —** External memory interface address 15.
PIO3_27	P14	[2]	Z	I/O	**PIO3_27 —** General-purpose digital input/output pin.
					R — Reserved.
				O	**SCT0_OUT1 —** SCTimer/PWM output 1.
				I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[16] —** External memory interface address 16.
PIO3_28	M11	[2]	Z	I/O	**PIO3_28 —** General-purpose digital input/output pin.
					R — Reserved.
				O	**SCT0_OUT2 —** SCTimer/PWM output 2.
				I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[17] —** External memory interface address 17.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO3_29	L13	[2]	Z	I/O	**PIO3_29 —** General-purpose digital input/output pin.
					R — Reserved.
				O	**SCT0_OUT3 —** SCTimer/PWM output 3.
				I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[18] —** External memory interface address 18.
PIO3_30	K13	[2]	Z	I/O	**PIO3_30 —** General-purpose digital input/output pin.
				I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**SCT0_OUT4 —** SCTimer/PWM output 4.
				I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
					R — Reserved.
					R — Reserved.
				O	**EMC_A[19] —** External memory interface address 19.
PIO3_31	J14	[2]	Z	I/O	**PIO3_31 —** General-purpose digital input/output pin.
				I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
				O	**SCT0_OUT5 —** SCTimer/PWM output 5.
				O	**CT4_MAT2 —** Match output 2 from Timer 4.
					R — Reserved.
				I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
				O	**EMC_A[20] —** External memory interface address 20.
PIO4_0	H13	[2]	Z	I/O	**PIO4_0 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**CT4_CAP1 —** Capture input 4 to Timer 1.
					R — Reserved.
				I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
				O	**EMC_CSN[1] —** External memory interface static chip select 1(active low).

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO4_1	G14	[2]	Z	I/O	**PIO4_1 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
					R — Reserved.
					R — Reserved.
				I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
				O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	F14	[2]	Z	I/O	**PIO4_2 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
					R — Reserved.
					R — Reserved.
				I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
				O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	F13	[2]	Z	I/O	**PIO4_3 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
				I	**CT0_CAP3 —** Capture 3 input to Timer 0.
					R — Reserved.
				I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
				O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	D9	[2]	Z	I/O	**PIO4_4 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
				I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
					R — Reserved.
				I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
				O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO4_5	E10	[2]	Z	I/O	**PIO4_5 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				O	**CT4_MAT3 —** Match output 3 from Timer 4.
				I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
				O	**EMC_CKE[2] —** External memory interface SDRAM clock enable 2.
PIO4_6	D10	[2]	Z	I/O	**PIO4_6 —** General-purpose digital input/output pin.
					R — Reserved.
				I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
					R — Reserved.
					R — Reserved.
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
				O	**EMC_CKE[3] —** External memory interface SDRAM clock enable 3.
PIO4_7	A14	[2][8]	Z	I/O	**PIO4_7 —** General-purpose digital input/output pin.
					R — Reserved.
				I	**CT4_CAP3 —** Capture input 3 to Timer 4.
				O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
				O	**USB0_FRAME —** USB0 frame toggle signal.
				I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
PIO4_8	B14	[2]	Z	I/O	**PIO4_8 —** General-purpose digital input/output pin.
				O	**ENET_TXD0 —** Ethernet transmit data 0.
				I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
				I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
				O	**USB0_LEDN —** USB0-configured LED indicator (active low).
				I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
PIO4_9	A12	[2][8]	Z	I/O	**PIO4_9 —** General-purpose digital input/output pin.
				O	**ENET_TXD1 —** Ethernet transmit data 1.
				I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
				O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
				O	**USB1_FRAME —** USB1 frame toggle signal.
				I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.

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Table 4. Pin description *...continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
PIO4_10	B9	[2]	Z	I/O	**PIO4_10 —** General-purpose digital input/output pin.
				I	**ENET_RX_DV —** Ethernet receive data valid.
				I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
				I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
				O	**USB1_LEDN —** USB1-configured LED indicator (active low).
					SCT0_GPI3 — Pin input 3 to SCTimer/PWM.
PIO4_11	A9	[2]	Z	I/O	**PIO4_11 —** General-purpose digital input/output pin.
				I	**ENET_RXD0 —** Ethernet receive data 0.
				I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
				I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
					R — Reserved.
				I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
PIO4_12	A6	[2]	Z	I/O	**PIO4_12 —** General-purpose digital input/output pin.
				I	**ENET_RXD1 —** Ethernet receive data 1.
				I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
					R — Reserved.
				I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
PIO4_13	B6	[2]	Z	I/O	**PIO4_13 —** General-purpose digital input/output pin.
				O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
				O	**CT4_MAT0 —** Match output 0 from Timer 4.
					R — Reserved.
				I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
PIO4_14	B5	[2]	Z	I/O	**PIO4_14 —** General-purpose digital input/output pin.
				I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
				O	**CT4_MAT1 —** Match output 1 from Timer 4.
				I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
					R — Reserved.
				I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
USB1_AVSSC	F2				USB1 analog 3.3 V ground.
USB1_REXT	F1				USB1 analog signal for reference resistor, 12.4 kΩ +/-1%
USB1_ID	G1				Indicates to the transceiver whether connected as an A-device (USB1_ID LOW) or B-device (USB1_ID HIGH).

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
USB1_VBUS	G2	[6][8]		I/O	VBUS pin (power on USB cable). 5 V tolerant when USB1_AVDD3V3 and USB1_AVDDTX3V3 = 0 V.
USB1_AVDDC3V3	G3				USB1 analog 3.3 V supply.
USB1_AVDDTX3V3	H1				USB1 analog 3.3 V supply for line drivers.
USB1_DP	H3	[6]		I/O	USB1 bidirectional D+ line.
USB1_DM	H2	[6]		I/O	USB1 bidirectional D- line.
USB1_AVSSTX3V3	J1				USB1 analog ground for line drivers.
USB0_DP	E5	[6]		I/O	USB0 bidirectional D+ line.
USB0_DM	D5	[6]		I/O	USB0 bidirectional D- line.
RESETN	N13	[5]			External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.
VDD	A4 E6; E8; F5; G5; J12; L6; L11		-	-	Single 2.7 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	B3; D7; D8; E11; H5; J5; K7		-	-	Ground.
VDDA	N6		-	-	Analog supply voltage.
VREFN	N4		-	-	ADC negative reference voltage.
VREFP	P6		-	-	ADC positive reference voltage.
VSSA	L5		-	-	Analog ground.
XTALIN	K4	[7]	-	-	Main oscillator input.
XTALOUT	J4	[7]	-	-	Main oscillator output.
VBAT	N11		-	-	Battery supply voltage. If no battery is used, tie VBAT to VDD or to ground.
RTCXIN	L12		-	-	RTC oscillator input.

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Table 4. Pin description *…continued*

Symbol	180-pin, TFBGA		Reset state[1] [9]	Type	Description
RTCXOUT	K11		-	-	RTC oscillator output.
Flash Enable	N7; C4		PU	I	**Flash Enable —** Enables the internal serial flash memory. Pins C4 and N7 must be connected to each other.
N.C.	K8; L9; M7; M9; M13		-	-	**Not Connected pins —** These pins must be left unconnected (floating).

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 39. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

[9] Z = high impedance; pull-up or pull-down disabled. GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

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Table 5. Termination of unused pins

Pin	Default state[1][2]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; Z	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USBn_DM	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USB1_AVSCC	F	Tie to VSS.
USB1_VBUS	F	Tie to VDD.
USB1_AVDDC3V3	F	Tie to VDD.
USB1_AVDDTX3V3	F	Tie to VDD.
USB1_AVSSTX3V3	F	Tie to VSS.
USB1_ID	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled, F = Floating

[2] Z = high impedance; pull-up or pull-down disabled. GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down[3]
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled or high Z [2].			Floating
PIO0_13 to PIO0_14 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
PIO3_23 to PIO3_24 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

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[1] Default and programmed pin states are retained in sleep and deep-sleep.

[2] Z = high impedance; pull-up or pull-down disabled. GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

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7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC54018JxM/LPC54S018JxM uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

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7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- Supports up to 54 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M4 core clock.

7.7 On-chip serial flash

The LPC54018JxM/LPC54S018JxM supports up to 4 MB of on-chip Quad SPI Serial Flash (connected on SPIFI interface).

7.8 On-chip static RAM

The LPC54018JxM/LPC54S018JxM support 360 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.9 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-Application Programming (IAP) and In-System Programming (ISP).
- ROM-based USB drivers (HID, CDC, MSC, and DFU).
- Supports serial interface booting (UART, I2C, SPI) from an application processor, automated booting from NOR flash (SPI, quad SPIFI, 8/16/32-bit external parallel flash), and USB booting (full-speed, high speed).
- Execute in place (XIP) from SPIFI NOR flash (in quad, dual SPIFI mode or single-bit SPI mode), and parallel NOR flash.
- FRO API for selecting FRO output frequency.
- OTP API for programming OTP memory.
- Random Number Generator (RNG) API.

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- RSA API calls (LPC54S018Jx only).
- Secure Boot features on LPC54S018Jx devices:
  - Supports boot image authentication using RSASSA-PKCS1-v1_5 signature verification with 2048-bit public keys (2048-bit modulus, 32-bit exponent).
  - Supports Root of Trust (RoT) establishment by comparing the SHA-256 hash digest of the RoT public key with OTP memory contents.
  - Supports secure anti-rollback of images through revocation of image key certificate. Supports up to 8 revocations through OTP fuses.
  - Supports boot of AES-GCM encrypted images with a 128-bit symmetric key stored in OTP memory or a 256-bit symmetric key stored using on-chip SRAM PUF.
  - Secure Authentication Only Boot. Enforce booting of RSA-2048 signed images only.
  - Encrypted Image Boot. Enforce booting of AES-GCM encrypted images only.
  - Enhanced Image Boot. Enforce booting of encrypted then signed images only.

7.10 Memory mapping

The LPC54018JxM/LPC54S018JxM incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 4 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

The ARM Cortex-M4 processor has a single 4 GB address space. The following table shows how this space is used on the LPC54018JxM/LPC54S018JxM.

Table 7. Memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	SRAMX	0x0000 0000 - 0x0002 FFFF	I&D SRAM bank (192 kB).
	Boot ROM	0x0300 0000 - 0x0300 FFFF	Boot ROM with API services in a 64 kB space.
	On-chip Serial Flash Memory (connected to SPIFI interface)	0x1000 0000 - 0x103F FFFF	Serial flash memory mapped access space (4 MB).
0x2000 0000 to 0x3FFF FFFF	Main SRAM Banks	0x2000 0000 - 0x2002 7FFF	SRAM0, SRAM1, SRAM2, SRAM3 banks (Total 160 kB).
	SRAM bit band alias addressing	0x2200 0000 - 0x23FF FFFF	SRAM bit band alias addressing (32 MB).
	SRAM Bank	0x4010 0000 0x4010 2000	USB SRAM (8 kB).

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Table 7. Memory usage and details *…continued*

Address range	General Use	Address range details and description	
0x4000 0000 to 0x7FFF FFFF	APB peripherals	0x4000 0000 - 0x4001 FFFF	APB slave group 0 up to 32 peripheral blocks of 4 kB each (128 kB).
		0x4002 0000 - 0x4003 FFFF	APB slave group 1 up to 32 peripheral blocks of 4 kB each (128 kB).
		0x4004 0000 - 0x4005 FFFF	APB asynchronous slave group 2 up to 32 peripheral blocks of 4 kB each (128 kB).
	AHB peripherals	0x4008 0000 - 0x400B FFFF	AHB peripherals (256 kB).
	Peripheral bit band alias addressing	0x4200 0000 - 0x43FF FFFF	Peripheral bit band alias addressing (32 MB).
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)[1]
		0x8800 0000 - 0x8BFF FFFF	Static memory chip select 1 (up to 64 MB)[2]
		0x9000 0000 – 0x93FF FFFF	Static memory chip select 2 (up to 64 MB).
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 3 (up to 64 MB).
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xA7FF FFFF	Dynamic memory chip select 0 (up to 256 MB).
		0xA800 0000 - 0xAFFF FFFF	Dynamic memory chip select 1 (up to 256 MB).
		0xB000 0000 - 0xB7FF FFFF	Dynamic memory chip select 2 (up to 256 MB).
		0xB800 0000 - 0xBFFF FFFF	Dynamic memory chip select 3 (up to 256 MB).
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

[1] Can be up to 256 MB, upper address 0x8FFF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the LPC54018JxM/LPC54S018JxM *user manual*.

[2] Can be up to 128 MB, upper address 0x97FF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the LPC54018JxM/LPC54S018JxM *user manual*.

Figure 4 shows the overall map of the entire address space from the user program viewpoint following reset.

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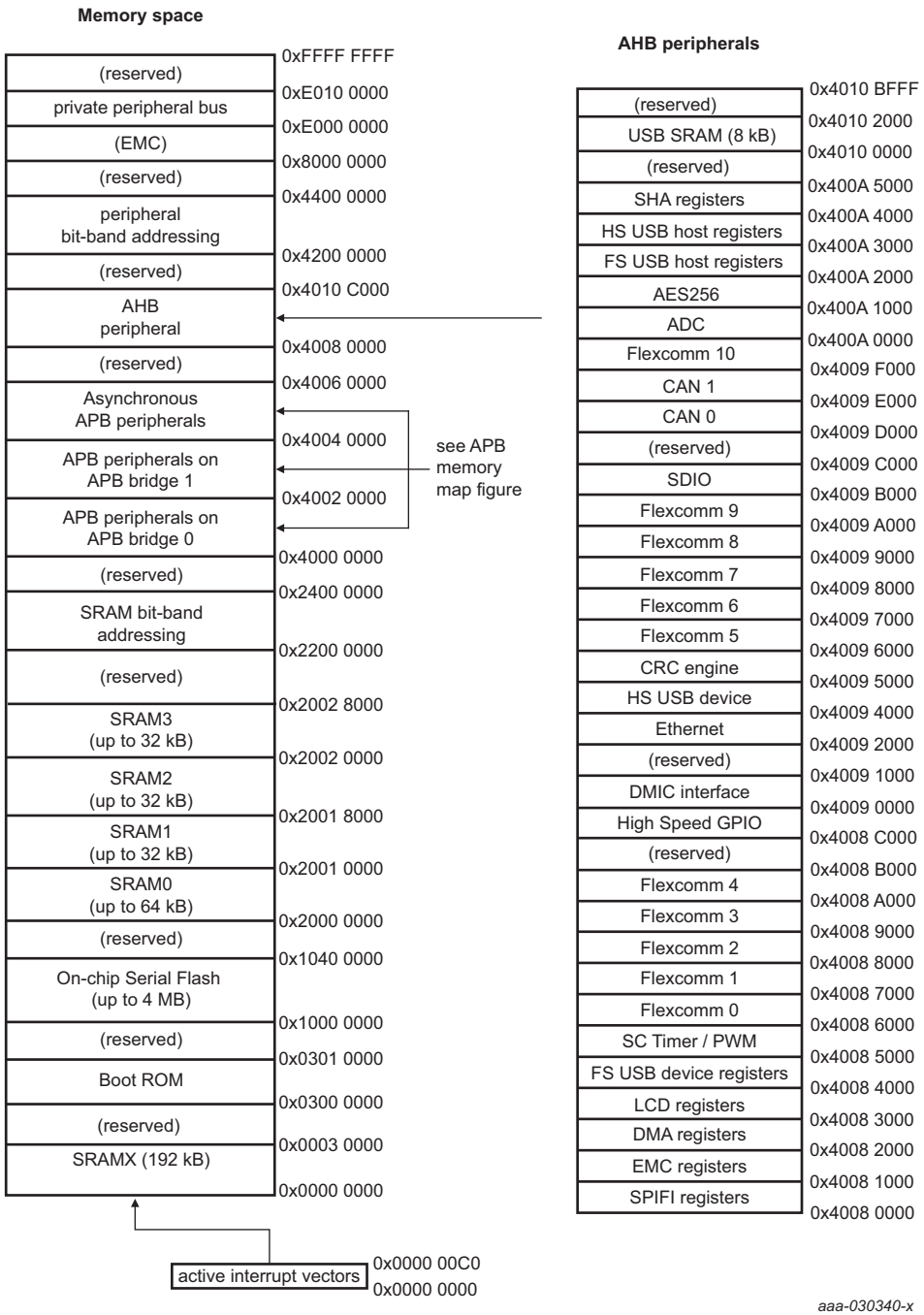

The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

Fig 4. LPC54018JxM/LPC54S018JxM Memory mapping

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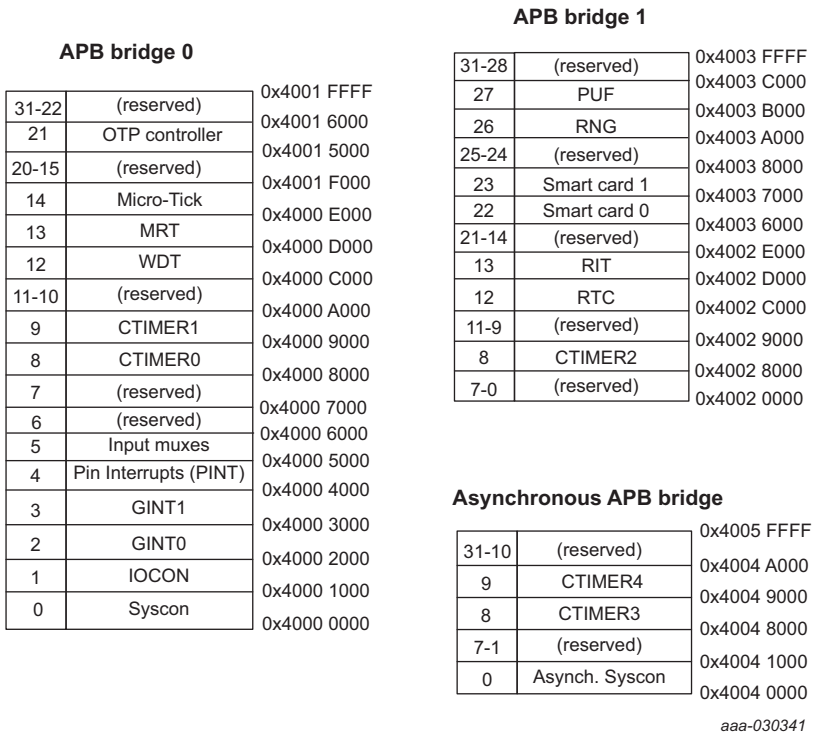

Fig 5. LPC54018JxM/LPC54S018JxM APB Memory map

7.11 One-Time Programmable (OTP) memory

The OTP memory contains four memory banks of 128 bits each. The first memory bank (OTP Bank 0) is reserved. The other three OTP banks are programmable. In LPC54018Jx devices, OTP banks 1 and 2 are available for storing general purpose data. In LPC54S018Jx devices, OTP banks 1 and 2 are used for storing the AES keys. OTP bank 3 is used for customer programmable device configuration data.

7.11.1 Features

- The OTP memory stores user settings in bank 3, register 0 to configure:
  - ISP and boot source modes
  - Secure boot
  - SPIFI boot delay
  - Customer definable bits
- Root of Trust (RoT) hash digest for secure authenticated boot (OTP Banks 1, 2).
- Scrambled 128-bit AES key for secure encrypted boot (OTP Bank 2).
- USB Vendor and Product IDs (OTP Bank 2).
- Boot ROM API support for programming the OTP memory provided.

Remark: OTP programming requires a supply voltage of at least 3.3 V. To use the OTP API, the main system clock must be running from the 12 MHz clock.

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7.12 System control

7.12.1 Clock sources

The LPC54018JxM/LPC54S018JxM supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.12.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.12.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

7.12.1.3 Crystal oscillator

The LPC54018JxM/LPC54S018JxM include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC54018JxM/LPC54S018JxM will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 6 and Figure 7 for an overview of the LPC54018JxM/LPC54S018JxM clock generation.

7.12.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

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7.12.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

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7.12.5 Clock Generation

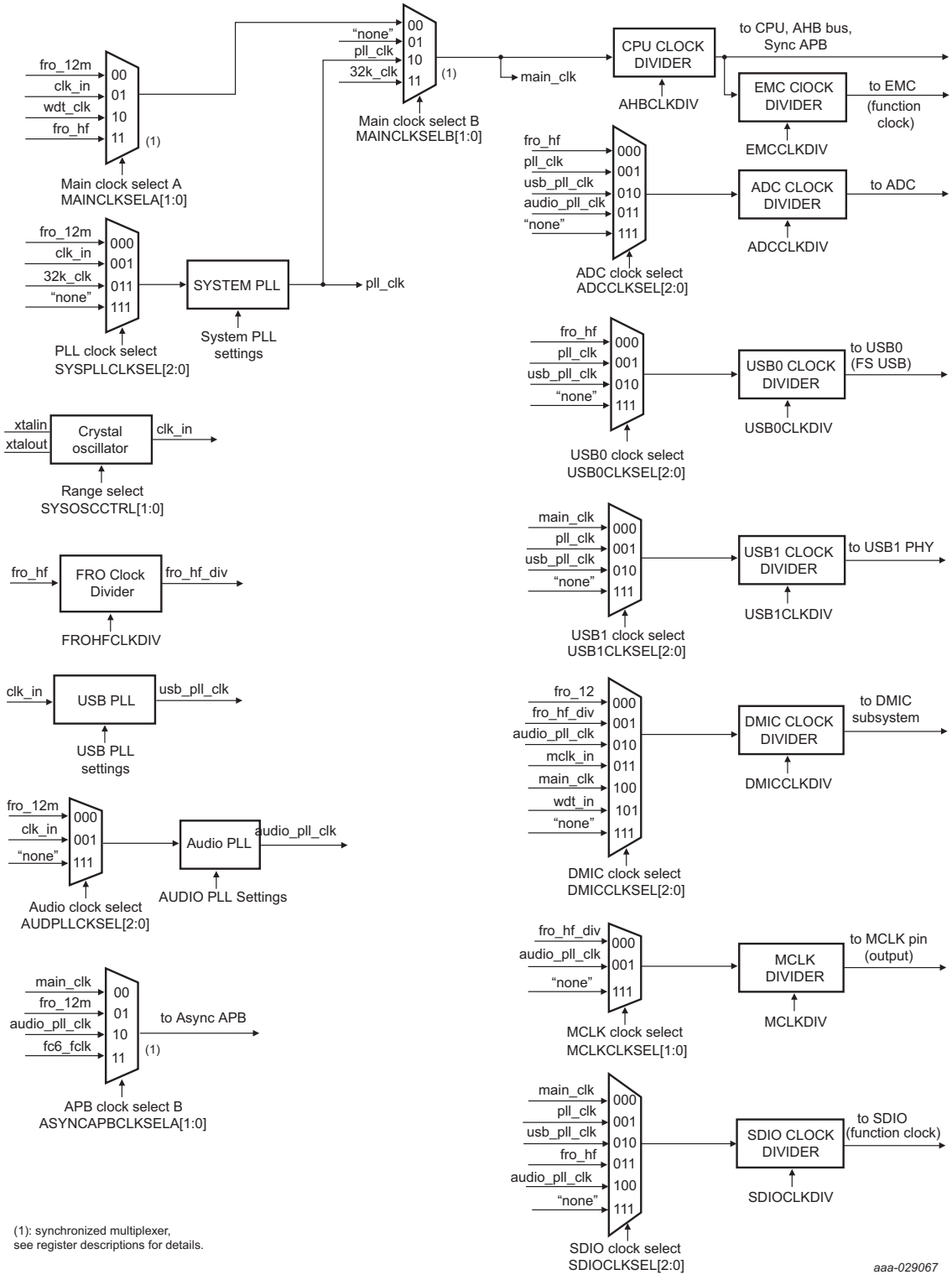

Fig 6. LPC54018JxM/LPC54S018JxM clock generation

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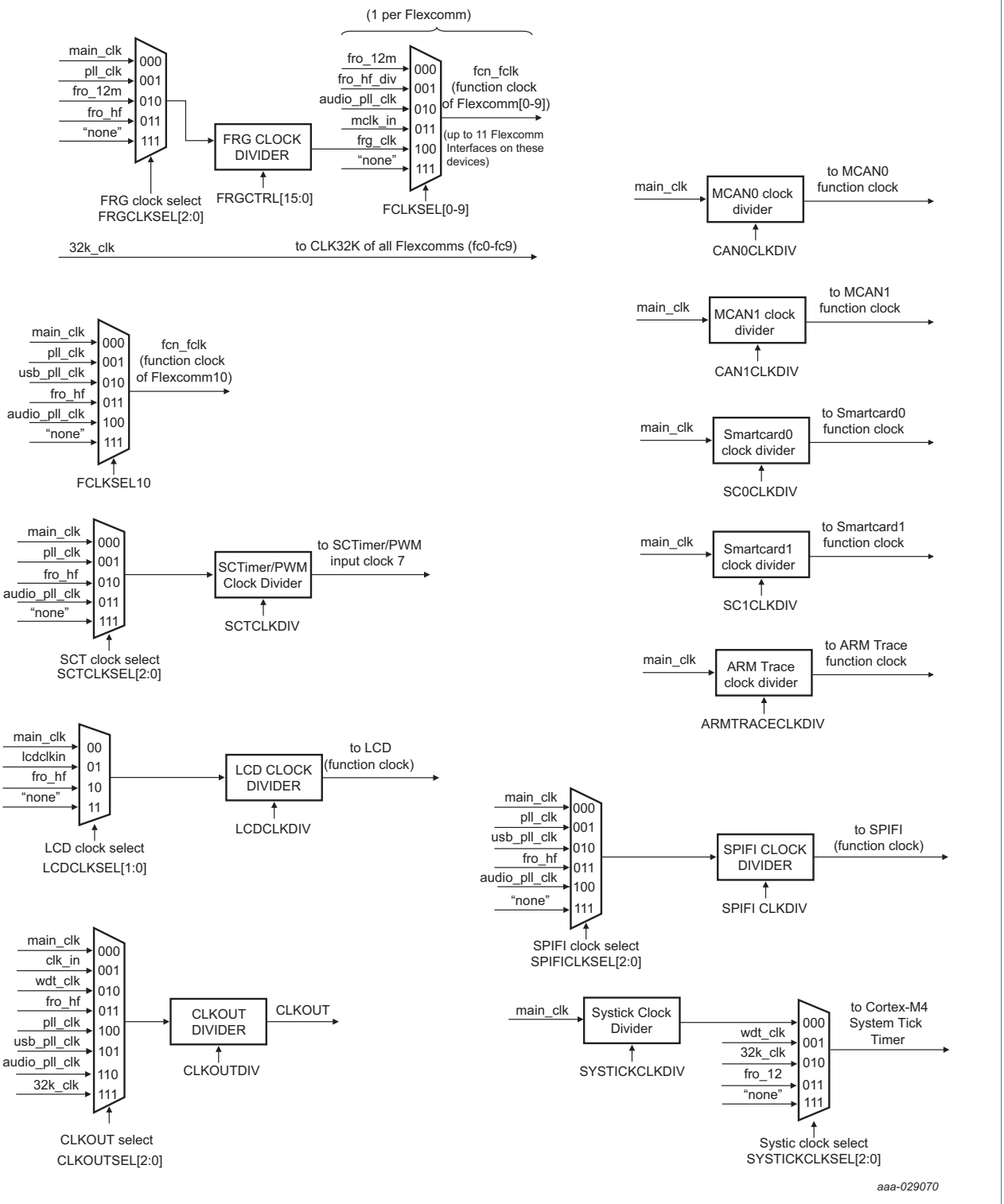

Fig 7. LPC54018JxM/LPC54S018JxM clock generation (continued)

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7.12.6 Brownout detection

The LPC54018JxM/LPC54S018JxM includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold level can be selected to cause chip reset.

7.12.7 Safety

The LPC54018JxM/LPC54S018JxM includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.13 Power control

The LPC54018JxM/LPC54S018JxM support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are three special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode that can be activated using the power API library from the SDK software package.

7.13.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.13.2 Deep-sleep mode

In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled by default. The FRO is disabled.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

GPIO Pin Interrupts, GPIO Group Interrupts, and selected peripherals such as USB0, USB1, DMIC, SPI, I2C, USART, WWDT, RTC, Micro-tick Timer, and BOD can be left running in deep sleep mode The FRO, RTC oscillator, and the watchdog oscillator can be left running.In some cases, DMA can operate in deep-sleep mode.

7.13.3 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the $\overline{\text{RESET}}$ pin. The LPC54018JxM/LPC54S018JxM can wake up from deep power-down mode via the $\overline{\text{RESET}}$ pin and the RTC alarm. The ALARM1HZ flag in RTC

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control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations.	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB0	Software configured	Software configured	Off
USB1	Software configured	Software configured	Off
Ethernet	Software configured	Off	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

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Table 9 shows wake-up sources for reduced power modes.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.
Deep-sleep	Pin interrupts	Enable pin interrupts in NVIC and STARTER0 and/or STARTER1 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTER0 registers. • Enable interrupt in BODCTRL register. • Configure the BOD to keep running in this mode with the power API.
	BOD reset	Enable reset in BODCTRL register.
	Watchdog interrupt	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog interrupt in NVIC and STARTER0 registers. • Enable the watchdog in the WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • Configure the WDTOSC to keep running in this mode with the power API.
	Watchdog reset	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog and watchdog reset in the WWDT MOD register and feed.
	Reset pin	Always available.
	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register. • Enable the RTCALARM interrupt in the STARTER0 register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTC CTRL register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC. • Enable the RTC wake-up interrupt in the STARTER0 register.
	Micro-tick timer (intended for ultra-low power wake-up from deep-sleep mode	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the Micro-tick timer clock by writing to the AHBCLKCTRL1 register. • Start the Micro-tick timer by writing UTICK CTRL register. • Enable the Micro-tick timer interrupt in the STARTER0 register.
	I2C interrupt	Interrupt from I2C in slave mode.
	SPI interrupt	Interrupt from SPI in slave mode.
	USART interrupt	Interrupt from USART in slave or 32 kHz mode.
	USB0 need clock interrupt	Interrupt from USB0 when activity is detected that requires a clock.
	USB1 need clock interrupt	Interrupt from USB1 when activity is detected that requires a clock.
	Ethernet interrupt	Interrupt from ethernet.
	DMA interrupt	Interrupt from DMA.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.

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Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Deep power-down	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTC CTRL register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC.
	Reset pin	Always available.

7.14 General Purpose I/O (GPIO)

The LPC54018JxM/LPC54S018JxM provides a total of 137 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

7.14.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.15 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

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7.15.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.16 Serial peripherals

7.16.1 Full-speed USB Host/Device interface (USB0)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.16.1.1 USB0 device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Supports 10 physical (5 logical) endpoints including two control endpoints.
- Single and double-buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from reduced power mode on USB activity and remote wake-up.
- Supports SoftConnect.
- Link Power Management (LPM) supported.

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7.16.1.2 USB0 host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

Features

- OHCI compliant.
- Two downstream ports.

7.16.2 High-speed USB Host/Device interface (USB1)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.16.2.1 USB1 device controller

The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Fully compliant with *USB 2.0 Specification* (high speed).
- Supports 8 physical (16 logical) endpoints with up to 8 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- While USB is in the Suspend mode, the LPC54018JxM/LPC54S018JxM can enter one of the reduced power modes and wake up on USB activity.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.16.2.2 USB1 host controller

The host controller enables high speed data exchange with USB devices attached to the bus. It consists of register interface and serial interface engine. The register interface complies with the Enhanced Host Controller Interface (EHCI) specification.

Features

- EHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

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7.16.3 Ethernet AVB

The Ethernet block enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration.

7.16.3.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Supports IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
  - Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.16.4 SPI Flash Interface (SPIFI)

The SPI Flash Interface is connected to the on-chip serial flash in the LPC54018JxM/LPC54S018JxM microcontroller with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

7.16.4.1 Features

- Connected to on-chip serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.

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- Supports DMA access.
- Provides XIP (execute in place) feature to execute code directly from on-chip serial flash.

7.16.5 CAN Flexible Data (CAN FD) interface

The LPC54018JxM/LPC54S018JxM contains two CAN FD interfaces, CAN FD 1 and CAN FD 2.

7.16.5.1 Features

- Conforms with CAN protocol version 2.0 part A, B and ISO 11898-1.
- CAN FD with up to 64 data bytes supported.
- CAN Error Logging.
- AUTOSAR support.
- SAE J1939 support.
- Improved acceptance filtering.

7.16.6 DMIC subsystem

7.16.6.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

7.16.7 Smart card interface

7.16.7.1 Features

- Two DMA supported ISO 7816 Smart Card Interfaces.
- Both asynchronous protocols, T = 0 and T = 1 are supported.

7.16.8 Flexcomm Interface serial communication

7.16.8.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.

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7.16.8.2 SPI serial I/O controller

Features

- Maximum data rates of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. (Flexcomm Interface 0-9).
- Maximum data rates of 50 Mbit/s in master mode and 50 Mbit/s in slave mode for SPI functions (Flexcomm Interface10).
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.16.8.3 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

Features

- All I2Cs support standard, Fast-mode, and Fast-mode Plus with data rates of up to 1 Mbit/s.
- All I2Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Activity on the I2C in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

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7.16.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.16.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC54018JxM/LPC54S018JxM, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

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The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I^2S block in the system level clocking scheme.

Features

- A Flexcomm Interface may implement one or more I^2S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I^2S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (for example, system clock frequency and PLL availability.) but generally supports standard audio data rates.

Remark: The Flexcomm Interface function clock frequency should not be above 48 MHz.

7.17 Digital peripheral

7.17.1 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

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7.17.1.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.17.2 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

7.17.2.1 Features

- Secure Digital memory (SD version 1.1).
- Secure Digital I/O (SDIO version 2.0).
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1).
- MultiMedia Cards (MMC version 4.1).
- Supports up to a maximum of 50 MHz of interface frequency.

7.17.3 External memory controller

The LPC54018JxM/LPC54S018JxM EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

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7.17.3.1 Features

- Read and write buffers to reduce latency and to improve performance.
- Low transaction latency.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- 8/16 data and 16/20/26 address lines wide static memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Dynamic memory interface support including single data rate SDRAM.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- EMC bus width (bit) on TFBGA180 package supports up to 8/16 data line wide static memory.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

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7.17.4 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.17.4.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.18 Counter/timers

7.18.1 General-purpose 32-bit timers/external event counter

The LPC54018JxM/LPC54S018JxM includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.18.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
  - Set LOW on match.
  - Set HIGH on match.

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- Toggle on match.
- Do nothing on match.

- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins may vary by device.)

7.18.2 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.18.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCTimer/PWM states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:

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- 8 inputs
- 10 outputs
- 16 match/capture registers
- 16 events
- 16 states

- PWM capabilities including dead time and emergency abort functions

7.18.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.18.3.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the WDOSC as the clock source.

7.18.4 Real Time Clock (RTC) timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.18.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.18.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat and one-shot interrupt modes.

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7.18.6 Repetitive Interrupt Timer (RIT)

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.18.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Can be used for ETM debug time stamping.

7.19 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.19.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

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7.20 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.20.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.21 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

7.22 Security features

The LPC54018JxM/LPC54S018JxM consists of an AES engine (LPC54S018Jx only), a SHA engine, a random number generator, and a key storage block that supports keys stored in OTP or keys from an SRAM based PUF (LPC54S018Jx only). Additionally, for each device there is a 128-bit unique device serial number for identification.

7.22.1 SHA-1 and SHA-2

All LPC54018JxM/LPC54S018JxM devices provide on-chip hash support to perform SHA-1 and SHA-2 with 256-bit digest (SHA-256). Hashing is a way to reduce arbitrarily large messages or code images to a relatively small fixed size "unique" number called a digest. The SHA-1 Hash produces a 160 bit digest (5 words), and the SHA-256 hash produces a 256 bit digest (8 words).

7.22.1.1 Features

- Performs SHA-1 and SHA-2(256) based hashing.

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- Used with HMAC to support a challenge/response or to validate a message.

7.22.2 AES encryption/decryption

The LPC54S018Jx devices provide an on-chip hardware AES encryption and decryption engine to protect the image content and to accelerate processing for data encryption or decryption, data integrity, and proof of origin. Data can be encrypted or decrypted by the AES engine using the scrambled key from the OTP or a software supplied key.

7.22.2.1 Features

- Encryption and Decryption of data.
- Secure storage of AES key that cannot be read.
- AES engine peak performance of 0.5 bytes/clock cycle.
- GF128 Hash Engine.
- AES engine supports 128, 192 or 256-bit key in:
  - Electronic Codebook (ECB) mode.
  - Cipher Block Chaining (CBC) mode.
  - Cipher Feedback (CFB) mode.
  - Output Feedback (OFB) mode.
  - Counter (CTR) mode.
  - Galois/Counter Mode (GCM).
- The AES engine is compliant with the FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard (AES).
- Data is processed in little endian mode. This means that the first byte read from memory is integrated into the AES codeword as least significant byte. The 16th byte read from memory is the most significant byte of the first AES codeword.
- DMA transfers supported through the DMA controller.

7.22.3 PUF

The PUF controller on the LPC54S018Jx provides a secure key storage without injecting or provisioning device unique PUF root key.The PUF block can generate, store, and reconstruct key sizes from 64 to 4096 bits.

7.22.3.1 PUF keys

The PUF controller provides secure key storage without storing the key. This is done by using the digital fingerprint of a device derived from SRAM. Instead of storing the key, a Key Code is generated, which in combination with the digital fingerprint is used to reconstruct keys that are routed to the AES engine or for use by software. The PUF controller provides generation and secure storage for keys.

7.22.3.2 PUF controller features

The PUF controller has the following features:

- Key strength of 256 bits.

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  - The PUF constructs 256-bit strength device unique PUF root key using the digital fingerprint of a device derived from SRAM and error correction data called Activation Code (AC). The Activation Code is generated during enrollment process. The Activation Code should be stored on external non-volatile memory device in the system.
- Generation, storage, and reconstruction of keys.
- Key sizes from 64 to 4096 bits.
  - PUF controller allows storage of keys, generated externally or on chip, of sizes 64 to 4096 bits.
  - PUF Controller combines keys with digital fingerprint of device to generate key codes. These key codes should be provided to the controller to reconstruct original key. They can be stored on external non-volatile memory device in the system.
- Key output via dedicated hardware interface or through register interface.
  - PUF controller allows to assign a 4-bit index value for each key while generating key codes. Keys that are assigned index value zero are output through HW bus, accessible to AES engine only. Keys with non-zero index are available through APB register interface.
- 32-bit APB interface.

7.23 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

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8. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	on pin VDD	[2]	-0.5	+4.6	V
V_{DDA}	analog supply voltage	on pin VDDA		-0.5	+4.6	V
V_{BAT}	battery supply voltage	on pin VBAT		-0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP	-	-0.5	+4.6	V
V_I	input voltage	only valid when the V_{DD} > 1.8 V; 5 V tolerant I/O pins	[6][7]	-0.5	+5.0	V
		on I2C open-drain pins	[5]	-0.5	+5.0	V
		USB_DM, USB_DP pins		-0.5	+5.0	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[8][9]	-0.5	VDD	V
I_{DD}	supply current	per supply pin, 2.7 V ≤ V_{DD} < 3.6 V	[3]	-	300	mA
I_{SS}	ground current	per ground pin, 2.7 V ≤ V_{DD} < 3.6 V	[3]	-	300	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	100	mA
T_{stg}	storage temperature		[10]	-65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C
$P_{tot(pack)}$ total power dissipation (per package)		Based on package heat transfer, not device power consumption	[11]	-	0.95	W
		Based on package heat transfer, not device power consumption	[13]	-	1.2	W
V_{ESD}	electrostatic discharge voltage	Human Body Model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 19.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 19) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

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[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

[13] 8-layer (4.5 in × 3 in); still air.

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9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W

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10. Static characteristics

10.1 General operating conditions

Table 12. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	CPU clock frequency			-	-	180	MHz
	CPU clock frequency	For USB high-speed device and host operations		60	-	180	MHz
	CPU clock frequency	For USB full-speed device and host operations		12	-	180	MHz
V_{DD}	supply voltage (core and external rail)			2.7	-	3.6	V
		For OTP programming only	[2]	2.7	-	3.6	V
		For USB Full-Speed operation only		3.0	-	3.6	V
		For USB High-Speed operation only		2.7	-	3.6	V
V_{DDA}	analog supply voltage			2.7	-	3.6	V
V_{BAT}	battery supply voltage			1.71	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.7	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
USB1_AVDD3V3, USB1_AVDDTX3V3	USB1 analog supply			3.0	3.3	3.6	V
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		-0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		-0.5	-	+3.6	V
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	-	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	-	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Attempting to program below 2.7 V will result in unpredictable results and the part might enter an unrecoverable state.

10.2 CoreMark data

Table 13. CoreMark score

T_{amb} = 25°C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[1][3][4][5]	3.38	(Iterations/s) / MHz
	CCLK = 96 MHz	[1][3][4][5]	3.38	(Iterations/s) / MHz
	CCLK = 180 MHz	[2][3][4][5]	3.38	(Iterations/s) / MHz

[1] Clock source FRO. PLL disabled.

[2] Clock source 12 MHz FRO. PLL enabled.

[3] Characterized through bench measurements using typical samples.

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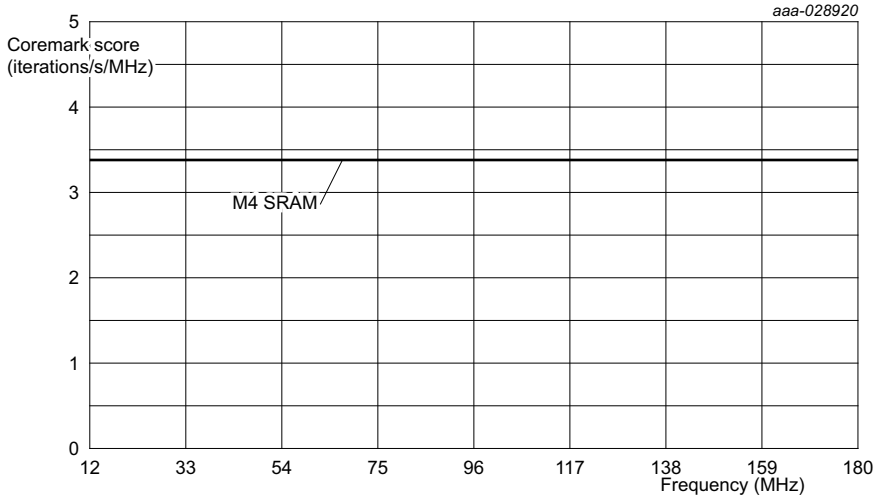
[4] Compiler settings: IAR C/C++ Compiler for Arm ver 8.22.2, optimization level 3, optimized for time on.

[5] SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, and 180 MHz: FRO enabled; PLL enabled.
CoreMark score from SRAMX: SRAM0 is powered.

Fig 8. Typical CoreMark score ((iterations/s)/MHz) vs. Frequency (MHz) from SRAMX

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10.3 Power consumption

Power measurements in Active, sleep, and deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 14. Static characteristics: Power consumption in active and sleep mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified.2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Active mode							
I_{DD}	supply current	CoreMark code executed from SRAMX:					
		CCLK = 12 MHz	[2][3][4]	-	3.0	-	mA
		CCLK = 96 MHz	[2][3][4]	-	16.0	-	mA
		CCLK = 180 MHz	[3][4][5]	-	35.0	-	mA
Sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[2][3][4]	-	1.7	-	mA
		CCLK = 96 MHz	[2][3][4]	-	4.1	-	mA
		CCLK = 180 MHz	[3][4][5]	-	8.3	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source FRO. PLL disabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil uVision v.5.23, optimization level 0, optimized for time off.

[5] Clock source FRO. PLL enabled.

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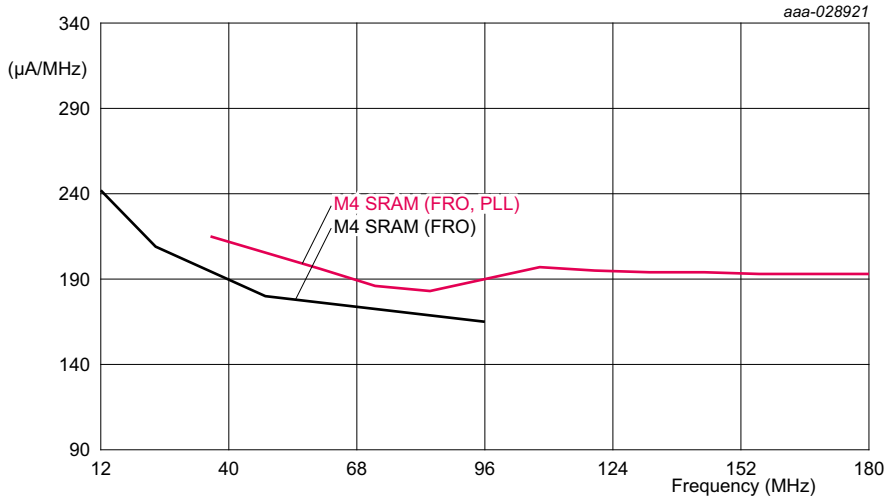

Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Measured with Keil uVision v.5.23. Optimization level 0, optimized for time off.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, and 180 MHz: FRO enabled; PLL enabled.
CoreMark µA/MHz from SRAMX: SRAM0 is powered.

Fig 9. CoreMark power consumption: typical µA/MHz vs. frequency (MHz) SRAMX

Table 15. Static characteristics: Power consumption in deep-sleep and deep power-down modes
T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode:					
		SRAMX (64 KB) powered T_{amb} = 25 °C		-	55	175	µA
		SRAMX (64 KB) powered T_{amb} = 105 °C		-	-	2020	µA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	891	1.6	µA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	42	µA
		RTC oscillator running with external crystal VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	660	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] Tested in production, VDD = 3.6 V.

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Table 16. Static characteristics: Power consumption in deep power-down mode

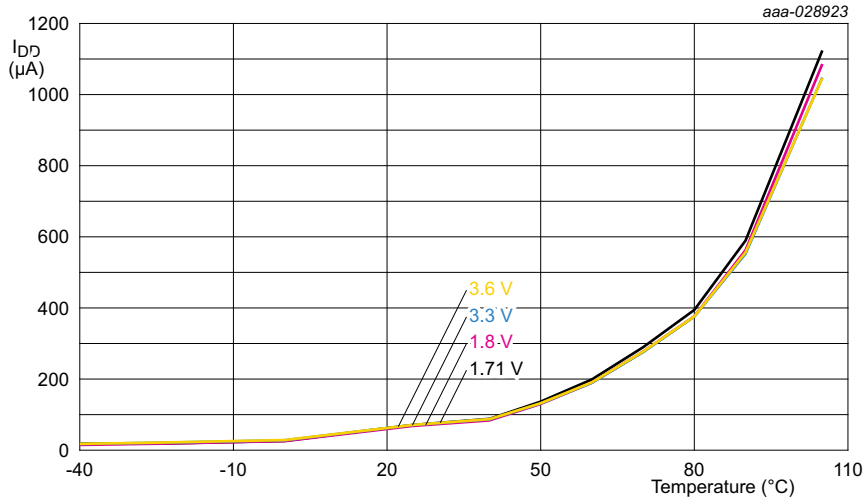
T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
I_{BAT}	battery supply current	deep power-down mode; RTC oscillator running with external crystal					
		VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	0	-	nA
		VDD = VDDA= VREFP = 0 V or tied to ground, VBAT = 3.0 V		-	380[3]	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.



Conditions: BOD disabled; all oscillators and analog blocks disabled; all SRAM disabled except 64 KB SRAMX.

Remark: At hot temperature and below 2.0 V, the supply current increases slightly because of reduction of available RBB (reverse body bias) voltage.

Fig 10. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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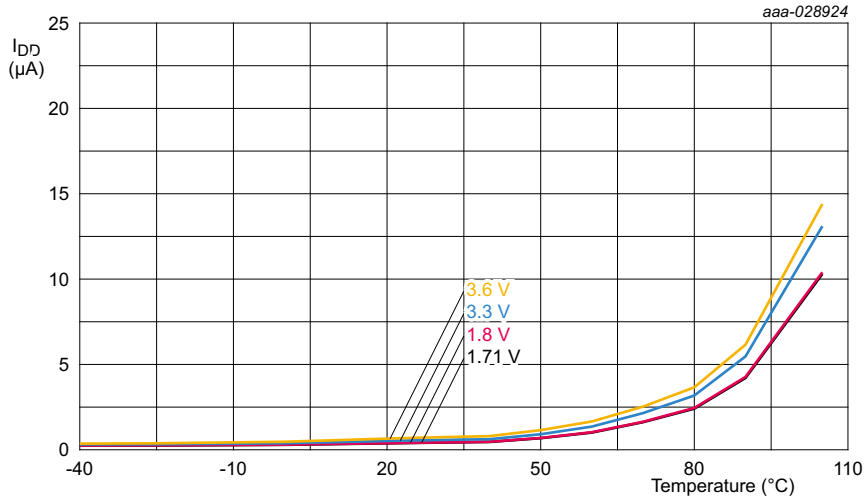

RTC disabled (RTC oscillator input grounded).

Fig 11. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 17 shows the typical peripheral power consumption measured on a typical sample at Tamb = 25 °C and VDD = 3.3 V. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1/2, and PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180MHz.

Table 17. Typical peripheral power consumption[1][2]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO	100
WDT OSC	2.0
BOD	2.0

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		CPU: 12 MHz, sync APB bus: 12 MHz	CPU: 48 MHz, sync APB bus: 48 MHz	CPU: 96 MHz, sync APB bus: 96 MHz	CPU: 180 MHz, sync APB bus: 180 MHz
USB0 device		0.3	0.3	0.3	0.4
USB1 device		4.4	4.4	4.4	5.0
DMIC		0.2	0.2	0.2	0.2
GPIO0	[1]	0.9	0.9	0.9	1.0

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Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
GPIO1	[1]	0.8	0.8	0.8	1.0
GPIO2	[1]	1.0	1.0	1.0	1.1
GPIO3	[1]	1.1	1.1	1.1	1.3
GPIO4	[1]	1.0	1.0	1.0	1.2
GPIO5	[1]	0.7	0.7	0.7	0.8
DMA		0.7	0.7	0.7	0.8
CRC		1.0	1.0	1.0	1.0
ADC0		1.6	1.6	1.6	1.9
SCTimer/PWM		4.5	4.5	4.5	5.3
Ethernet AVB		24.0	24.0	24.0	28.0
LCD		13.0	13.0	13.0	15.0
EMC		39.0	39.0	39.0	45.4
CAN0		10.8	10.8	10.8	12.6
CAN1		10.7	10.7	10.7	12.4
SD/MMC		7.9	7.9	7.9	9.3
Flexcomm Interface 0 (USART, SPI, I^2C)		1.6	1.6	1.6	1.9
Flexcomm Interface1 (USART, SPI, I^2C)		1.6	1.6	1.6	1.8
Flexcomm Interface 2 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9
Flexcomm Interface 3 (USART, SPI, I^2C)		1.4	1.4	1.4	1.6
Flexcomm Interface 4 (USART, SPI, I^2C)		1.4	1.5	1.5	1.7
Flexcomm Interface 5 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9
Flexcomm Interface 6 (USART, SPI, I^2C, I^2S)		2.0	2.0	2.0	2.3
Flexcomm Interface 7 (USART, SPI, I^2C, I^2S)		1.6	1.6	1.6	1.9
Flexcomm Interface 8 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8
Flexcomm Interface 9 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8
Flexcomm Interface 10 (SPI)		1.5	1.5	1.5	1.8
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**
INPUTMUX	[1]	0.83	0.85	0.86	1.0
IOCON	[1]	2.67	2.65	2.65	3.13
PINT		1.1	1.1	1.1	1.3
GINT0 and GINT1		1.33	1.35	1.34	1.52

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Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
WWDT		0.42	0.42	0.42	0.46
RTC		0.3	0.3	0.3	0.3
MRT		0.3	0.3	0.3	0.3
RIT		0.1	0.1	0.1	0.1
UTICK		0.2	0.2	0.2	0.2
CTimer0		0.8	0.8	0.8	0.9
CTimer1		0.8	0.9	0.9	1.0
CTimer2		0.83	0.85	0.88	0.99
Smart card0		2.5	2.5	2.5	2.8
Smart card1		2.5	2.5	2.5	2.8
RNG		1.4	1.4	1.4	1.5
OTP controller		4.0	4.0	4.0	4.5
SHA		1.2	1.2	1.2	1.3
AES		<tbd>	<tbd>	<tbd>	<tbd>
PUF		<tbd>	<tbd>	<tbd>	<tbd>

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Table 18. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz[2]**	**CPU: 96 MHz, Async APB bus: 12 MHz[2]**	**CPU: 180 MHz, Async APB bus: 12 MHz[2]**
Timer3		0.9	0.9	0.9	0.9
Timer4		0.9	0.9	0.9	0.9

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.4 Pin characteristics

Table 19. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 2.7 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} > 1.8 V	[3]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA

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Table 19. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 2.7 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current. Drive HIGH; connected to ground;	2.7 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	87	mA
I_{OLS}	LOW-level short-circuit output current. Drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	µA
		V_I = 5 V	[2]	80		100	µA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	µA
		V_{DD} < V_I < 5 V	[2][7]	6		30	µA
Open-drain I²C pins							
V_{IH}	HIGH-level input voltage	2.7 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	2.7 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	µA
		V_I = 5 V		-	5.5	10	µA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA

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Table 19. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 2.7 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB0_DM and USB0_DP pins							
V_I	input voltage			0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Z_{out}	output impedance		[11]	33.0	-	44	Ω
V_{OH}	HIGH-level output voltage		[12]	2.8	-	-	V
V_{OL}	LOW-level output voltage		[13]	-	-	0.3	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.3$ V	[9][10]	38	-	74	mA
		$V_{OH} = V_{DD} - 0.3$ V	[10][11]	6.0		9.0	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.3$ V	[9][10]	38	-	74	mA
		$V_{OL} = 0.3$ V	[10][11]	6.0		9.0	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	[10]	-	-	100	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	[10]	-	-	100	mA
Pin capacitance							
C_{io}	input/output capacitance	I^2C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[6]	-	-	2.0	pF
		Pins with digital and analog functions	[6]	-	-	7.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[5] To V_{SS}.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the V_{DD} rail and pulls up the I/O pin to the V_{DD} level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Without 33 Ω ± 2 % series external resistor.

[10] The parameter values specified are simulated and absolute values.

[11] With 33 Ω ± 2 % series external resistor.

[12] With 15 KΩ ± 5 % resistor to V_{SS}.

[13] With 1.5 KΩ ± 5% resistor to 3.6 V external pull-up.

[14] Guaranteed by design, not tested in production.

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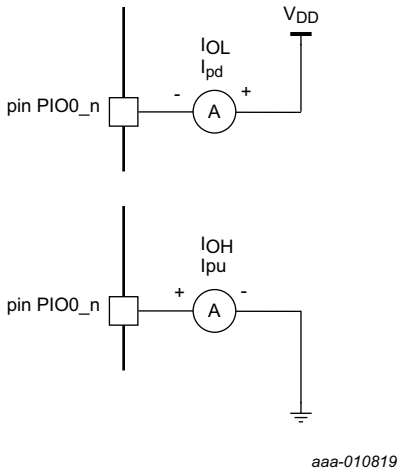
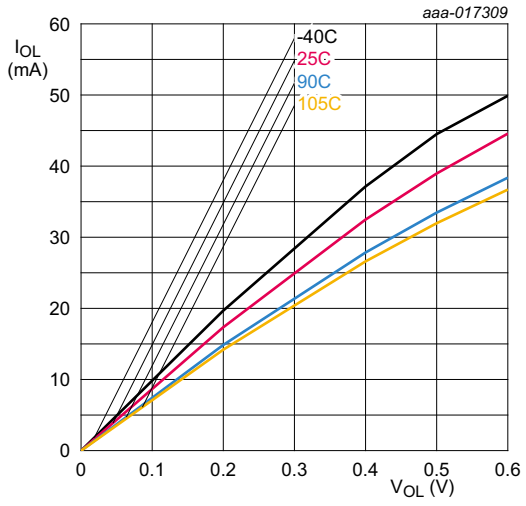
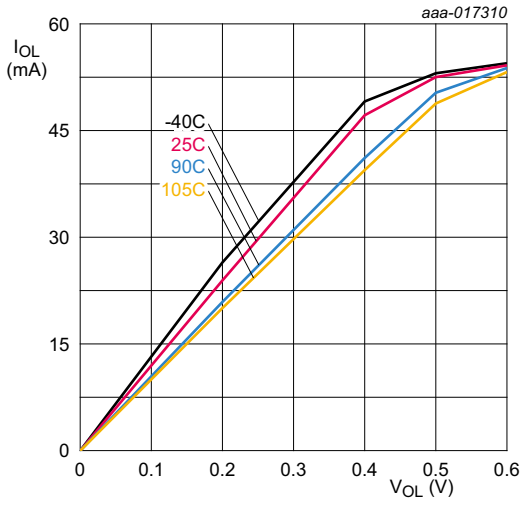


Fig 12. Pin input/output current measurement

10.4.1 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pins PIO0_13 to PIO0_14.



Conditions: V_{DD} = 3.3 V; on pins PIO0_13 to PIO0_16.

Fig 13. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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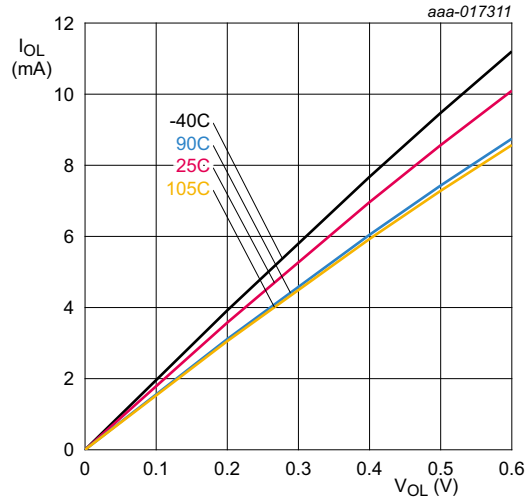
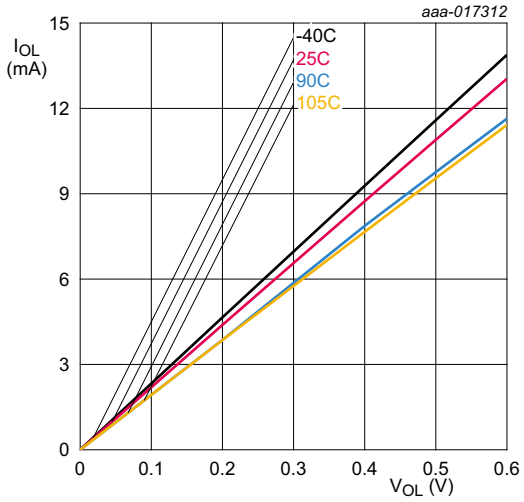
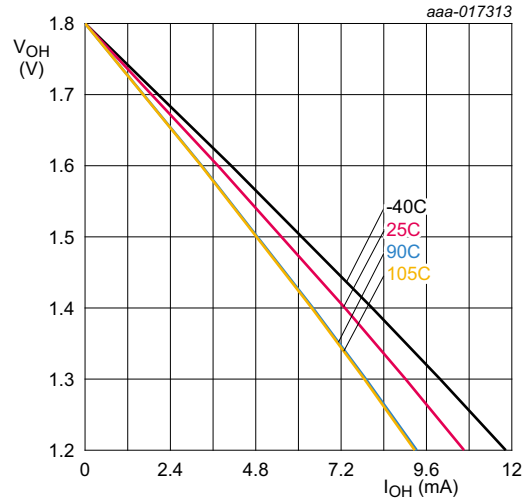


Conditions: V_{DD} = 1.8 V; on standard port pins.

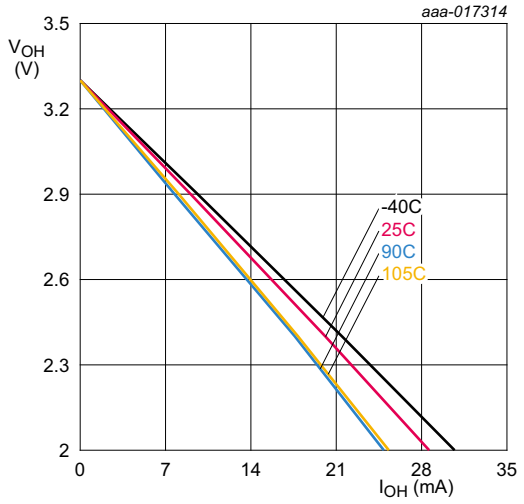


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 14. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 15. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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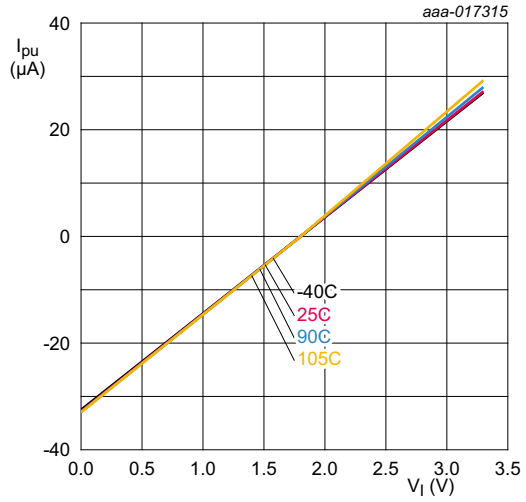
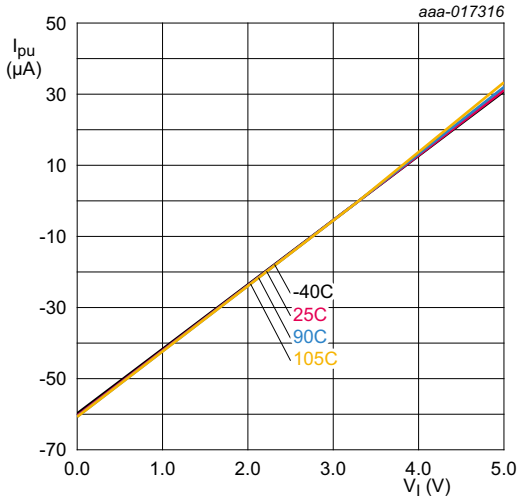
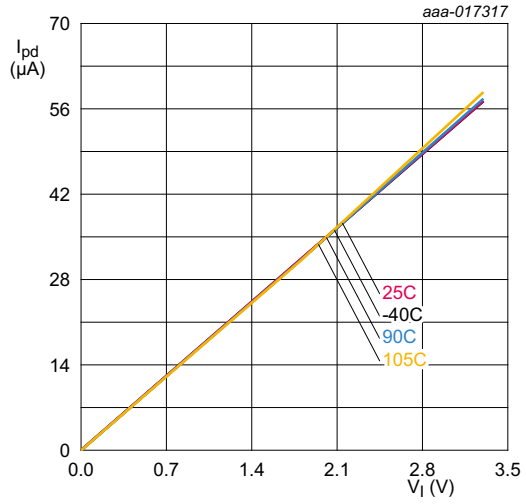


Conditions: V_{DD} = 1.8 V; on standard port pins.

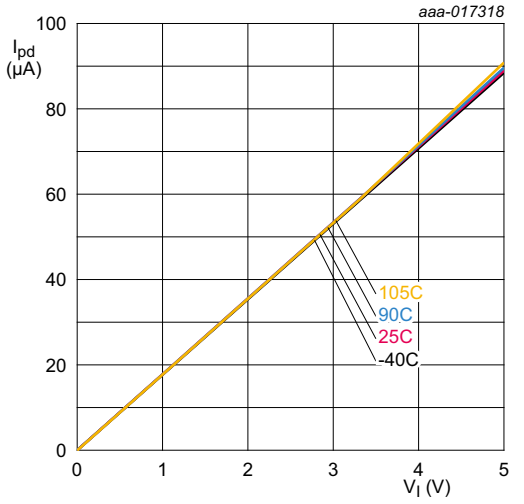


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-down current I_{PD} versus input voltage V_I

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11. Dynamic characteristics

11.1 I/O pins

Table 20. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (Fast-mode); 2.7 V ≤ V_{DD} <= 3.6 V	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; SLEW = 1 (Fast-mode); 2.7 V ≤ V_{DD} <= 3.6 V	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode); 2.7 V ≤ V_{DD} ≤ 3.6 V	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data, not tested in production.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

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11.2 Wake-up process

Table 21. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.0	-	µs
		from deep-sleep mode; SRAMx powered. SRAM0, SRAM1, SRAM2, SRAM3, and USB SRAM powered down.	[2][5]	-	150	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

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11.3 External memory interface

Table 22. Dynamic characteristics: Static external memory interface

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.4+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−1.6	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−6.7 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−4.8	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.8	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1.0	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.6	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.2	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	2.5	-	5.5	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6	-	2.9	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.6	-	0.9	ns

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Table 22. Dynamic characteristics: Static external memory interface *...continued*

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1	[6]	−0.8	-	0	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[6]	0.6	-	0.9	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[2][6]	−0.8	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[2][6]	−1.2 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[2][6]	2.5 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	5.5 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[2][5][6]	−0.8 + $T_{cy(clk)}$	-	$T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[2][6]	0.2 + $T_{cy(clk)}$	-	0.5 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 18 as indicated in the Conditions column.

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM11060* LPC54018JxM/LPC54S018JxM *manual*).

[3] Latest of address valid, $\overline{EMC_CSx}$ LOW, $\overline{EMC_OE}$ LOW, $\overline{EMC_BLSx}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{EMC_CSx}$ HIGH, $\overline{EMC_OE}$ HIGH, $\overline{EMC_BLSx}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{EMC_CSx}$ HIGH, $\overline{EMC_BLSx}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM11060* LPC54018JxM/LPC54S018JxM *manual*).

Table 23. Dynamic characteristics: Static external memory interface

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.5+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−2.3	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−7.9 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns

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Table 23. Dynamic characteristics: Static external memory interface *…continued*

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−5.5	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.7	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time	RD_8	[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.5 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.9	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	−0.1 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	3.1	-	6.7	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6 + $T_{cy(clk)}$	-	2.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.5 +$T_{cy(clk)}$	-	0.8 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1	[6]	−0.8	-	0	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[6]	0.5	-	0.8	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[2][6]	−0.8	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[2][6]	−1.9 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[2][6]	3.1+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	6.7+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[2][5][6]	−0.8 + $T_{cy(clk)}$	-	$T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[2][6]	0.2 + $T_{cy(clk)}$	-	0.5 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 18 as indicated in the Conditions column.

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[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM11060* LPC54018JxM/LPC54S018JxM *manual*).

[3] Latest of address valid, $\overline{\text{EMC_CSx}}$ LOW, $\overline{\text{EMC_OE}}$ LOW, $\overline{\text{EMC_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC_CSx}}$ HIGH, $\overline{\text{EMC_OE}}$ HIGH, $\overline{\text{EMC_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC_CSx}}$ HIGH, $\overline{\text{EMC_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM11060* LPC54018JxM/LPC54S018JxM *manual*).

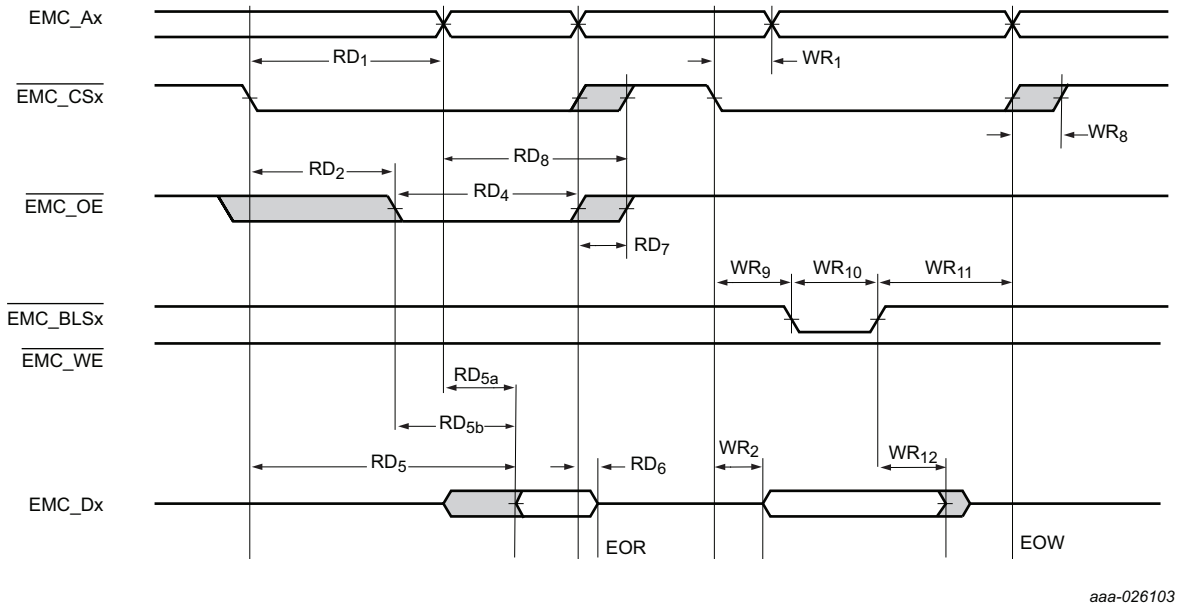

Fig 18. External static memory read/write access (PB = 0)

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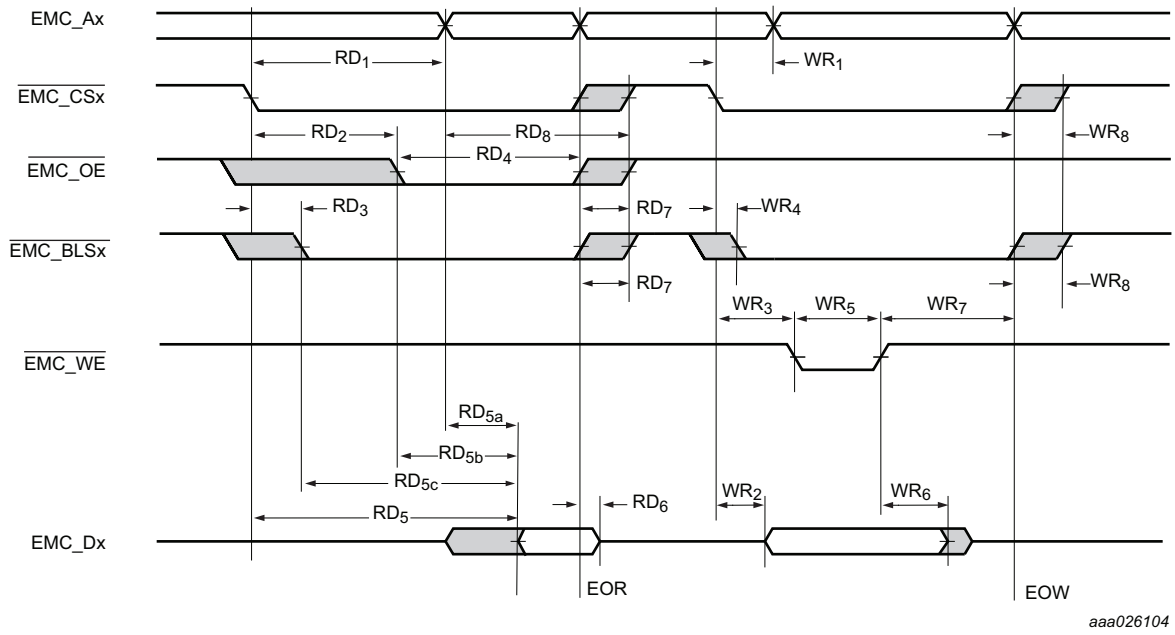

Fig 19. External static memory read/write access (PB =1)

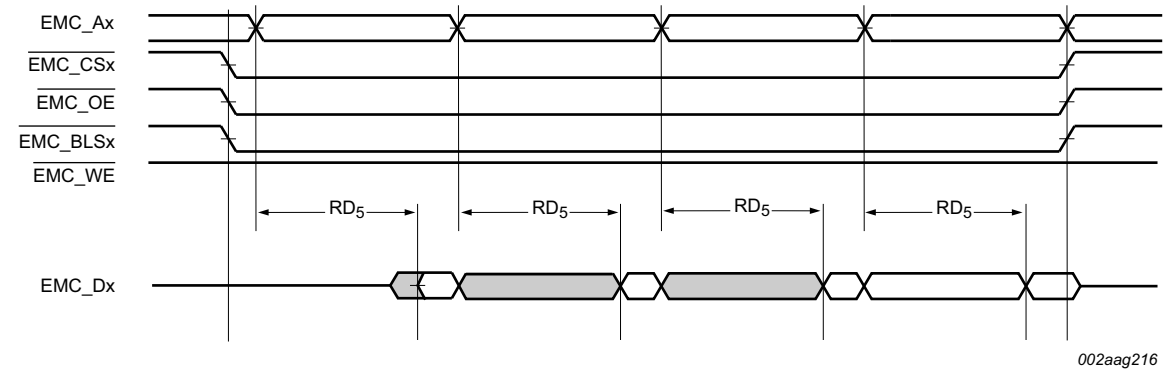

Fig 20. External static memory burst read cycle

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Table 24. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 3.7	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.7	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 4.1	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.8	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 4.4	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.9	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 5.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 4.8	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.7	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	8.1	ns
$t_{h(Q)}$	data output hold time		−1.7	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 26 for internal programmable delay.

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Table 25. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 4.9	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 5.4	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 2.5	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 5.6	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 2.6	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 6.3	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 3.1	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 6.1	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 2.4	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	9.3	ns
$t_{h(Q)}$	data output hold time		−2.4	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 26 for internal programmable delay.

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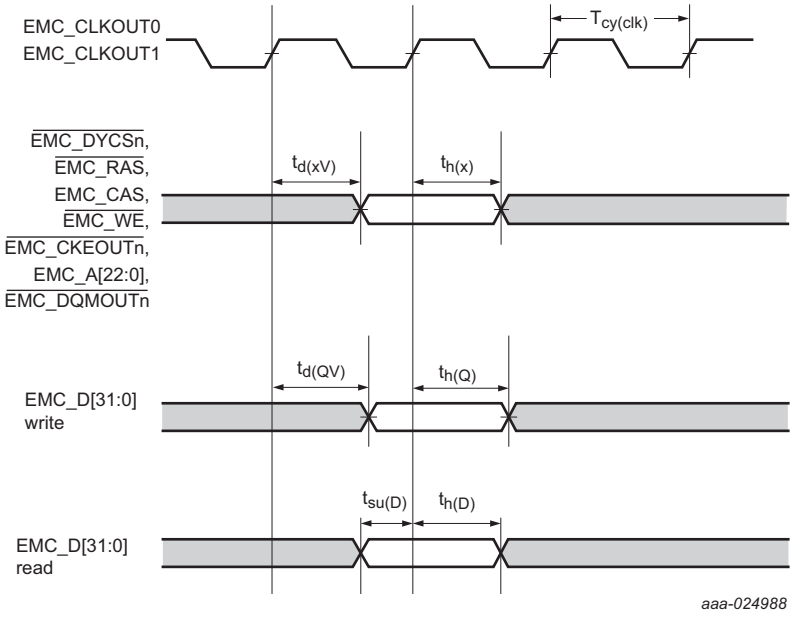

Fig 21. Dynamic external memory interface signal timing

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Table 26. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY)

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}	delay time	b00000	0.41	0.66	0.77	ns
		b00001	0.52	0.85	1.03	ns
		b00010	0.69	1.11	1.3	ns
		b00011	0.8	1.3	1.56	ns
		b00100	0.95	1.53	1.77	ns
		b00101	1.06	1.72	2.03	ns
		b00110	1.23	1.98	2.3	ns
		b00111	1.34	2.17	2.56	ns
		b01000	1.45	2.3	2.67	ns
		b01001	1.56	2.49	2.93	ns
		b01010	1.73	2.75	3.2	ns
		b01011	1.84	2.94	3.46	ns
		b01100	1.99	3.17	3.67	ns
		b01101	2.1	3.36	3.93	ns
		b01110	2.27	3.62	4.2	ns
		b01111	2.38	3.81	4.46	ns
		b10000	2.45	3.86	4.46	ns
		b10001	2.56	4.05	4.72	ns
		b10010	2.73	4.31	4.99	ns
		b10011	2.84	4.5	5.25	ns
		b10100	2.99	4.73	5.46	ns
		b10101	3.1	4.92	5.72	ns
		b10110	3.27	5.18	5.99	ns
		b10111	3.38	5.37	6.25	ns
		b11000	3.49	5.5	6.36	ns
		b11001	3.6	5.69	6.62	ns
		b11010	3.77	5.95	6.89	ns
		b11011	3.88	6.14	7.15	ns
		b11100	4.03	6.37	7.36	ns
		b11101	4.14	6.56	7.62	ns
		b11110	4.31	6.82	7.89	ns
		b11111	4.42	7.01	8.15	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0.

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11.4 System PLL (PLL0)

Table 27. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 2.7 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL0 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]			96	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	2.0	mA
PLL0 configuration: input frequency 32 kHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]	-	-	108	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 28. Dynamic characteristics of the PLL0[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			32.768 kHz	-	25 MHz	
Clock output							
f_o	output frequency	for PLL0 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL0 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at f_{out} = f_{CCO} = 540 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

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11.5 USB PLL (PLL1)

Table 29. PLL1 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 2.7 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL1 configuration: input frequency 12 MHz; output frequency 48 MHz							
$t_{lock(PLL1)}$	PLL1 lock time		[1]	-	7.4	-	µs
$I_{DD(PLL1)}$	PLL1 current	When locked	[1][2]	-	260	-	µA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 30. Dynamic characteristics of the PLL1[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL1 clkout output	[2]	9.75	-	160	MHz
d_o	output duty cycle	for PLL1 clkout output		45	-	55	%
f_{CCO}	CCO frequency			156	-	320	MHz
Dynamic parameters at f_{out} = f_{CCO} = 320 MHz; standard bandwidth settings							
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 4 MHz	[3][4]	-	-	300	ps

[1] Data based on simulation, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.6 Audio PLL (PLL2)

Table 31. PLL2 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 2.7 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	96	µs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	2.0	mA
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	108	µs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

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Table 32. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 540$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	$f_{ref} = 10$ MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	$f_{ref} = 10$ MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.7 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 33. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 Crystal oscillator

Table 34. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

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Table 34. Dynamic characteristic: oscillator *...continued*

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
High-frequency mode (20 - 25 MHz)[5]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] Select Low Frequency range = 0 in the SYSOSCCTRL register.

[5] Select High Frequency = 1 in the SYSOSCCTRL register.

11.9 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to an external clock source.

Table 35. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 2.7 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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11.10 Watchdog oscillator

Table 36. Dynamic characteristics: Watchdog oscillator

T_{amb} = −40 °C to +105 °C; 2.7 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency		[2]	200	-	1500	kHz
D_{clkout}	clkout duty cycle			48	-	52	%
J_{PP-CC}	peak-peak period jitter		[3][4]	-	1	20	ns
t_{start}	start-up time		[4]	-	4	-	µs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

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11.11 I²C-bus

Table 37. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	Both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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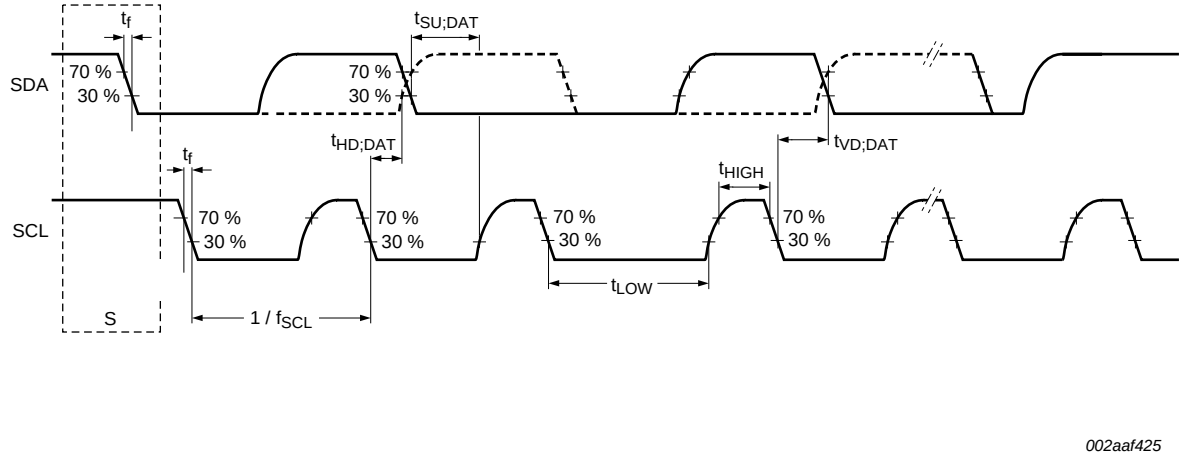

Fig 22. I²C-bus pins clock timing

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11.12 I²S-bus interface

Table 38. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		CCLK > 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		CCLK > 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
Master; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		21.4	-	30.4	ns
		CCLK > 100 MHz		20.6	-	28.7	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		21.1	-	29	ns
		CCLK > 100 MHz		20.3	-	28.3	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		1.3	-	-	ns
		CCLK > 100 MHz		1.0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		2.9	-	-	ns
		CCLK > 100 MHz		3.3	-	-	ns
Slave; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		13.8	-	23.6	ns
		CCLK > 100 MHz		13	-	21.9	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		CCLK > 100 MHz		4.2	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0.9	-	-	ns
		CCLK > 100 MHz		0.7	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		CCLK > 100 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		1.5	-	-	ns
		CCLK > 100 MHz		1.3	-	-	ns

[1] Based on characterization; not tested in production.

[2] Clock Divider register (DIV) = 0x0.

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[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM11060) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

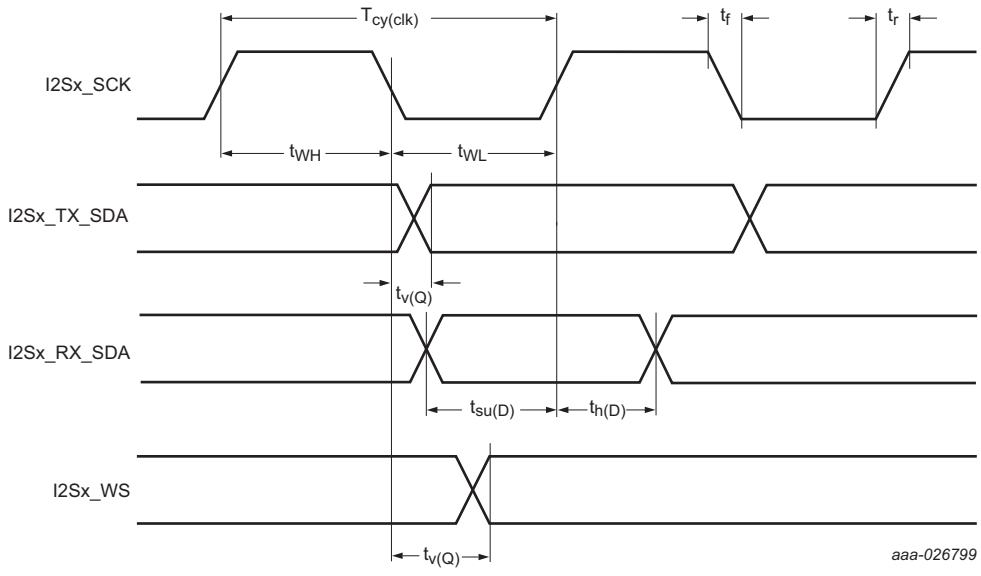

Fig 23. I²S-bus timing (master)

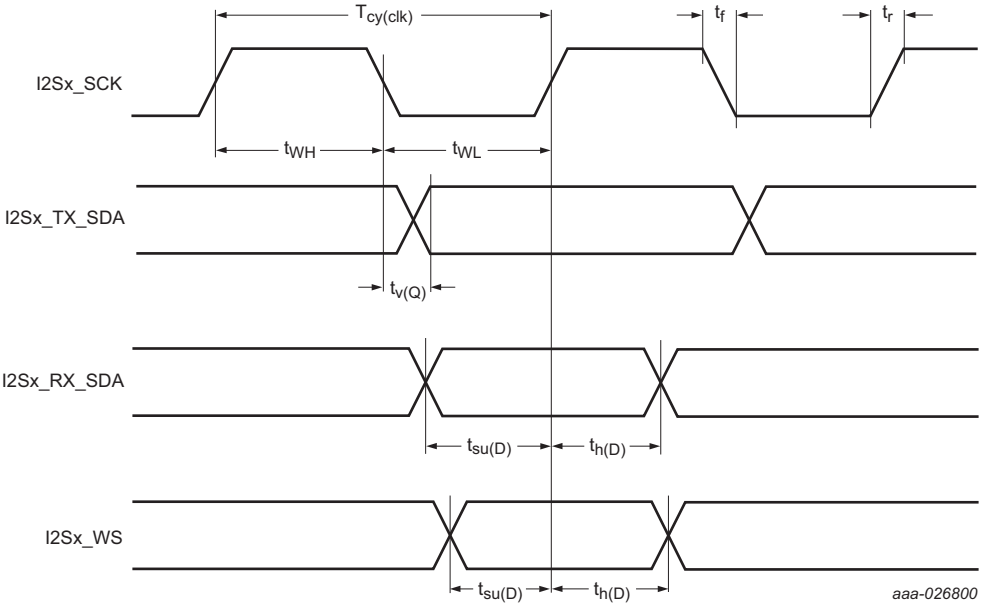

Fig 24. I²S-bus timing (slave)

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11.13 SPI interfaces (Flexcomm Interface 0-9)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 14 Mbit/s.

Table 39. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.4	-	-	ns
		CCLK > 100 MHz		2.2	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		4.2	-	-	ns
		CCLK > 100 MHz		4.5	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		1.8	-	4.6	ns
		CCLK > 100 MHz		1.7	-	4.0	ns
SPI slave 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.2	-	-	ns
		CCLK > 100 MHz		1.0	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		0	-	-	ns
		CCLK > 100 MHz		0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		14	-	23.9	ns
		CCLK > 100 MHz		13.3	-	22.2	ns

[1] Based on characterization; not tested in production.

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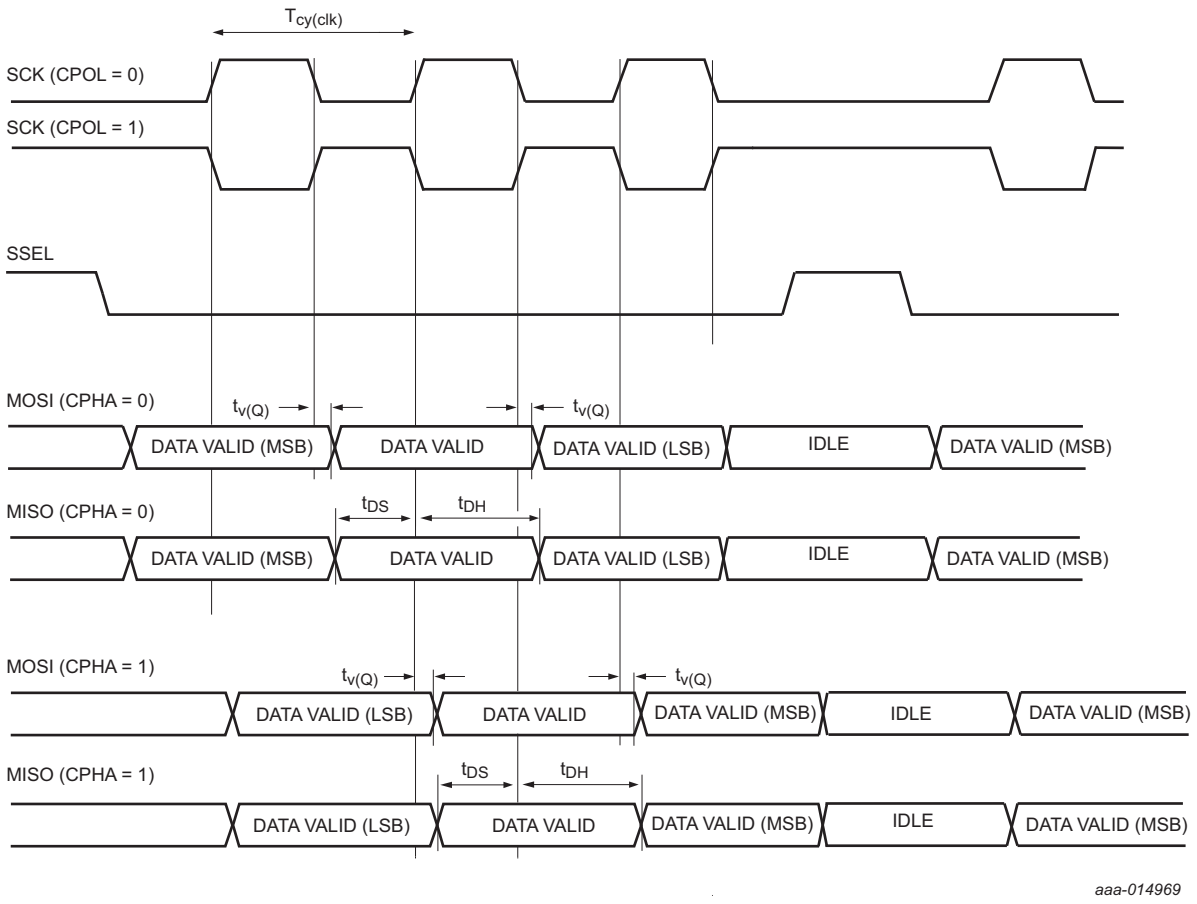

Fig 25. SPI master timing

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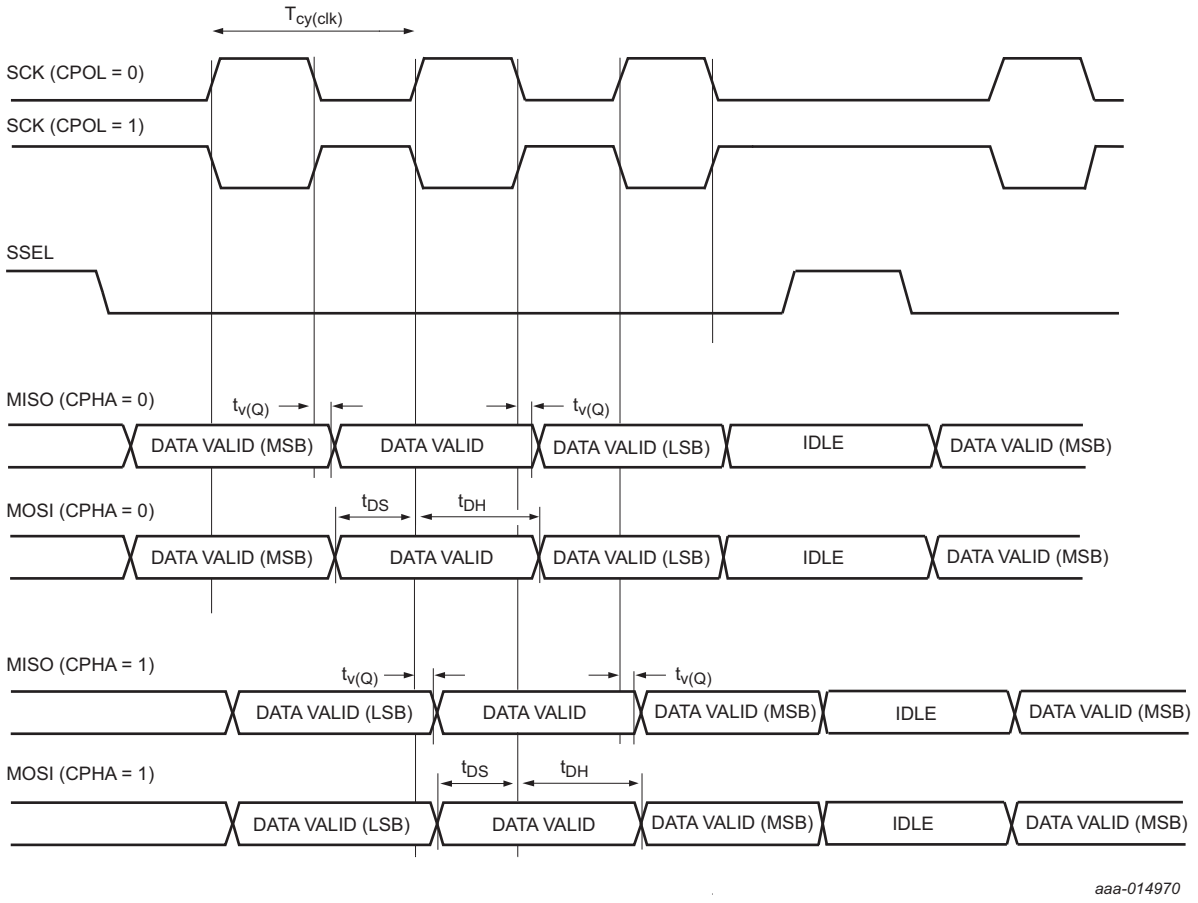

Fig 26. SPI slave timing

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11.14 SPI interfaces (Flexcomm Interface 10)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 50 Mbit/s, and the maximum supported bit rate for SPI slave mode is 50 Mbit/s.

Table 40. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master						
t_{DS}	data set-up time		0	-	-	ns
t_{DH}	data hold time		10.0	-	-	ns
$t_{v(Q)}$	data output valid time		0.8	-	10.0	ns
SPI slave						
t_{DS}	data set-up time		1.2	-	-	ns
t_{DH}	data hold time		10.0	-	-	ns
$t_{v(Q)}$	data output valid time		4.28	-	10.0	ns

[1] Based on characterization; not tested in production.

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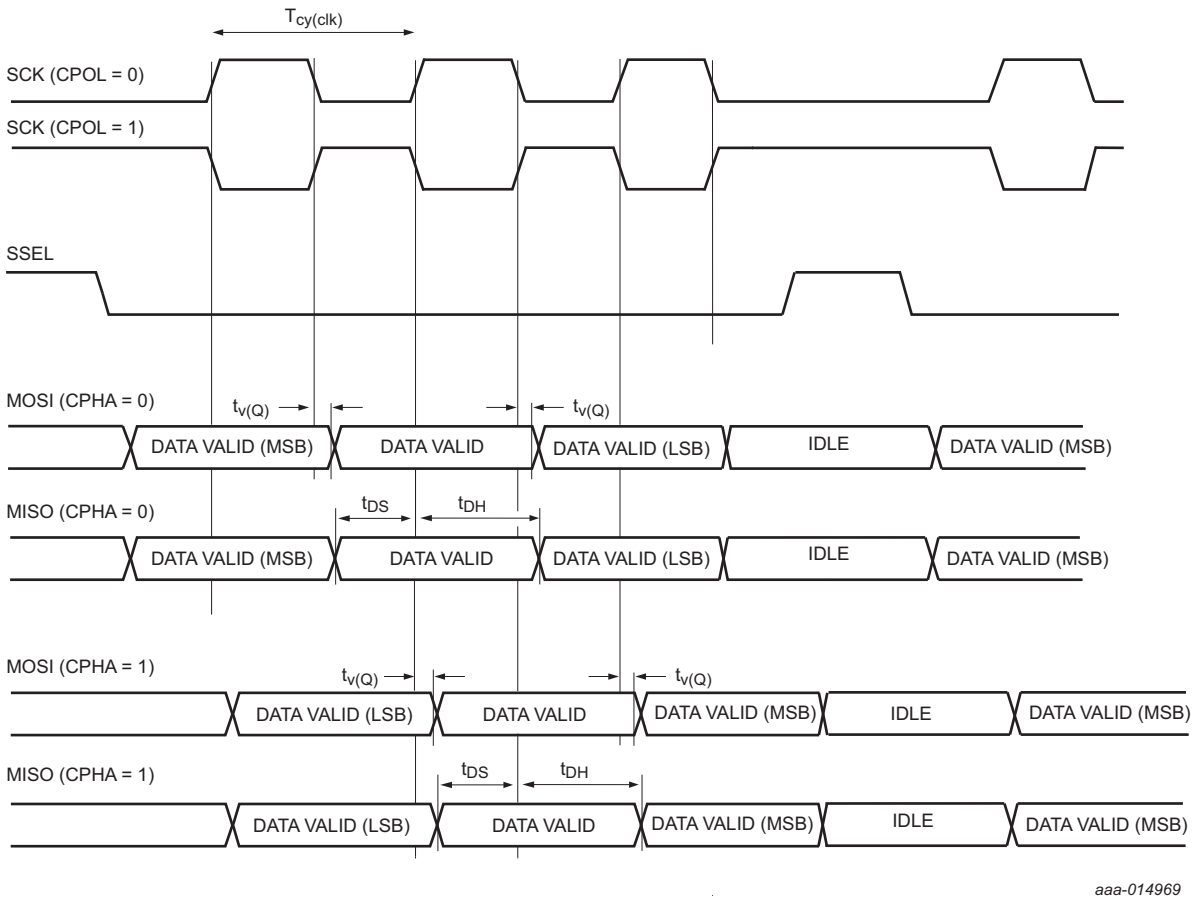

Fig 27. SPI master timing

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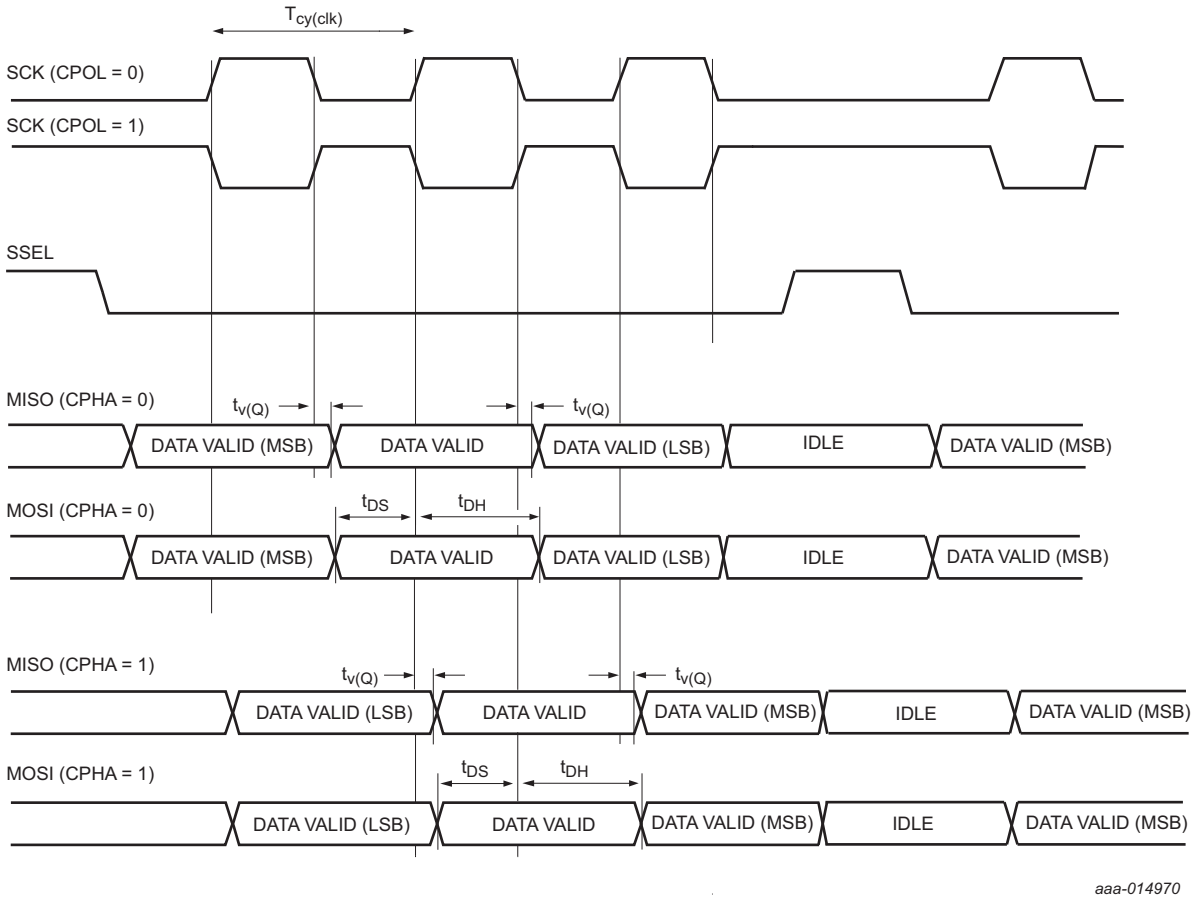

Fig 28. SPI slave timing

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11.15 DMIC subsystem

Table 41. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Bypass bit = 0; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DS}	data set-up time	CCLK ≤ 100 MHz	14.3	-	-	ns
		CCLK > 100 MHz	14.3	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns

[1] Based on simulated values.

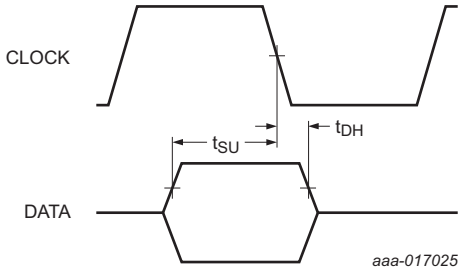

Fig 29. DMIC timing diagram

11.16 Smart card interface

Table 42. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		CCLK > 100 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		CCLK > 100 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

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11.17 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 43. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		CCLK > 100 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		CCLK > 100 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		CCLK > 100 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		CCLK > 100 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

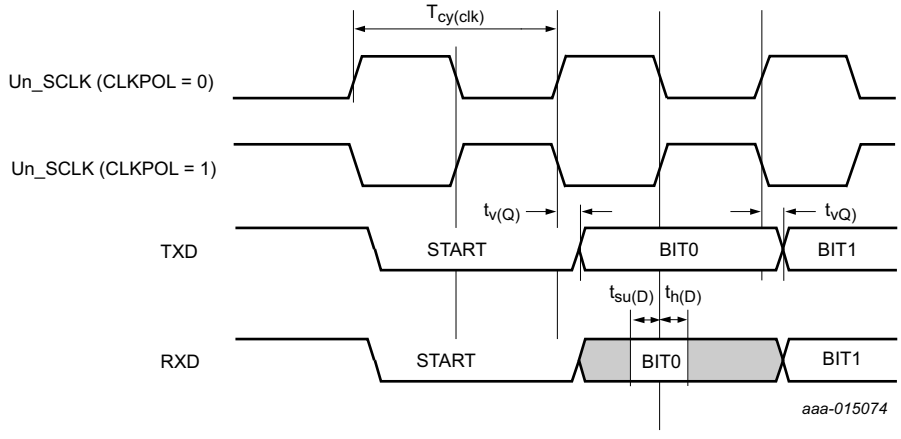

Fig 30. USART timing

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11.18 SCTimer/PWM output timing

Table 44. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 90 % and 10 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	3.4	-	4.5	ns

11.19 USB interface characteristics

Table 45. Dynamic characteristics: USB0 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0		20	ns
t_f	fall time	10 % to 90 %		4.0		20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90		111.11	%
V_{CRS}	output signal crossover voltage			1.3		2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 31		160		175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 31		−2		+5	ns
t_{JR1}	receiver jitter to next transition			−18.5		+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 31	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 31	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

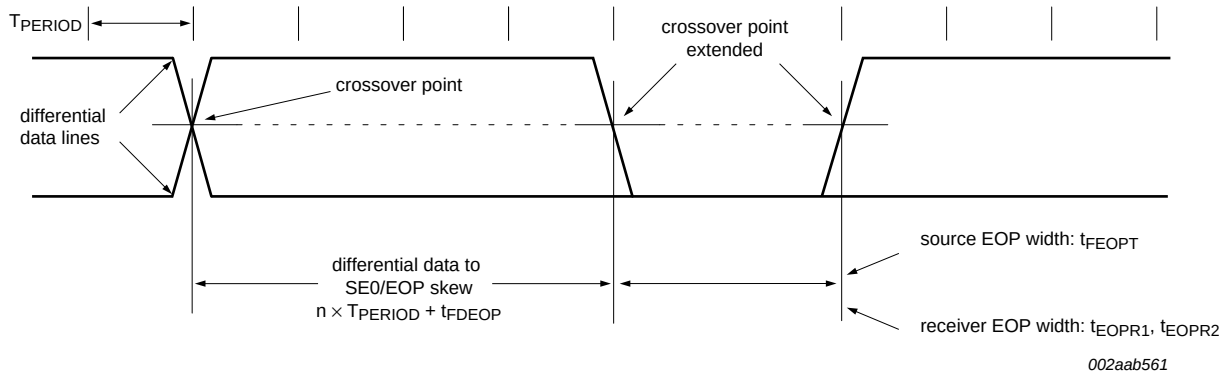

Fig 31. Differential data-to-EOP transition skew and EOP width

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11.21 Ethernet AVB

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

Table 46. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Based on simulation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RMII mode							
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	50.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.4	-	-	ns
		CCLK > 100 MHz		4.4	-	-	ns
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.3	-	0	ns
		CCLK > 100 MHz		−1.3	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN	[1][2]				
		CCLK ≤ 100 MHz		9.9	-	17.3	ns
		CCLK > 100 MHz		9.9	-	17.3	ns
MII mode							
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		CCLK > 100 MHz		4.7	-	-	ns
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.2	-	0	ns
		CCLK > 100 MHz		−1.2	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]				
		CCLK ≤ 100 MHz		10.0	-	18.2	ns
		CCLK > 100 MHz		10.0	-	18.2	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

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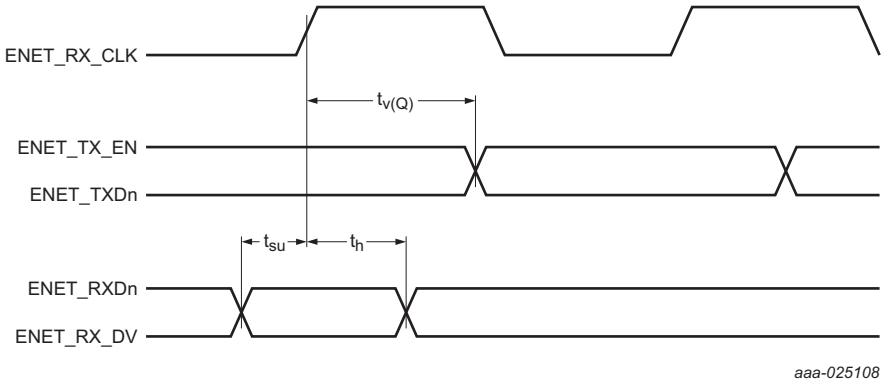

Fig 32. Ethernet RMII timing

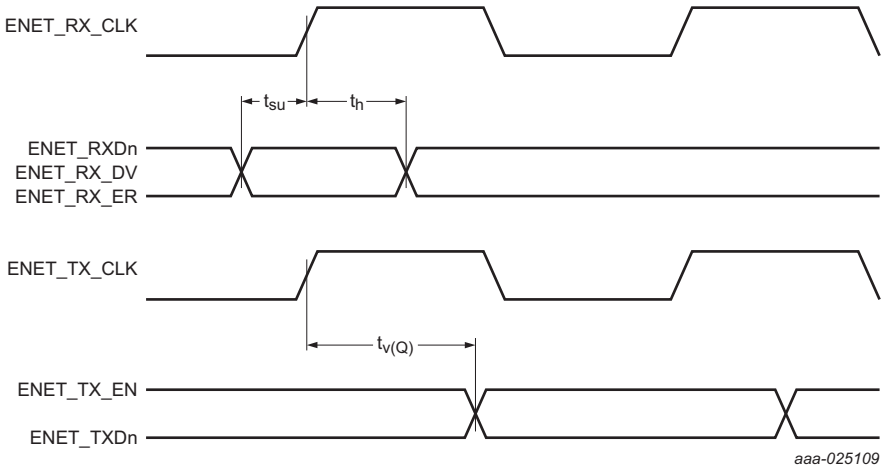

Fig 33. Ethernet MII timing

11.22 SD/MMC and SDIO

Table 47. Dynamic characteristics: SD/MMC and SDIO

T_{amb} = −40 °C to +105 °C, V_{DD} = 2.7 V to 3.6 V; C_L = 20 pF. SAMPLE_DELAY = 0, DRV_DELAY = 0 in the SDDELAY register, SDIOCLKCTRL = 0x84, sampled at 90 % and 10 % of the signal level, SLEW = 1 ns for SD_CLK pin, SLEW = 1 ns for SD_DATn and SD_CMD pins. Simulated values in high-speed mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	-	50	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		CCLK > 100 MHz	14.4	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		CCLK > 100 MHz	14.4	-	-	ns

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Table 47. Dynamic characteristics: SD/MMC and SDIO *…continued*

T_{amb} = −40 °C to +105 °C, V_{DD} = 2.7 V to 3.6 V; C_L = 20 pF. SAMPLE_DELAY = 0, DRV_DELAY = 0 in the SDDELAY register, SDIOCLKCTRL = 0x84, sampled at 90 % and 10 % of the signal level, SLEW = 1 ns for SD_CLK pin, SLEW = 1 ns for SD_DATn and SD_CMD pins. Simulated values in high-speed mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		CCLK > 100 MHz	1.5	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		CCLK > 100 MHz	1.5	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		CCLK > 100 MHz	1.9	-	3.5	ns
		on pins SD_CMD as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		CCLK > 100 MHz	1.9	-	3.5	ns

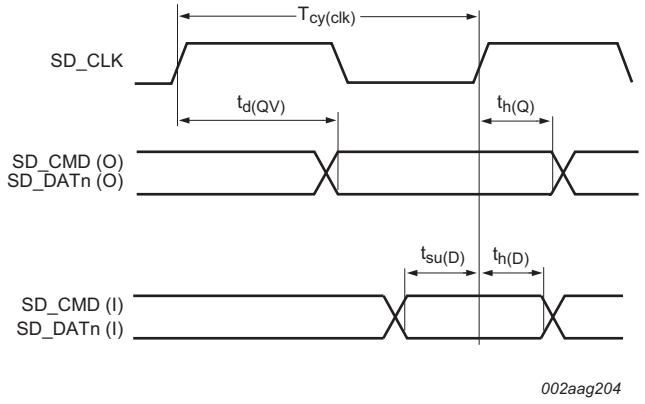

Fig 34. SD/MMC and SDIO timing

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11.23 LCD

Table 48. Dynamic characteristics: LCD

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	-	50	MHz
$t_{v(Q)}$	data output valid time on all LCD output pins	CCLK ≤ 100 MHz	0.9	-	1.6	ns
		CCLK > 100 MHz	0.9	-	1.6	ns

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12. Analog characteristics

12.1 BOD

Table 49. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		1.5	-	1.63	V
		de-assertion		1.55	-	1.69	V
		reset level 0					
		assertion		1.5	-	1.62	V
		de-assertion		1.55	-	1.69	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		1.54	-	1.68	V
		de-assertion		1.6	-	1.75	V
		reset level 1					
		assertion		1.55	-	1.68	V
		de-assertion		1.61	-	1.74	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		1.79	-	1.95	V
		de-assertion		1.85	-	2.02	V
		reset level 2					
		assertion		2.04	-	2.21	V
		de-assertion		2.19	-	2.38	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		2.62	-	2.86	V
		de-assertion		2.77	-	3.03	V
		reset level 3					
		assertion		2.62	-	2.85	V
		de-assertion		2.78	-	3.02	V

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12.2 12-bit ADC characteristics

Table 50. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	5.0	5.3	Msamples/s
E_D	differential linearity error	2.7 V < V_{DDA} ≤ 3.6 V 2.7 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V < V_{DDA} ≤ 3.6 V 2.7 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.7 V < V_{DDA} ≤ 3.6 V 2.7 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 35.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 35.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 35.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 35.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 19 for C_{io}. See Figure 36.

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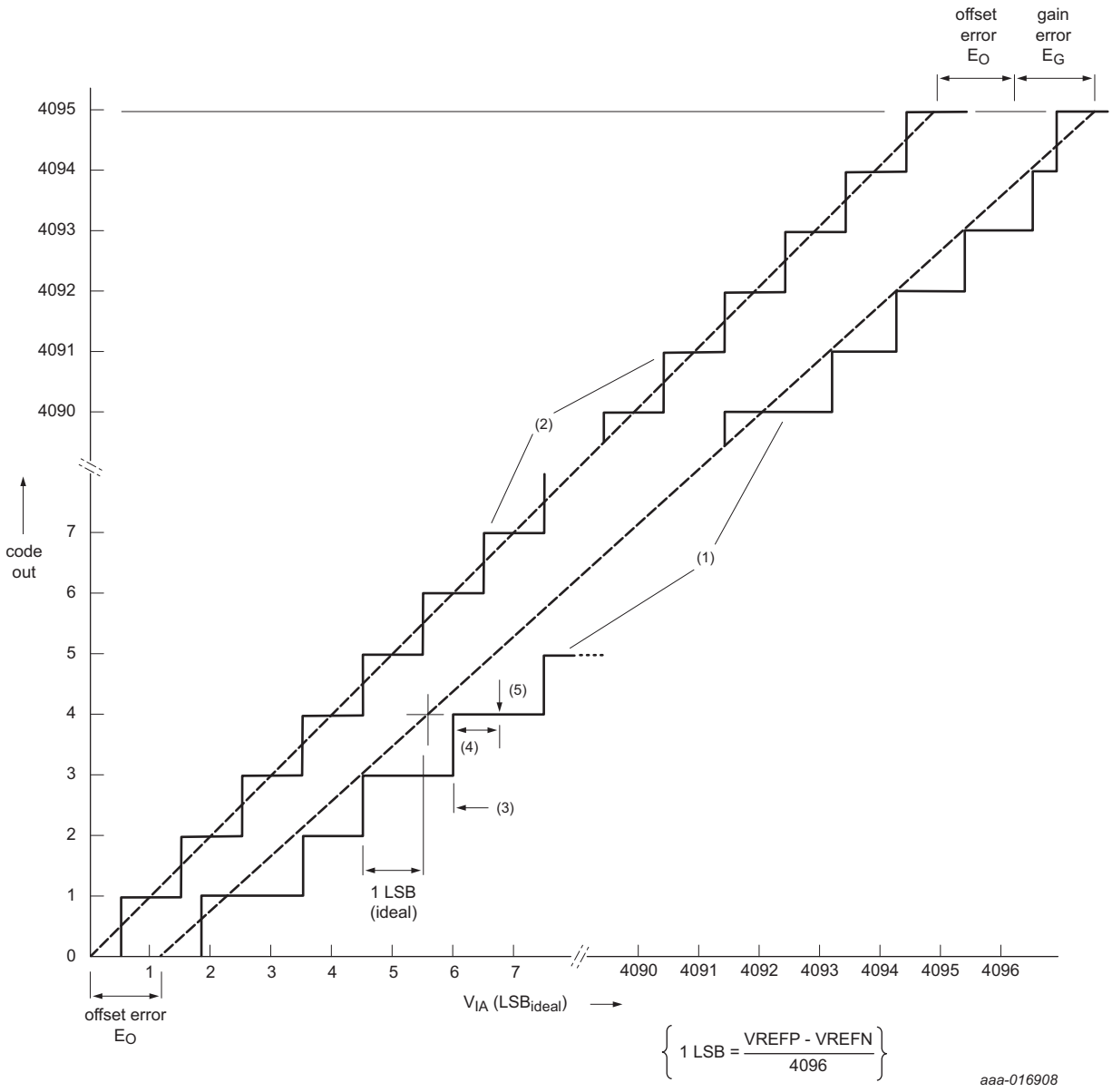

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 35. 12-bit ADC characteristics

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Table 51. ADC sampling times[1]

-40 °C ≤ T_{amb} <= 85 °C; 2.7 V ≤ V_{DDA} ≤ 3.6 V; 2.7 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		47	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		38	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		30	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		22	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		74	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		105	-	-	ns

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Table 51. ADC sampling times[1] *...continued*

-40 °C ≤ T_{amb} <= 85 °C; 2.7 V ≤ V_{DDA} ≤ 3.6 V; 2.7 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		61	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		48	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		36	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

[4] For VDD ≤ 2.5 V, add one additional clock cycle to the values in Table 51.

12.2.1 ADC input impedance

Figure 36 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through R_1 + R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 487 Ω, R_{sw} = 278 Ω
- See Table 19 for C_{io}.
- See Table 50 for C_{ia}.

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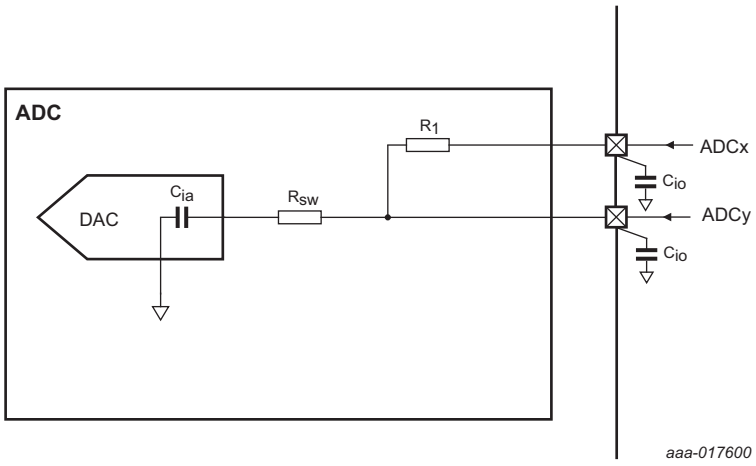

Fig 36. ADC input impedance

12.3 Temperature sensor

Table 52. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 2.7\ V$ *to* $3.6\ V$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = –40 °C to +105 °C	[1]	-		2.56	°C
E_L	linearity error	T_{amb} = –40 °C to +105 °C		-	-	2.56	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

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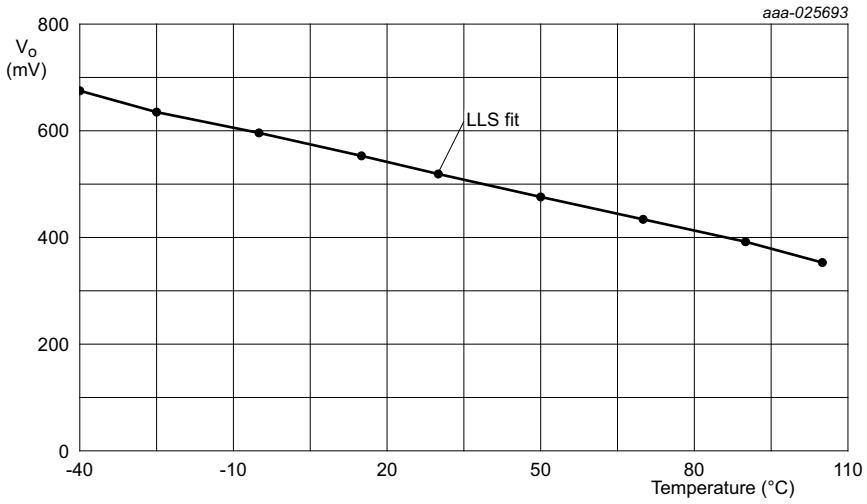
Table 53. Temperature sensor Linear-Least-Square (LLS) fit parameters

V_{DD} = V_{DDA} = 2.7 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	[1]	-	−2.04	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C	[1]	-	584.0	-	mV
Value at 30 °C		[2]	520.3	-	532.7	mV

[1] Measured over typical samples.

[2] Measured for samples over process corners.



V_{DD} = V_{DDA} 3.3 V; measured on matrix samples.

Fig 37. LLS fit of the temperature sensor output voltage

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13. Application information

13.1 Start-up behavior

Figure 38 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

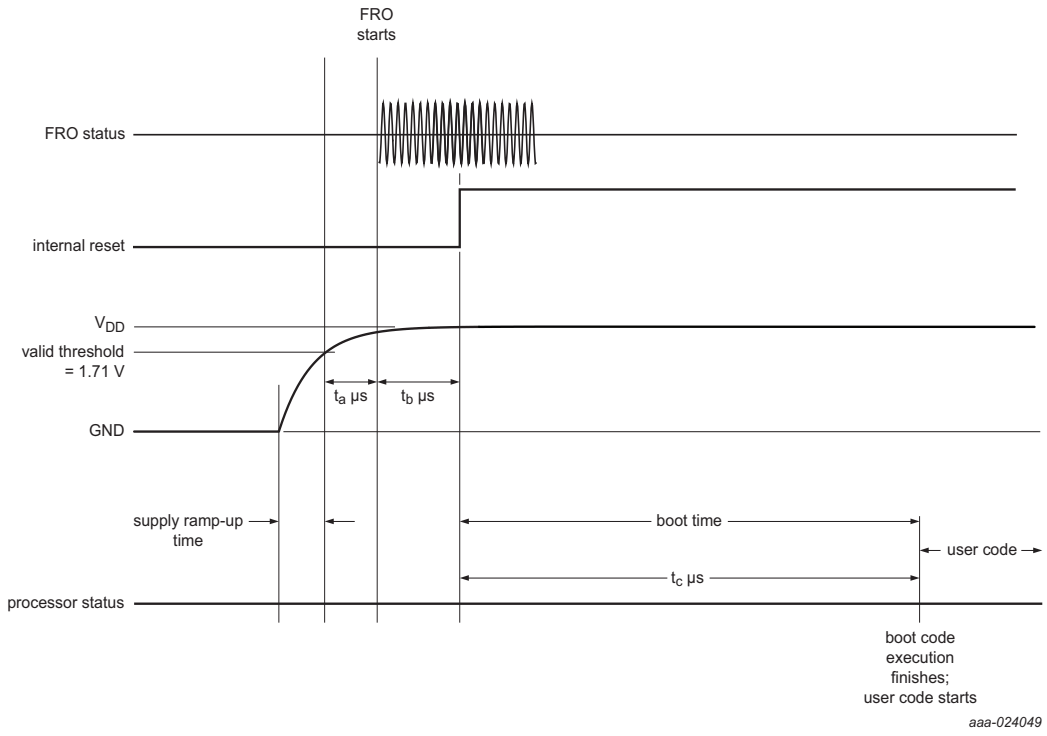

Fig 38. Start-up timing

Table 54. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 20 µs
t_b	Internal reset de-asserted	151 µs

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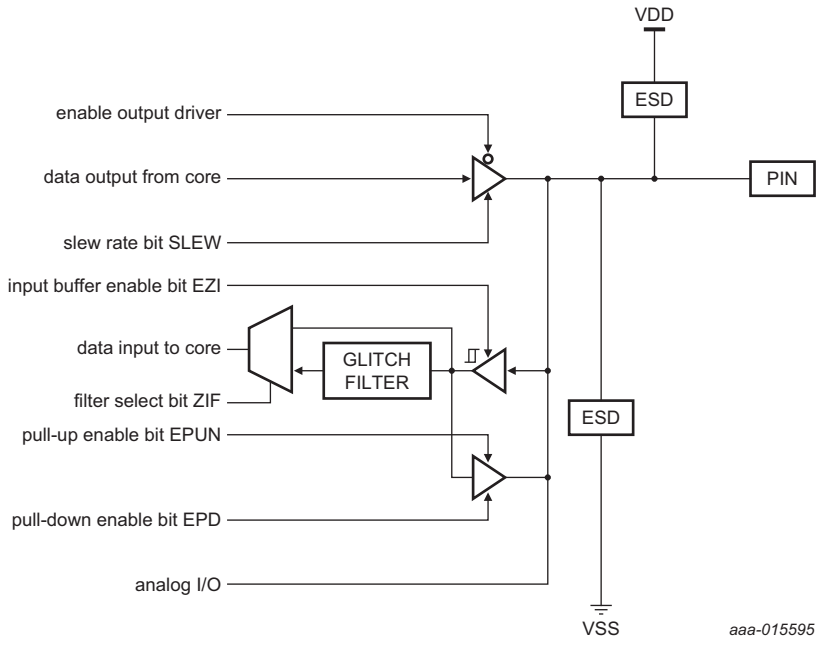
13.2 Standard I/O pin configuration

Figure 39 shows the possible pin modes for standard I/O pins:

- Digital output driver: enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Z mode; High impedance (no cross-bar currents for floating inputs).

Default configuration for the standard I/O pins is Z mode (high impedance; pull-up or pull-down disabled). The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors. GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.



The glitch filter rejects pulses of typical 12 ns width.

Fig 39. Standard I/O and $\overline{\text{RESET}}$ pin configuration

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13.3 Connecting power, clocks, and debug functions

Figure 40 shows the basic board connections used to power the LPC54018JxM/LPC54S018JxM devices, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

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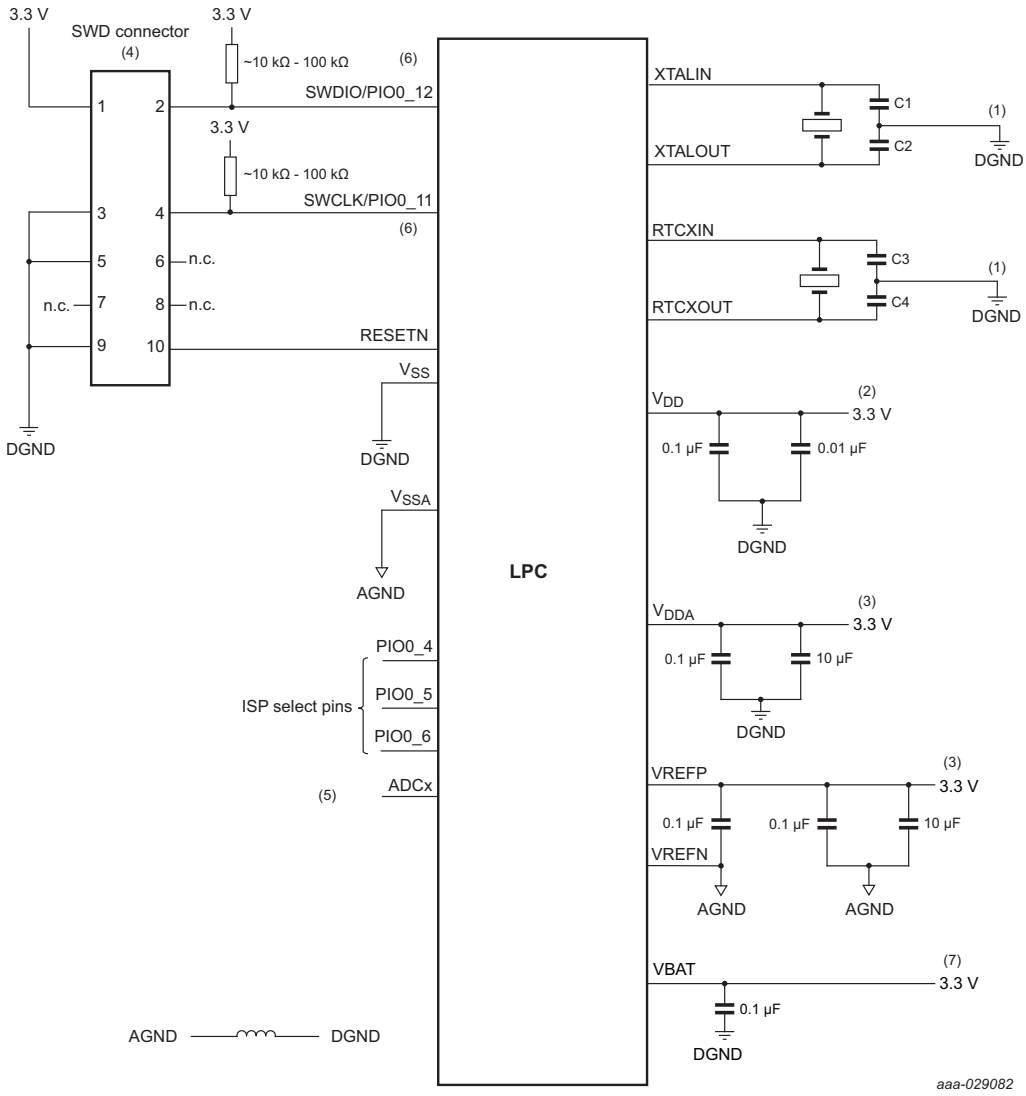

(1) See Section 13.6 “XTAL oscillator” for the values of C1, C2, C3, and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are needed since these pins are in high Z mode (internal pull-up and pull-down disabled). GPIO pins SWDIO/PIO0_12, SWCLK/PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

(7) Position the decoupling capacitor of 0.1 µF as close as possible to the V_{BAT} pin. Tie V_{BAT} to V_{DD} if not used.

Fig 40. Power, clock, and debug connections

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13.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 19 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 19, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 19 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

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13.5 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See Figure 41.

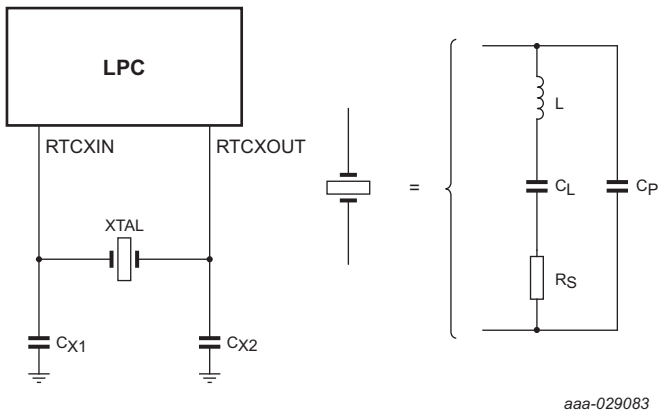

Fig 41. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

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13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

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13.6 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 42.

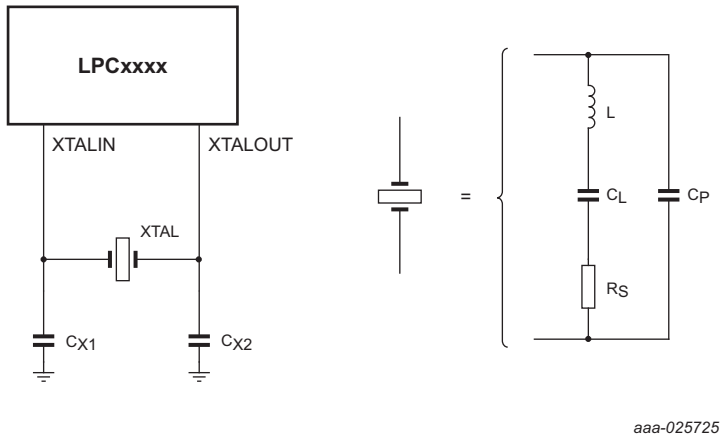

Fig 42. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

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13.6.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 43) or bus-powered device (see Figure 44).

On the LPC54018JxM/LPC54S018JxM, the USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 V_{DD} to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

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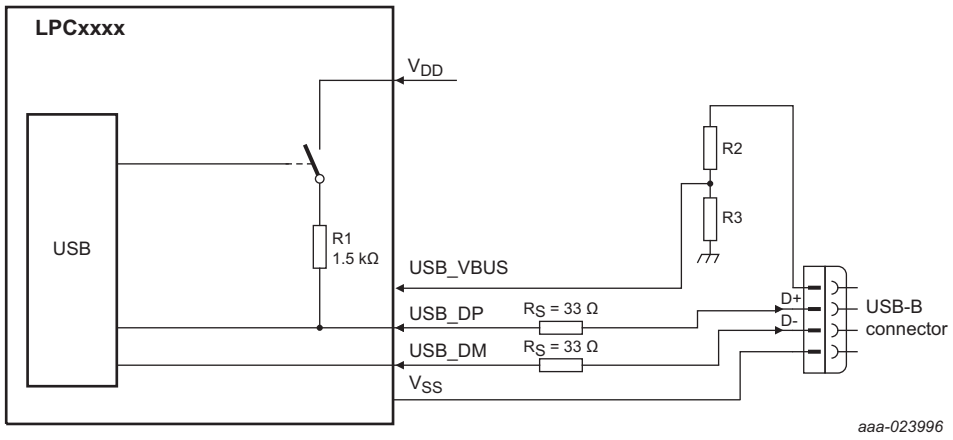
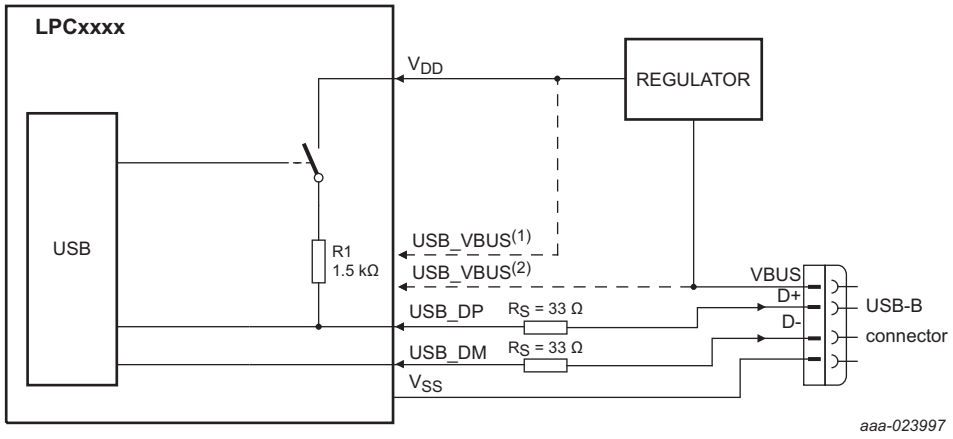


Fig 43. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 44. USB interface on a bus-powered device

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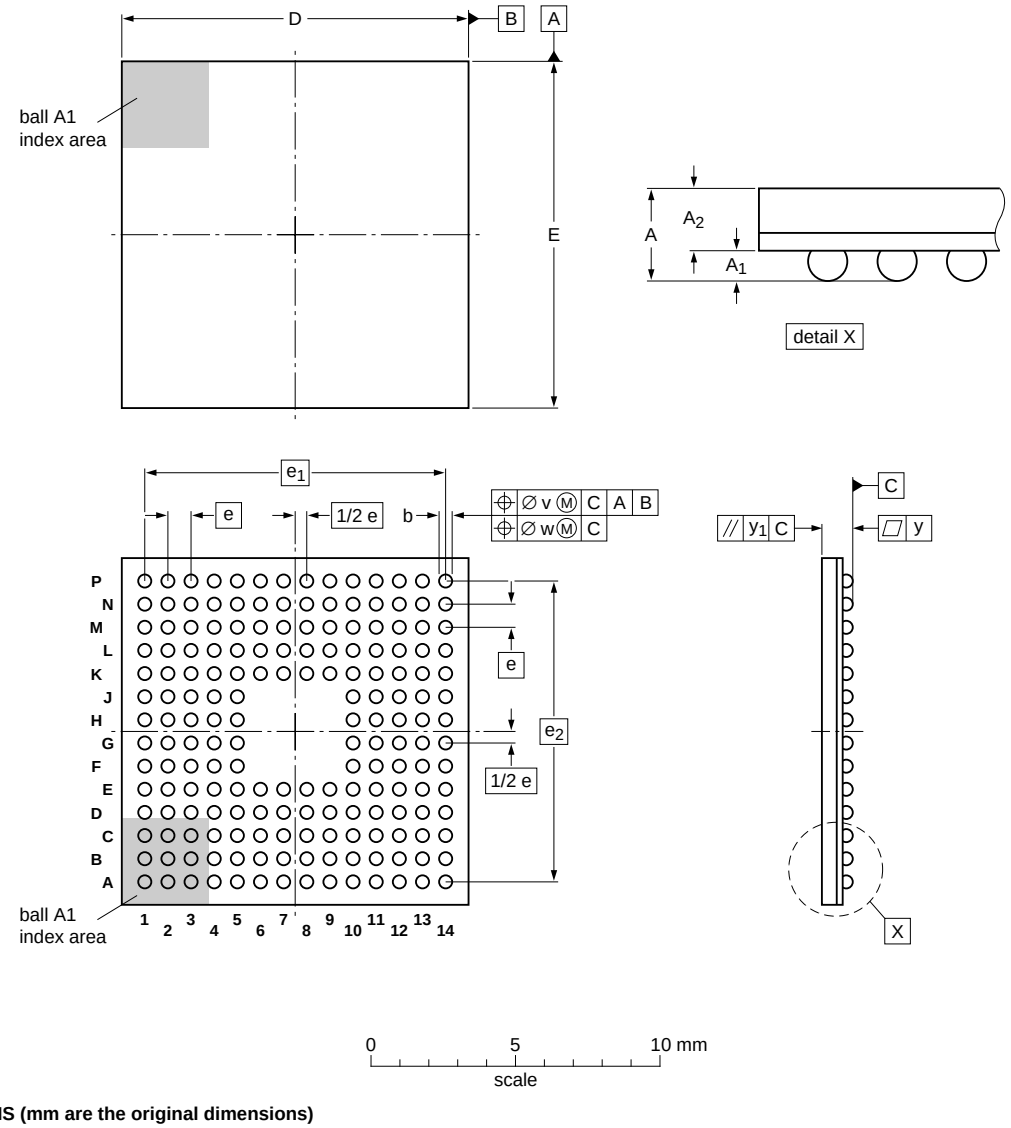
14. Package outline

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 45. TFBGA180 package

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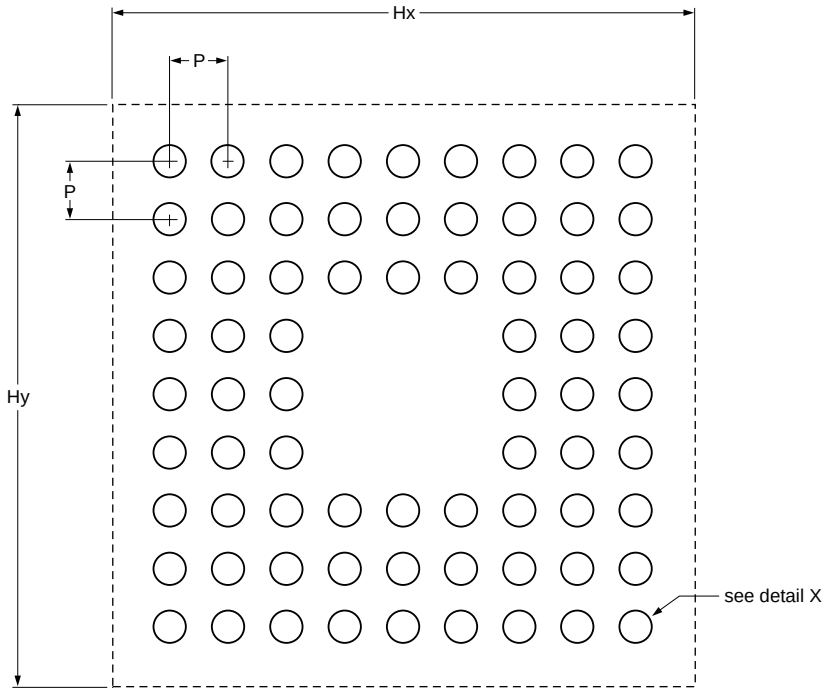
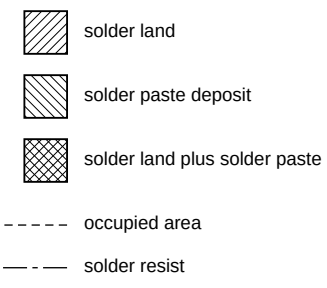
15. Soldering

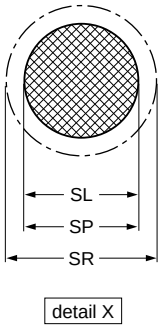
Footprint information for reflow soldering of TFBGA180 package **SOT570-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.400	0.400	0.550	12.575	12.575

sot570-3_fr

Fig 46. Reflow soldering of the TFBGA180 package

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16. Abbreviations

Table 55. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] LPC54018JxM/LPC54S018JxM. User manual UM11155

[2] LPC54018JxM/LPC54S018JxM. Errata sheet.

[3] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

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18. Revision history

Table 56. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC54018JxM/LPC54S018JxM v1.1	20190127	Product data sheet	-	v.1.0
Modifications:	• Updated Table 4 “Pin description”: Added text to USB1_VBUS. • Updated Table 12 “General operating conditions”: Added USB1 analog supply. • Updated Section 7.13.2 “Deep-sleep mode”: Added text: In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled by default. • Updated part number in ordering information			
LPC54018JxM/LPC54S018JxM v1.0	20180918	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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