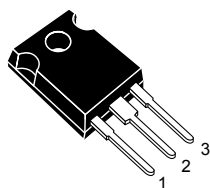
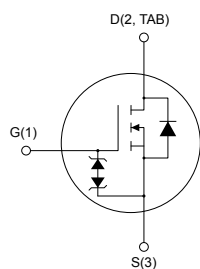


## N-channel 600 V, 0.260 $\Omega$ typ., 12 A MDmesh™ DM2 Power MOSFET in a TO-247 package



TO-247



AM0147SV1



### Features

| Order code  | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|-------------|----------|-------------------|-------|
| STW18N60DM2 | 600 V    | 0.295 $\Omega$    | 12 A  |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

#### Product status links

[STW18N60DM2](#)

#### Product summary

|            |             |
|------------|-------------|
| Order code | STW18N60DM2 |
| Marking    | 18N60DM2    |
| Package    | TO-247      |
| Packing    | Tube        |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                              | Value      | Unit               |
|----------------|------------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                                    | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$  | 12         | A                  |
| $I_D$          | Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$ | 7.6        | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                                 | 48         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$     | 110        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                      | 40         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                              | 50         |                    |
| $T_{stg}$      | Storage temperature range                                              | -55 to 150 | $^{\circ}\text{C}$ |
| $T_j$          | Operating junction temperature range                                   |            | $^{\circ}\text{C}$ |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 12$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 1.14  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 50    |                             |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                                 | Value | Unit |
|----------|---------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive<br>(pulse width limited by $T_{jmax}$ )                                   | 2.5   | A    |
| $E_{AR}$ | Single pulse avalanche energy<br>(starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 380   | mJ   |

## 2 Electrical characteristics

( $T_{case} = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

| Symbol        | Parameter                         | Test conditions                                                                                | Min. | Typ.  | Max.    | Unit          |
|---------------|-----------------------------------|------------------------------------------------------------------------------------------------|------|-------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                    | 600  |       |         | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                                |      |       | 1       | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ ,<br>$T_{case} = 125\text{ °C}$ <sup>(1)</sup> |      |       | 100     | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                             |      |       | $\pm 5$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                             | 3    | 4     | 5       | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 6\text{ A}$                                                    |      | 0.260 | 0.295   | $\Omega$      |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                              | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                         | -    | 800  | -    | pF   |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                              | -    | 40   | -    | pF   |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                              | -    | 1.33 | -    | pF   |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                             | -    | 80   | -    | pF   |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                      | -    | 5.6  | -    | pF   |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 20   | -    | nC   |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                              | -    | 5.2  | -    | nC   |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                              | -    | 8.5  | -    | nC   |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                              | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 13.5 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                              | -    | 8    | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                              | -    | 9.5  | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                              | -    | 32.5 | -    | ns   |

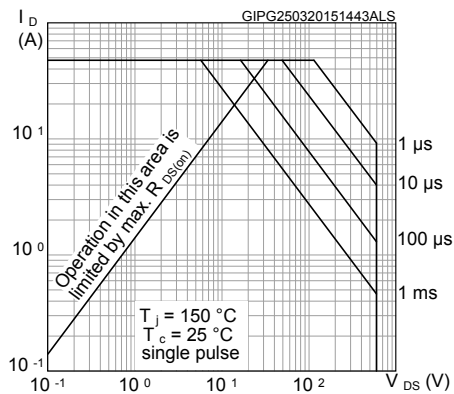
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                 | Min. | Typ.  | Max. | Unit          |
|-----------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                 | -    |       | 12   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                 | -    |       | 48   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 12\text{ A}$                                                                                                                                                                  | -    |       | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                     | -    | 125   |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 0.675 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 11    |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ ,<br>$T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 190   |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 1.225 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 13    |      | A             |

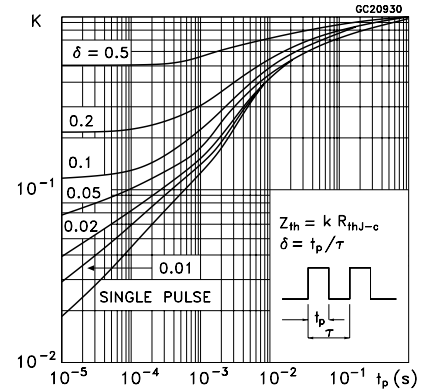
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

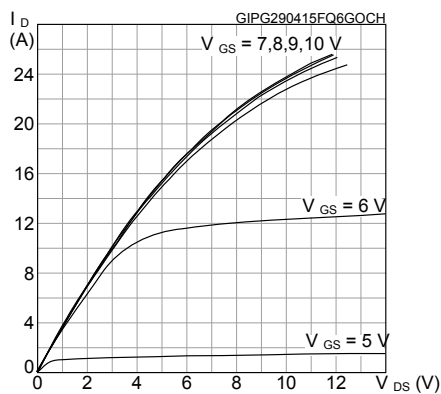
**Figure 1. Safe operating area**



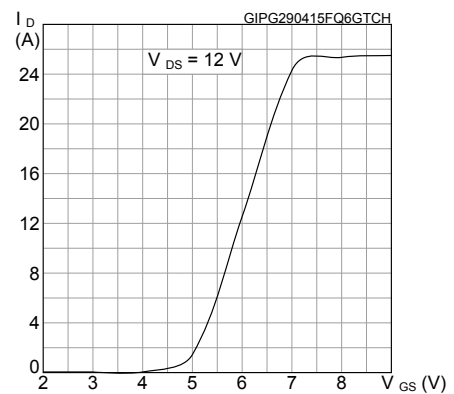
**Figure 2. Thermal impedance**



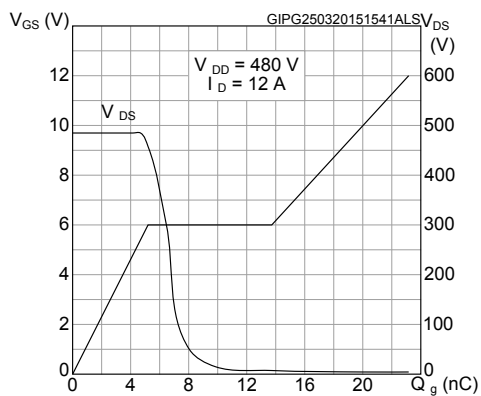
**Figure 3. Output characteristics**



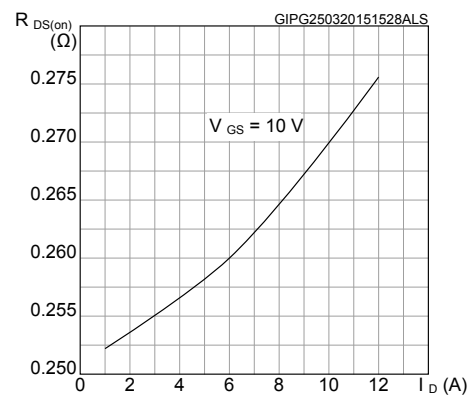
**Figure 4. Transfer characteristics**



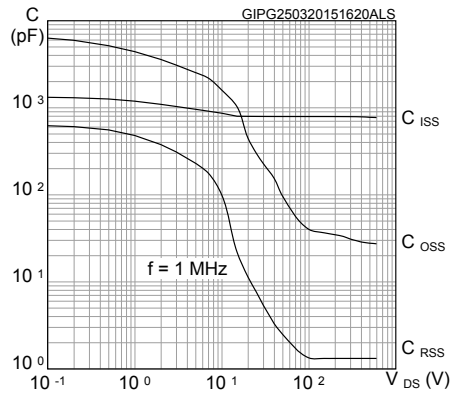
**Figure 5. Gate charge vs gate-source voltage**



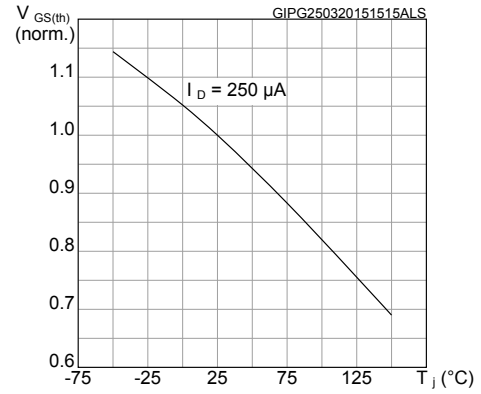
**Figure 6. Static drain-source on-resistance**



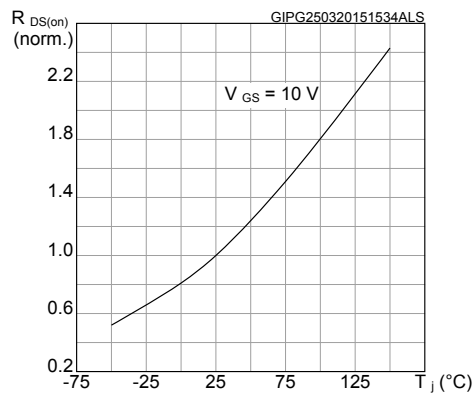
**Figure 7. Capacitance variations**



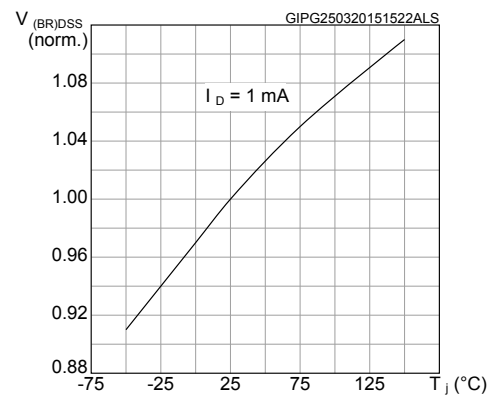
**Figure 8. Normalized gate threshold voltage vs temperature**



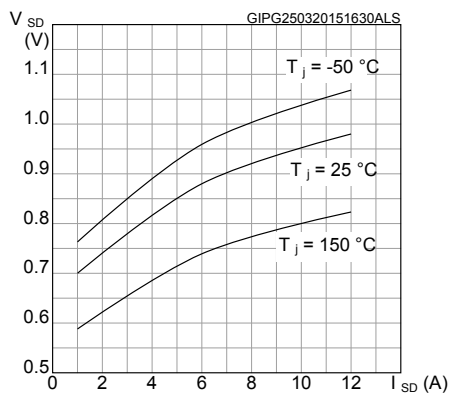
**Figure 9. Normalized on-resistance vs temperature**



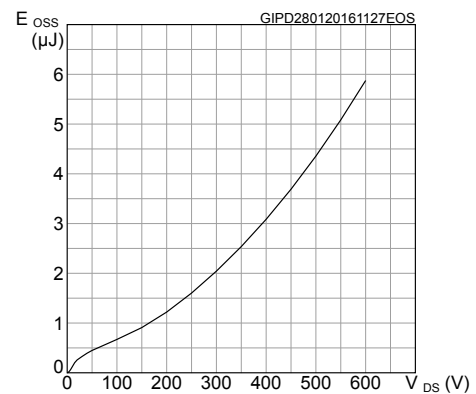
**Figure 10. Normalized V\_(BR)DSS vs temperature**



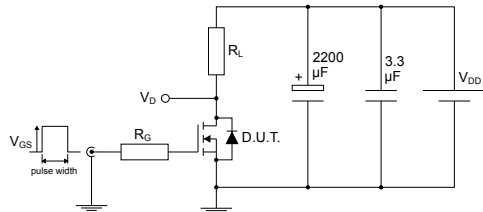
**Figure 11. Source-drain diode forward characteristics**



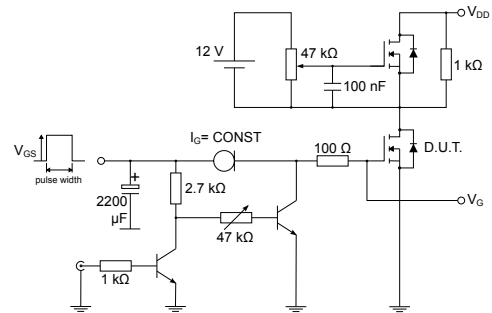
**Figure 12. Output capacitance stored energy**



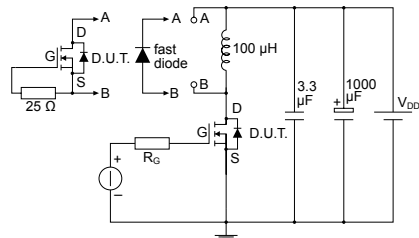
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


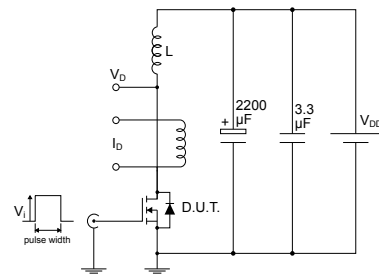
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


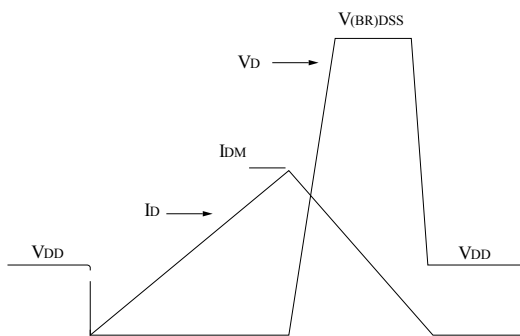
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


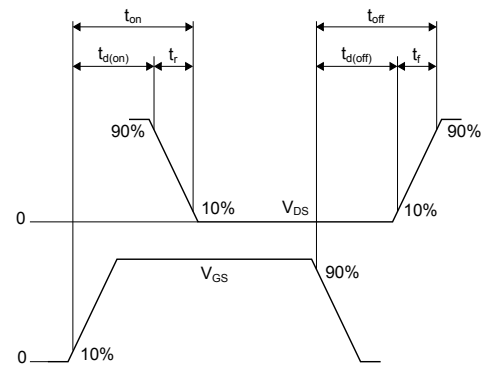
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

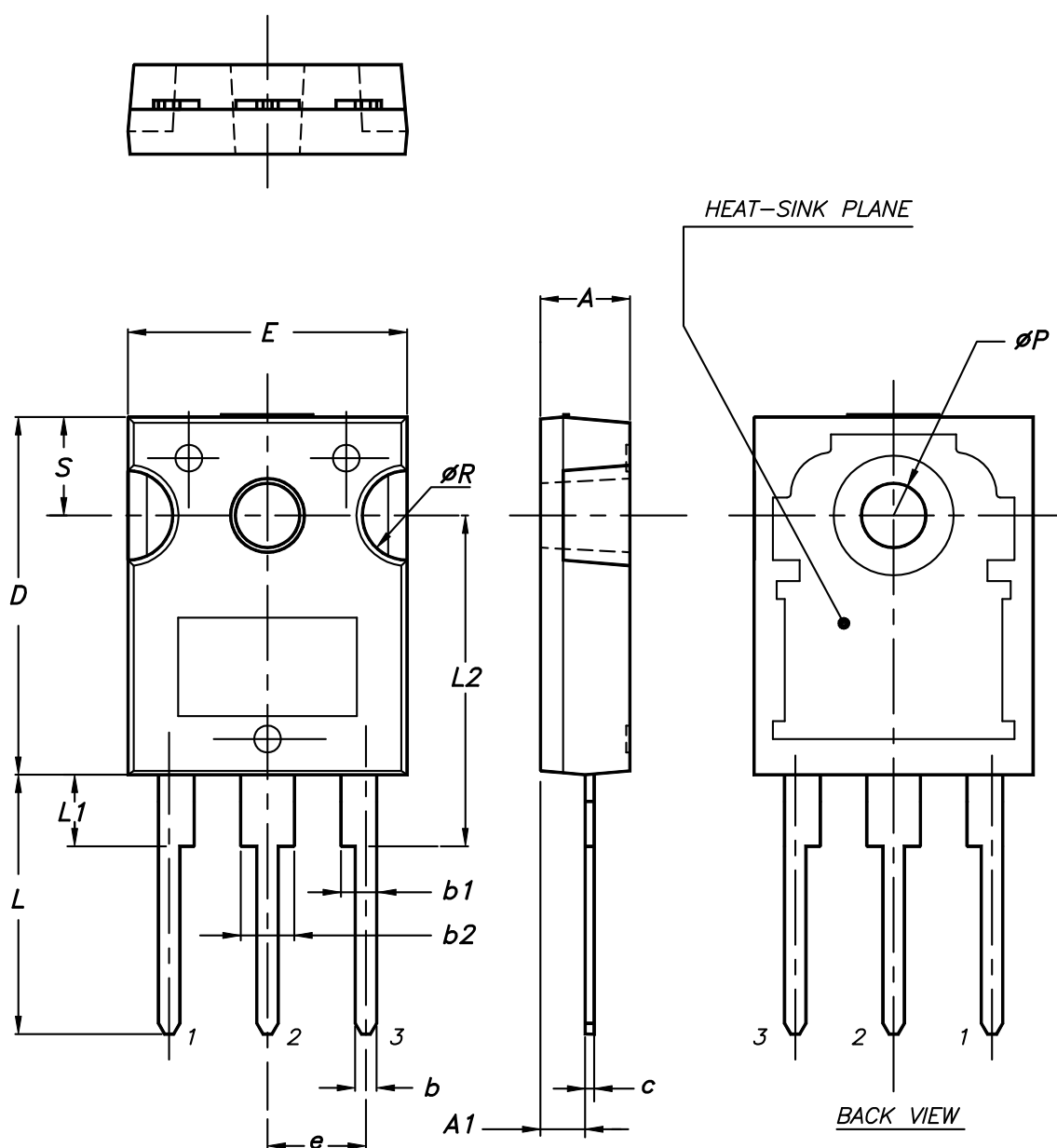
---

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



## 4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325\_9

**Table 8. TO-247 package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                 |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 01-Apr-2015 | 1        | First release.                                                                                                                                                                                                                                                          |
| 29-Apr-2015 | 2        | In <i>Section 2.1 Electrical characteristics (curves)</i> :<br>- updated <i>Figure 4: Output characteristics</i><br>- updated <i>Figure 5: Transfer characteristics</i>                                                                                                 |
| 28-Jan-2016 | 3        | Updated <i>Section 2.1: "Electrical characteristics (curves)"</i>                                                                                                                                                                                                       |
| 06-Dec-2018 | 4        | Removed maturity status indication from cover page. The document status is production data.<br>Modified schematic on cover page.<br>Modified <a href="#">Table 4. Static</a><br>Updated <a href="#">Section 4.1 TO-247 package information</a> .<br>Minor text changes. |
| 28-May-2019 | 5        | Updated <a href="#">Table 1</a> , <a href="#">Table 2</a> and <a href="#">Table 4</a>                                                                                                                                                                                   |

## Contents

|          |                                           |           |
|----------|-------------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings .....</b>           | <b>2</b>  |
| <b>2</b> | <b>Electrical characteristics.....</b>    | <b>3</b>  |
| 2.1      | Electrical characteristics (curves) ..... | 5         |
| <b>3</b> | <b>Test circuits .....</b>                | <b>7</b>  |
| <b>4</b> | <b>Package information.....</b>           | <b>8</b>  |
| 4.1      | TO-247 package information .....          | 8         |
|          | <b>Revision history .....</b>             | <b>11</b> |

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved