

# EiceDRIVER™ Compact

High voltage gate driver IC

## 2EDL family

600 V half bridge gate drive IC

2EDL23I06PJ

2EDL23N06PJ

EiceDRIVER™ Compact

## Final datasheet

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Final

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## **EiceDRIVER™ Compact** **600 V half bridge gate drive IC**

### **1 Overview**

#### **Main features**

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Individual control circuits for both outputs
- Filtered detection of under voltage supply
- All inputs clamped by diodes
- Active shut down function
- Asymmetric undervoltage lockout thresholds for high side and low side
- Qualified according to JEDEC<sup>1</sup> (high temperature stress tests for 1000h) for target applications



#### **Product highlights**

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Ultra fast bootstrap diode
- Overcurrent comparator
- Enable function, Fault indicator

#### **Typical applications**

- Home appliances
- Consumer electronics
- Fans, pumps
- General purpose drives

#### **Product family**

**Table 1 Members of 2EDL family**

| <b>Sales Name</b> | <b>Special function</b>                 | <b>output current</b> | <b>Target transistor</b> | <b>typ. LS UVLO-thresholds</b> | <b>Bootstrap diode</b> | <b>Package</b> |
|-------------------|-----------------------------------------|-----------------------|--------------------------|--------------------------------|------------------------|----------------|
| 2EDL23I06PJ       | deadtime, interlock, Enable, Fault, OCP | 2.3 A                 | IGBT                     | 12.5 V / 11.6 V                | Yes                    | DSO-14         |
| 2EDL23N06PJ       | deadtime, interlock, Enable, Fault, OCP | 2.3 A                 | MOSFET                   | 9.1 V / 8.3 V                  | Yes                    | DSO-14         |

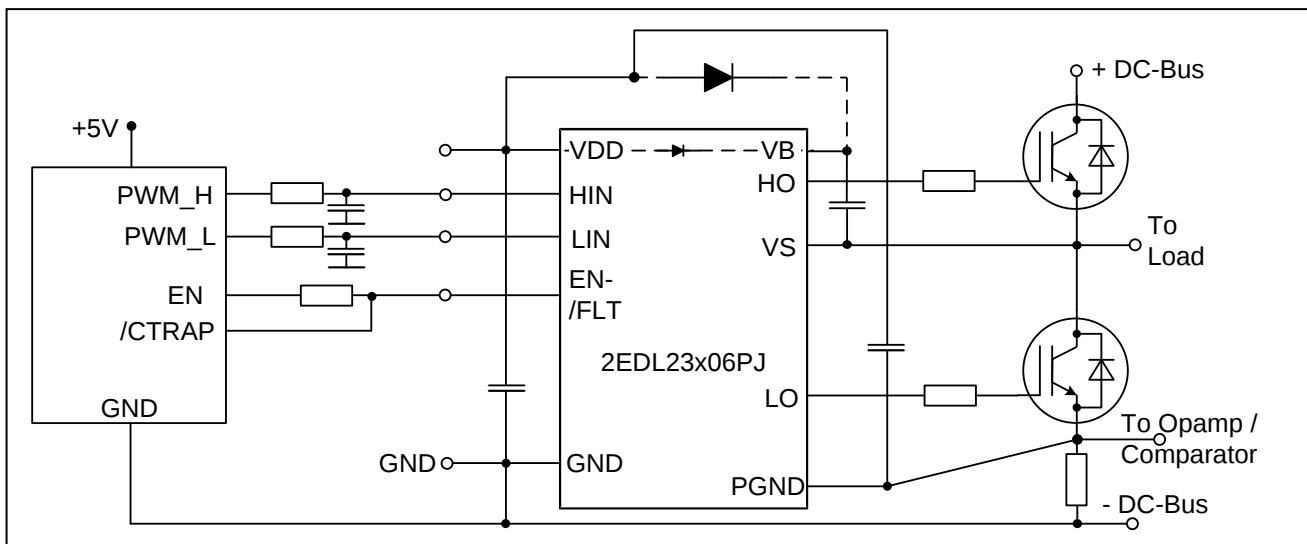
<sup>1</sup> J-STD-020 and JESD-022

## Description

The 2EDL family contains devices, which control power devices like MOS-transistors or IGBTs with a maximum blocking voltage of +600V in half bridge configurations. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

The two independent drivers outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET.

Those parts, which are designed for IGBT have asymmetric undervoltage lockout levels, which support strongly the integrated ultrafast bootstrap diode. Additionally, the offline gate clamping function provides an inherent protection of the transistors for parasitic turn-on by floating gate conditions, when the IC is not supplied via VDD.

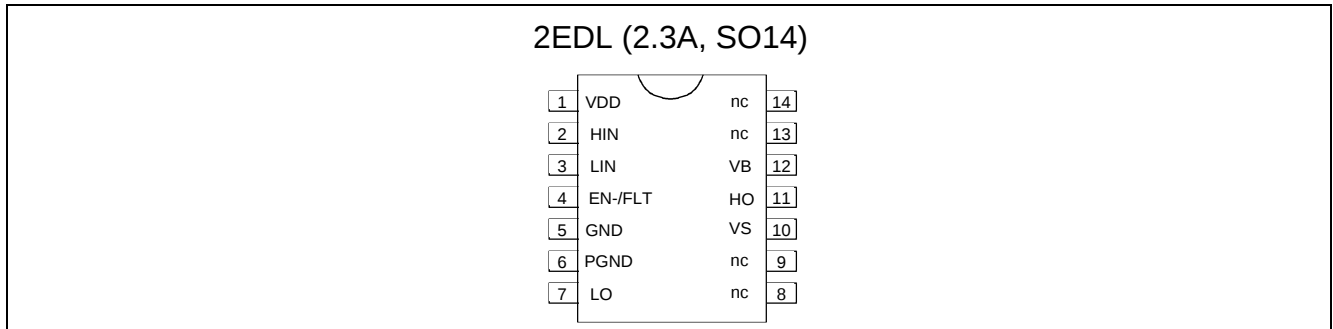


**Figure 1 Typical Application**



### 3 Pin configuration, description, and functionality

#### 3.1 Pin Configuration and Description



**Figure 3** Pin Configuration of 2EDL family

**Table 2** Pin Description

| Symbol  | Description                              |
|---------|------------------------------------------|
| VDD     | Low side power supply                    |
| GND     | Logic ground                             |
| HIN     | High side logic input                    |
| LIN     | Low side logic input                     |
| EN-/FLT | Enable input and Fault indication output |
| PGND    | Low side gate driver reference           |
| VB      | High side positive power supply          |
| HO      | High side gate driver output             |
| VS      | High side negative power supply          |
| LO      | Low side gate driver output              |
| nc      | Not Connected                            |

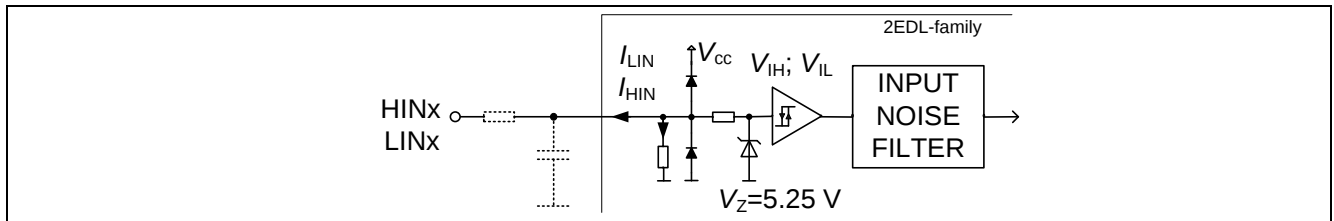
#### 3.2 Low Side and High Side Control Pins (LIN, HIN)

##### 3.2.1 Input voltage range

All input pins have the capability to process input voltages up to the supply voltage of the IC. The inputs are therefore internally clamped to VDD and GND by diodes. An internal pull-down resistor is high ohmic, so that it can keep the IC in a safe state in case of PCB crack.

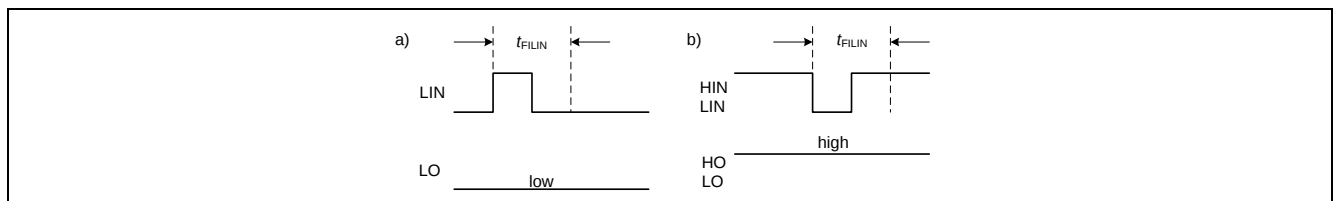
##### 3.2.2 Switching levels

The Schmitt trigger input threshold is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. The input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 5. Please note, that the switching levels of the input structures remain constant even though they can accept amplitudes up to the IC supply level.



**Figure 4**     **Input pin structure**

### 3.2.3 Input filter time



**Figure 5** Input filter timing diagram

Short pulses are suppressed by means of an input filter. The MOSFET version (2EDL23N06PJ) has an input filter time of  $t_{FILIN} = 100$  ns typ. for high side and 150ns typ. for low side. The IGBT version (2EDL23I06PJ) has filter times of 190ns typ.

### 3.3 VDD, GND and PGND (Low Side Supply)

VDD is the low side supply and it provides power to both the input logic and the low side output power stage. The input logic is referenced to GND ground as well as the under-voltage detection circuit. Output power stage is referenced to PGND ground. PGND ground is floating respect to GND ground with an absolute maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The undervoltage lockout circuit enables the device to operate at power on when a typical supply voltage higher than  $V_{DDUV+}$  is present. Please see section 3.6 “Undervoltage lockout” for further information.

A filter time of typ.  $1.5\ \mu\text{s}^1$  helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

### 3.4 VB and VS (High Side Supplies)

VB to VS is the high side supply voltage. The high side circuit can float with respect to GND following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VDD. A filter time of typ. 1.3  $\mu$ s helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than  $V_{DDUV+}$  is present. Please see section 3.6 “Undervoltage lockout” for further information. Details on bootstrap supply section and transient immunity can be found in application note [EiceDRIVER™ 2EDL family: Technical description](#).

### 3.5 LO and HO (Low and High Side Outputs)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive for IGBT and MOSFET devices. Low side output is state triggered by the respective inputs, while high side output is edge triggered by the respective inputs. In particular, after an undervoltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the high side output. In contrast, the low side outputs switch to the state of their respective inputs after an undervoltage condition of the VDD supply.

The output current specification  $I_{O+}$  and  $I_{O-}$  is defined in a way, which considers the power transistors miller voltage. This helps to design the gate drive better in terms of the application needs. Nevertheless, the devices are also characterised for the value of the pulse short circuit value  $I_{OPk+}$  and  $I_{OPk-}$ .

### 3.6 Undervoltage lockout (UVLO)

Two different UVLO options are required for IGBT and MOSFET. The types 2EDL23I06PJ are designed to drive IGBT. There are higher levels of undervoltage lockout for the low side UVLO than for the high side. This supports an improved start up of the IC, when bootstrapping is used. The thresholds for the low side are typically  $V_{DDUV+} = 12.5 \text{ V}$  (positive going) and  $V_{DDUV-} = 11.6 \text{ V}$  (negative going). The thresholds for the high side are typically  $V_{BSUV+} = 11.6 \text{ V}$  (positive going) and  $V_{BSUV-} = 10.7 \text{ V}$  (negative going).

The types 2EDL23N06PJ are designed to drive power MOSFET. A similar distinction for the high side and low side UVLO threshold as for IGBT is not realised here. The IC shuts down all the gate drivers power outputs, when the supply voltage is below typ.  $V_{DDUV-} = 8.3 \text{ V}$  (min. / max. =  $7.5 \text{ V} / 9 \text{ V}$ ). The turn-on threshold is typ.  $V_{DDUV+} = 9.1 \text{ V}$  (min. / max. =  $8.3 \text{ V} / 9.9 \text{ V}$ ).

### 3.7 Bootstrap diode

An ultra fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when charging the bootstrap capacitor initially.

### 3.8 Deadtime and interlock function

The IC provides a hardware fixed deadtime. The deadtime is different for the MOSFET type (2EDL23N06PJ) and for the IGBT type (2EDL23I06PJ). The deadtimes are particularly typ. 380 ns for IGBT and typ. 75 ns for MOSFET. An additional interlock function prevents the two outputs from being activated simultaneously.

### 3.9 EN-/FLT (fault indication and enable function)

The types 2EDL23x06PJ provide a pin, which can either be used to shut down the IC or to read out a failure status of the IC. The signal applied to pin EN controls directly the output stages. All outputs are set to LOW, if EN is at LOW logic level. An integrated pull down resistor shuts down the IC in case of a floating input. The internal structure of the pin is given in Figure 6. The switching levels of the Schmitt-Trigger are here  $V_{EN,TH+} = 2.1 \text{ V}$  and  $V_{EN,TH-} = 0.9 \text{ V}$ . The typical propagation delay time is  $t_{EN} = 550 \text{ ns}$ . The input is clamped by diodes to VDD and GND. The input voltage range is the same as the input control pins with a max. of 20 V.

The /FAULT function is an active low open-drain output indicating the status of the gate driver (see Figure 6). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VDD supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VDD pin description for more details). The fault signal is activate as long as UVLO is given during power up.
- Overcurrent detection (ITRIP): The fault condition is latched until the overcurrent trigger condition is finished and additional typ. 230  $\mu\text{s}$  are elapsed.

The interface to the microcontroller can be realised by using an open collector / drain configured output pin for enabling the driver IC and a GPIO pin for monitoring the /FAULT. The external pull-up resistor will pull-up the voltage to +5V, when the IC is set for operation.

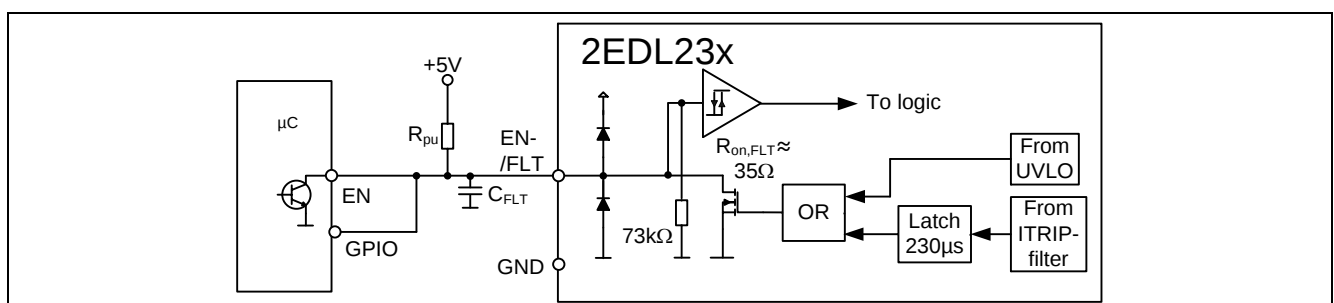


Figure 6 EN-/FLT pin structures and interface to microcontroller (µC)

### **3.10 Power ground / over current protection**

A power ground (PGND) connects directly the emitter or source of the low side transistor with the gate drive IC. No other components, such as shunts, etc., are between this connection and the emitter or source. This enables the routing of smallest gate circuit loops and therefore smallest gate inductances.

A potential shunt resistor is between the power ground (PGND) connection and the ground connection (GND), which leads to a voltage drop between these two pins.

The voltage drop between PGND and GND can be sensed by means of a comparator with a threshold of  $V_{th,ITRIP} = 0.46 \text{ V}$ . If the voltage drop is larger than  $V_{th,ITRIP}$ , then the output of the comparator is triggered and the /FLT output is activated. Simultaneously, the IC shuts down both gate outputs for the period of the fault indication, which is 230  $\mu\text{s}$ .

Several influences, such as reverse recovery currents, parasitic inductances and other noise sources, make the need of a signal filter necessary. The filter has a time constant of typically 1.8  $\mu\text{s}$  to ensure good noise quality.

---

<sup>1</sup> Not subject of production test, verified by characterisation

## 4 Electrical Parameters

### 4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to  $V_{GND}$  -potential unless otherwise specified. ( $T_a=25^{\circ}\text{C}$ )

**Table 3 Abs. maximum ratings**

| Parameter                                                                  | Symbol        | Min.               | Max.               | Unit               |
|----------------------------------------------------------------------------|---------------|--------------------|--------------------|--------------------|
| High side offset voltage(Note 1)                                           | $V_S$         | $V_{DD}-V_{BS}-6$  | 600                | V                  |
| High side offset voltage ( $t_p<500\text{ns}$ , Note 1)                    |               | $V_{DD}-V_{BS}-50$ | –                  |                    |
| High side offset voltage(Note 1)                                           | $V_B$         | $V_{DD}-6$         | 620                |                    |
| High side offset voltage ( $t_p<500\text{ns}$ , Note 1)                    |               | $V_{DD}-50$        | –                  |                    |
| High side floating supply voltage ( $V_B$ vs. $V_S$ ) (internally clamped) | $V_{BS}$      | -1                 | 20                 |                    |
| High side output voltage ( $V_{HO}$ vs. $V_S$ )                            | $V_{HO}$      | -0.5               | $V_B + 0.5$        |                    |
| Low side supply voltage (internally clamped)                               | $V_{DD}$      | -1                 | 20                 |                    |
| Low side supply voltage ( $V_{DD}$ vs. $V_{PGND}$ )                        | $V_{DDPGND}$  | -0.5               | 25                 |                    |
| Gate driver ground                                                         | $V_{PGND}$    | -5.7               | 5.7                |                    |
| Low side output voltage ( $V_{LO}$ vs. $V_{PGND}$ )                        | $V_{LO}$      | -0.5               | $V_{DDPGND} + 0.5$ |                    |
| Input voltage LIN,HIN,EN                                                   | $V_{IN}$      | -0.5               | $V_{DD} + 0.5$     |                    |
| FAULT output voltage                                                       | $V_{FLT}$     | -0.5               | $V_{DD} + 0.5$     |                    |
| Power dissipation (to package) (Note 2)                                    | $P_D$         | –                  | 0.9                | W                  |
| Thermal resistance<br>(junction to ambient, see section 6)                 | $R_{th(j-a)}$ | –                  | 134                | K/W                |
| Junction temperature (Note 3)                                              | $T_J$         | –                  | 150                | $^{\circ}\text{C}$ |
| Storage temperature                                                        | $T_S$         | - 40               | 150                |                    |
| offset voltage slew rate (Note 4)                                          | $dV_S/dt$     | –                  | 50                 | V/ns               |

Note :The minimum value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side ( $V_{DD}$ , HIN, LIN, FAULT, EN, GND, PGND, LO) and pins connected inside each high side itself ( $V_B$ , HO, VS) is guaranteed up to 1.5kV (Human Body Model) respectively.

Note 1 : In case  $V_{DD} > V_B$  there is an additional power dissipation in the internal bootstrap diode between pins  $V_{DD}$  and  $V_B$  in case of activated bootstrap diode. Insensitivity of bridge output to negative transient voltage up to  $-50\text{V}$  is not subject to production test – verified by design / characterization.

Note 2: Consistent power dissipation of all outputs. All parameters are inside operating range.

Note 3: Qualification stress tests cover a max. junction temperature of  $150^{\circ}\text{C}$  for 1000 h.

Note 4: Not subject of production test, verified by characterisation.

## 4.2 Required operation conditions

All voltages are absolute voltages referenced to  $V_{GND}$  -potential unless otherwise specified. ( $T_a = 25^\circ\text{C}$ )

**Table 4 Required Operation Conditions**

| Parameter                                           | Symbol       | Min. | Max. | Unit |
|-----------------------------------------------------|--------------|------|------|------|
| High side offset voltage (Note 1)                   | $V_B$        | 7    | 620  | V    |
| Low side supply voltage ( $V_{DD}$ vs. $V_{PGND}$ ) | $V_{DDPGND}$ | 10   | 25   |      |

## 4.3 Operating Range

All voltages are absolute voltages referenced to  $V_{GND}$  -potential unless otherwise specified. ( $T_a = 25^\circ\text{C}$ )

**Table 5 Operating range**

| Parameter                                                                   |              | Symbol             | Min.                  | Max.     | Unit             |
|-----------------------------------------------------------------------------|--------------|--------------------|-----------------------|----------|------------------|
| High side floating supply offset voltage                                    |              | $V_S$              | $V_{DD} - V_{BS} - 1$ | 500      | V                |
| High side floating supply offset voltage ( $V_B$ vs. $V_{DD}$ , statically) |              | $V_{BDD}$          | -1.0                  | 500      |                  |
| High side floating supply voltage ( $V_B$ vs. $V_S$ , Note 1)               | IGBT-Types   | $V_{BS}$           | 13                    | 17.5     |                  |
|                                                                             | MOSFET-Types |                    | 10                    | 17.5     |                  |
| High side output voltage ( $V_{HO}$ vs. $V_S$ )                             |              | $V_{HO}$           | 10                    | $V_{BS}$ |                  |
| Low side output voltage ( $V_{LO}$ vs. $V_{PGND}$ )                         |              | $V_{LO}$           | 0                     | $V_{DD}$ |                  |
| Low side supply voltage                                                     | IGBT-Types   | $V_{DD}$           | 13                    | 17.5     |                  |
|                                                                             | MOSFET-Types |                    | 10                    | 17.5     |                  |
| Low side ground voltage                                                     |              | $V_{PGND}$         | -2.5                  | 2.5      |                  |
| Logic input voltages LIN, HIN, EN (Note 2)                                  |              | $V_{IN}$           | 0                     | 17.5     |                  |
| FAULT output voltage                                                        |              | $V_{FLT}$          | 0                     | $V_{DD}$ | $\mu\text{s}$    |
| Pulse width for ON or OFF (Note 3)                                          | IGBT-Types   | $t_{IN}$           | 0.8                   | —        |                  |
|                                                                             | MOSFET-Types |                    | 0.3                   | —        |                  |
| Ambient temperature                                                         |              | $T_a$              | -40                   | 95       | $^\circ\text{C}$ |
| Thermal resistance<br>(junction to ambient, see section 6)                  | DSO8         | $\Psi_{th(j-top)}$ | —                     | 4.8      | K/W              |
|                                                                             | DSO14        |                    | —                     | 3.3      |                  |

Note 1 : Logic operational for  $V_B$  ( $V_B$  vs.  $V_{GND}$ )  $> 7.0\text{V}$

Note 2 : All input pins (HIN, LIN) and EN pin are internally clamped (see abs. maximum ratings)

Note 3 : The input pulse may not be transmitted properly in case of input pulse width at LIN and HIN below  $0.8\mu\text{s}$  (IGBT types) or  $0.3\mu\text{s}$  (MOSFET) respectively

#### 4.4 Static logic function table

| VDD          | VBS          | ENABLE | FAULT     | PGND             | LO  | HO  |
|--------------|--------------|--------|-----------|------------------|-----|-----|
| $<V_{DDUV-}$ | X            | X      | 0         | X                | 0   | 0   |
| 15V          | $<V_{BSUV-}$ | 3.3 V  | High imp. | $< V_{th,ITRIP}$ | LIN | 0   |
| 15V          | 15V          | 3.3 V  | 0         | $> V_{th,ITRIP}$ | 0   | 0   |
| 15V          | 15V          | 0 V    | High imp. | X                | 0   | 0   |
| 15V          | 15V          | 3.3 V  | High imp. | $< V_{th,ITRIP}$ | LIN | HIN |

All voltages with reference to GND

#### 4.5 Static parameters

$V_{DD} = V_{BS} = 15V$  unless otherwise specified. ( $T_a = 25^\circ C$ ) and  $V_{GND} = V_{PGND}$  unless otherwise specified

**Table 6** Static parameters

| Parameter                                             |              | Symbol              | Values |                 |                | Unit    | Test condition                                |
|-------------------------------------------------------|--------------|---------------------|--------|-----------------|----------------|---------|-----------------------------------------------|
|                                                       |              |                     | Min.   | Typ.            | Max.           |         |                                               |
| High level input voltage                              |              | $V_{IH}$            | 1.7    | 2.1             | 2.4            | V       |                                               |
| Low level input voltage                               |              | $V_{IL}$            | 0.7    | 0.9             | 1.1            |         |                                               |
| EN positive going threshold                           |              | $V_{EN,TH+}$        | 1.7    | 2.1             | 2.4            |         |                                               |
| EN negative going threshold                           |              | $V_{EN,TH-}$        | 0.7    | 0.9             | 1.1            |         |                                               |
| High level output voltage                             | LO           | $V_{OH}$            | –      | $V_{DD}-0.32$   | $V_{DD}-0.7$   |         | $I_O = -100\text{ mA}$                        |
|                                                       | HO           |                     | –      | $V_B-0.32$      | $V_B-0.7$      |         |                                               |
| High level output voltage                             | LO           | $V_{OL}$            | –      | $V_{PGND}+0.18$ | $V_{PGND}-0.4$ |         | $I_O = 100\text{ mA}$                         |
|                                                       | HO           |                     | –      | $V_S+0.18$      | $V_S+0.4$      |         |                                               |
| $V_{DD}$ supply undervoltage positive going threshold | IGBT-types   | $V_{DDUV+}$         | 11.8   | 12.5            | 13.2           |         |                                               |
|                                                       | MOSFET types |                     | 8.3    | 9.1             | 9.9            |         |                                               |
| $V_{BS}$ supply undervoltage positive going threshold | IGBT-types   | $V_{BSUV+}$         | 10.9   | 11.6            | 12.4           |         |                                               |
|                                                       | MOSFET types |                     | 8.3    | 9.1             | 9.9            |         |                                               |
| $V_{DD}$ supply undervoltage negative going threshold | IGBT-types   | $V_{DDUV-}$         | 10.9   | 11.6            | 12.4           |         |                                               |
|                                                       | MOSFET types |                     | 7.5    | 8.3             | 9              |         |                                               |
| $V_{BS}$ supply undervoltage negative going threshold | IGBT-types   | $V_{BSUV-}$         | 10     | 10.7            | 11.7           |         |                                               |
|                                                       | MOSFET types |                     | 7.5    | 8.3             | 9              |         |                                               |
| $V_{DD}$ and $V_{BS}$ supply UVLO hysteresis          | IGBT-types   | $V_{DDUVH}$         | 0.5    | 0.9             | –              |         |                                               |
|                                                       | MOSFET types | $V_{BSUVH}$         | 0.5    | 0.9             | –              |         |                                               |
| ITRIP comparator threshold                            |              | $V_{th,ITRIP}$      | 0.4    | 0.46            | 0.53           |         | $V_{ITRIP} = V_{PGND} - V_{GND}$              |
| ITRIP comparator hysteresis                           |              | $V_{th,ITRIP\ hys}$ | 0.045  | 0.07            | –              |         |                                               |
| High side leakage current betw. VS and GND            |              | $I_{LVS+}$          | –      | 1               | 12.5           | $\mu A$ | $V_S = 600V$                                  |
| High side leakage current betw. VS and GND            |              | $I_{LVS+}^1$        | –      | 10              | –              |         | $T_J = 125^\circ C$ ,<br>$V_S = 600\text{ V}$ |

<sup>1</sup> Not subject of production test, verified by characterisation

**Table 6 Static parameters**

| Parameter                                                                                      | Symbol       | Values |      |      | Unit          | Test condition                                  |
|------------------------------------------------------------------------------------------------|--------------|--------|------|------|---------------|-------------------------------------------------|
|                                                                                                |              | Min.   | Typ. | Max. |               |                                                 |
| Quiescent current $V_{BS}$ supply (VB only)                                                    | $I_{QBS1}$   | –      | 180  | 300  |               | HO = low<br>depending on<br>current types       |
| Quiescent current $V_{BS}$ supply (VB only)                                                    | $I_{QBS2}$   | –      | 180  | 300  |               | HO = high<br>depending on<br>current types      |
| Quiescent current VDD supply (VDD only)                                                        | $I_{QDD1}$   | –      | 0.34 | 0.8  | mA            | $V_{LIN} = \text{float}$                        |
| Quiescent current VDD supply (VDD only)                                                        | $I_{QDD2}$   | –      | 0.32 | 0.8  |               | $V_{LIN} = 3.3 \text{ V}$ , $V_{HIN}=0$         |
| Quiescent current VDD supply (VDD only)                                                        | $I_{QDD3}$   | –      | 0.32 | 0.8  |               | $V_{LIN}=0$ , $V_{HIN}=3.3 \text{ V}$           |
| Input bias current                                                                             | $I_{LIN+}$   | 15     | 35   | 60   | $\mu\text{A}$ | $V_{LIN} = 3.3 \text{ V}$                       |
| Input bias current                                                                             | $I_{LIN-}$   | –      | 0    | –    |               | $V_{LIN} = 0$                                   |
| Input bias current                                                                             | $I_{HIN+}$   | 15     | 35   | 60   |               | $V_{HIN} = 3.3 \text{ V}$                       |
| Input bias current                                                                             | $I_{HIN-}$   | –      | 0    | –    |               | $V_{HIN} = 0$                                   |
| Input bias current (EN=high)                                                                   | $I_{EN+}$    | –      | 45   | 100  |               | $V_{ENABLE} = 3.3 \text{ V}$                    |
| Mean output current for load capacity<br>charging in range from 4.5 (30%) to 7.5V<br>(50%)     | $I_{O+}$     | 1.3    | 1.8  | –    | A             | $C_L = 61 \text{ nF}$                           |
| Peak output current turn on (single pulse)                                                     | $I_{Opk+}^1$ | –      | 2.3  | –    | A             | $R_L = 0 \Omega$ , $t_p < 10 \mu\text{s}$       |
| Mean output current for load capacity<br>discharging in range from 7.5V (50%) to<br>4.5V (30%) | $I_{O-}$     | 1.65   | 2.5  | –    | A             | $C_L = 61 \text{ nF}$                           |
| Peak output current turn off (single pulse)                                                    | $I_{Opk-}^1$ | –      | 2.8  | –    | A             | $R_L = 0 \Omega$ , $t_p < 10 \mu\text{s}$       |
| Bootstrap diode forward voltage between<br>VDD and VB                                          | $V_{F,BSD}$  | –      | 0.9  | 1.2  | V             | $I_F = 0.3 \text{ mA}$                          |
| Bootstrap diode forward current between<br>VDD and VB                                          | $I_{F,BSD}$  | 45     | 82   | 120  | mA            | $V_{DD} - V_B = 4 \text{ V}$                    |
| Bootstrap diode resistance                                                                     | $R_{BSD}$    | 15     | 27   | 40   |               | $V_{F1} = 4 \text{ V}$ , $V_{F2} = 5 \text{ V}$ |
| EN-/FLT low on resistance of the pull down<br>transistor                                       | $R_{on,FLT}$ | –      | 35   | 70   |               | $V_{EN-/FLT} = 0.5 \text{ V}$                   |

<sup>1</sup> Not subject of production test, verified by characterisation

## 4.6 Dynamic parameters

$V_{DD} = V_{BS} = 15\text{ V}$ ,  $V_S = V_{GND} = V_{PGND}$ ,  $C_L = 180\text{ pF}$  unless otherwise specified. ( $T_A = 25^\circ\text{C}$ )

**Table 7 Dynamic parameters**

| Parameter                                                 |              | Symbol         | Values |      |      | Unit          | Test condition                                                                                                                                                                  |
|-----------------------------------------------------------|--------------|----------------|--------|------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                           |              |                | Min.   | Typ. | Max. |               |                                                                                                                                                                                 |
| Turn-on propagation delay                                 | IGBT types   | $t_{on}$       | 280    | 420  | 610  | ns            | $V_{LIN/HIN} = 0\text{ or }3.3\text{ V}$                                                                                                                                        |
|                                                           | MOSFET types |                | 210    | 310  | 460  |               |                                                                                                                                                                                 |
| Turn-off propagation delay                                | IGBT types   | $t_{off}$      | 260    | 400  | 590  |               |                                                                                                                                                                                 |
|                                                           | MOSFET types |                | 200    | 300  | 440  |               |                                                                                                                                                                                 |
| Turn-on rise time                                         |              | $t_r$          | —      | 48   | 80   | ns            | $V_{LIN/HIN} = 0\text{ or }3.3\text{ V}$<br>$C_L = 4.9\text{ nF}$                                                                                                               |
| Turn-off fall time                                        |              | $t_f$          | —      | 37   | 60   |               |                                                                                                                                                                                 |
| Shutdown propagation delay ENABLE                         |              | $t_{EN}$       | —      | 550  | 850  |               |                                                                                                                                                                                 |
| Input filter time at LIN/HIN for turn on and off          | IGBT types   | $t_{FILIN}$    | 120    | 190  | 320  |               | $V_{LIN/HIN} = 0\text{ \& }3.3\text{ V}$                                                                                                                                        |
|                                                           | MOSFET types |                | 50     | 100  | 170  |               |                                                                                                                                                                                 |
|                                                           | HIN<br>LIN   |                | 100    | 150  | 250  |               |                                                                                                                                                                                 |
| Input filter time EN                                      |              | $t_{FILEN}$    | 200    | 400  | —    | $\mu\text{s}$ | $V_{PGND} = 1\text{ V}$ , /FLT=0<br>$V_{PGND} = 1\text{ V}$<br>$V_{LO} / V_{HO} = 3\text{ V}$<br>$V_{PGND} = 1\text{ V}$ , /FLT=0.5 V<br>$V_{PGND} = 0.1\text{ V}$ , /FLT=2.1 V |
| ITRIP filter time                                         |              | $t_{FILITRIP}$ | 1.0    | 1.8  | 2.7  |               |                                                                                                                                                                                 |
| Shut down propagation delay PGND to any output            |              | $t_{ITRIP}$    | 1.1    | 2.2  | 3.0  |               |                                                                                                                                                                                 |
| Propagation delay ITRIP to FAULT                          |              | $t_{FLT}$      | 1.0    | 2.1  | 2.9  |               |                                                                                                                                                                                 |
| Fault-clear time                                          |              | $t_{FLTCLR}$   | 70     | 230  | —    | ns            | $V_{LIN/HIN} = 0\text{ \& }3.3\text{ V}$<br>ext. dead time 0ns<br>external dead time > 500 ns<br>external dead time >500 ns<br>$PW_{in} > 1\text{ }\mu\text{s}$                 |
| Dead time                                                 | IGBT types   | DT             | 260    | 380  | 540  |               |                                                                                                                                                                                 |
|                                                           | MOSFET types |                | 30     | 75   | 140  |               |                                                                                                                                                                                 |
| Dead time matching<br>abs(DT_LH – DT_HL)<br>for single IC | IGBT types   | MDT            | —      | 10   | 80   |               |                                                                                                                                                                                 |
|                                                           | MOSFET types |                | —      | 10   | 50   |               |                                                                                                                                                                                 |
| Matching delay ON, abs(ton_HS - ton_LS)                   |              | $MT_{ON}$      | —      | 10   | 60   |               |                                                                                                                                                                                 |
| Matching delay OFF, abs(toff_HS - toff_LS)                |              | $MT_{OFF}$     | —      | 10   | 60   |               |                                                                                                                                                                                 |
| Output pulse width<br>matching. $PW_{in} - PW_{out}$      | IGBT types   | PM             | —      | 20   | 80   |               |                                                                                                                                                                                 |
|                                                           | MOSFET types |                | —      | 20   | 70   |               |                                                                                                                                                                                 |

## 5 Timing diagrams

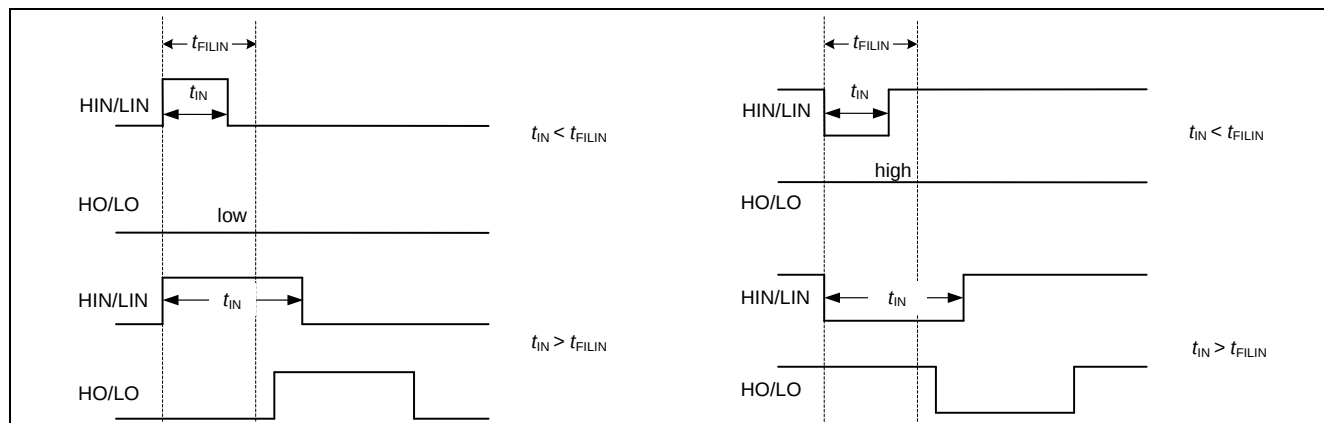


Figure 7 Timing of short pulse suppression

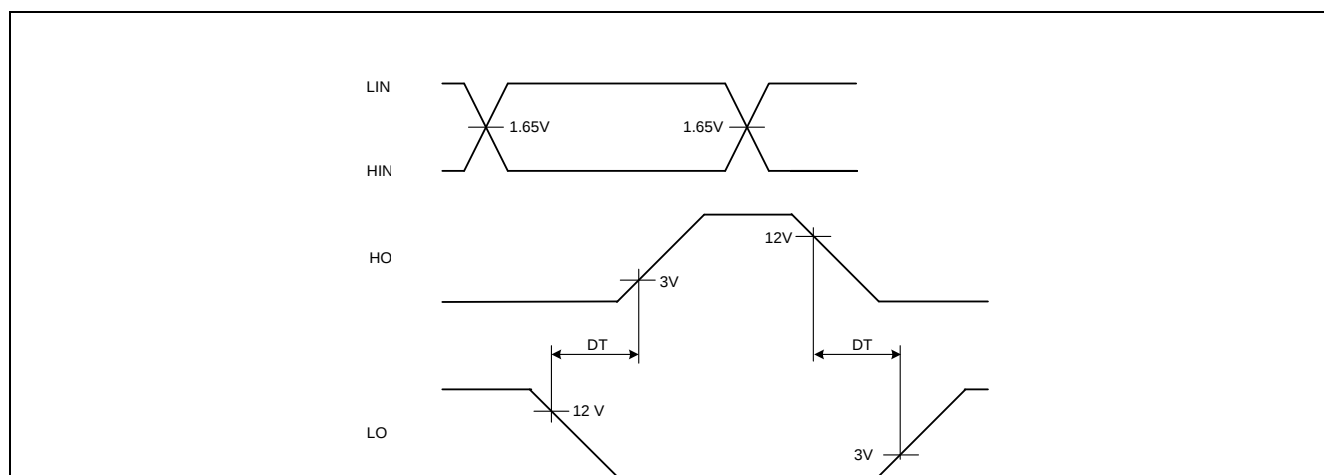


Figure 8 Timing of internal deadtime

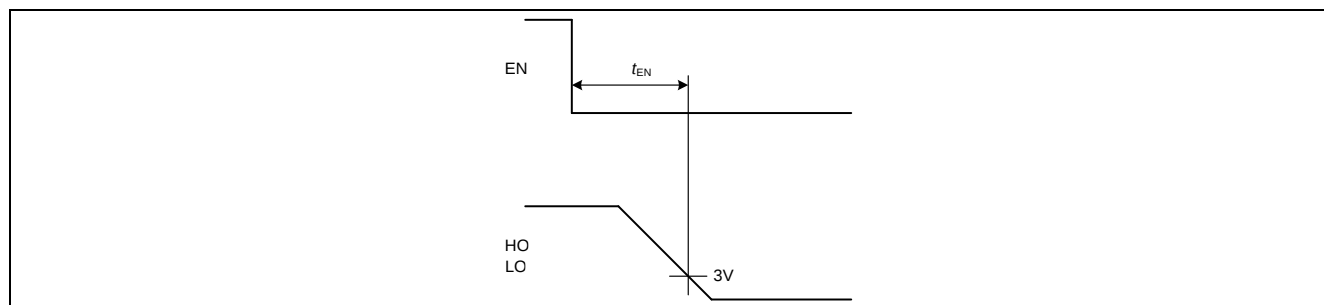


Figure 9 Enable delay time definition

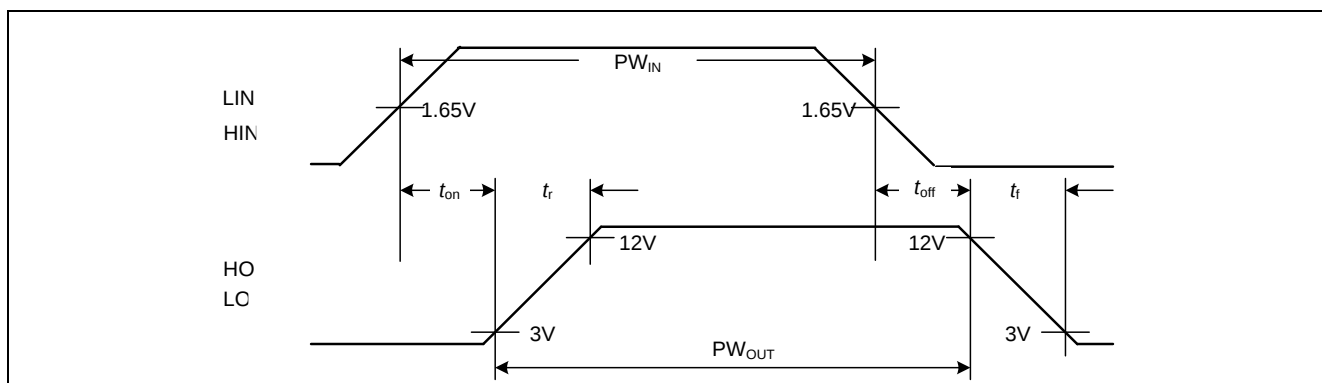


Figure 10 Input to output propagation delay times and switching times definition

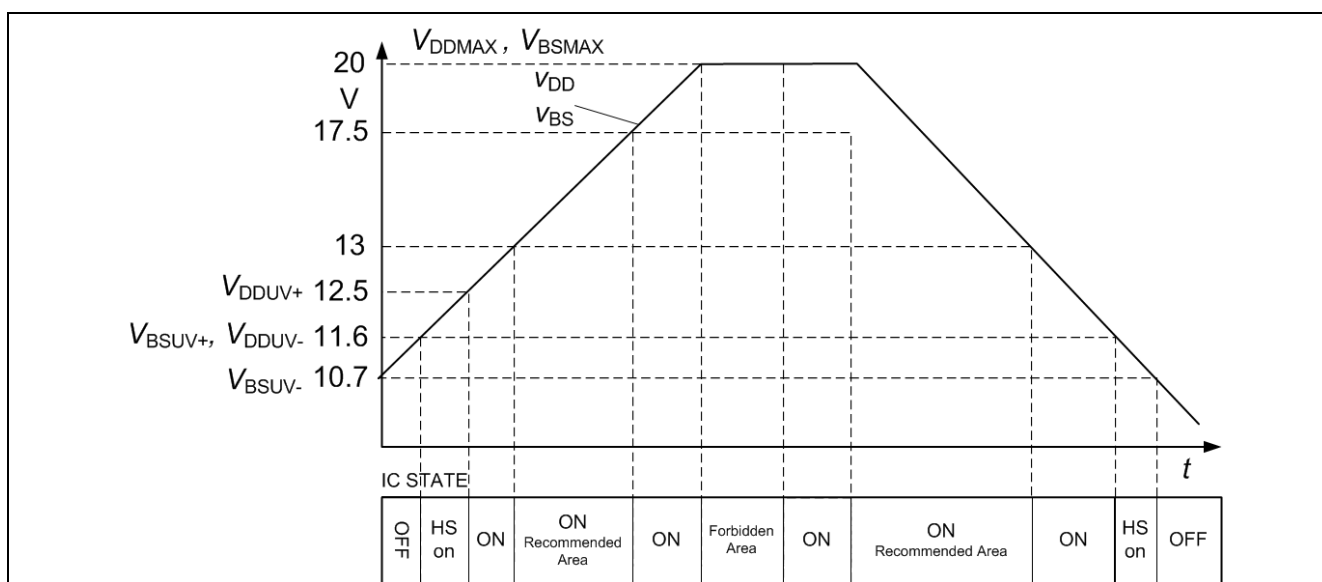


Figure 11 Operating areas (IGBT UVLO levels)

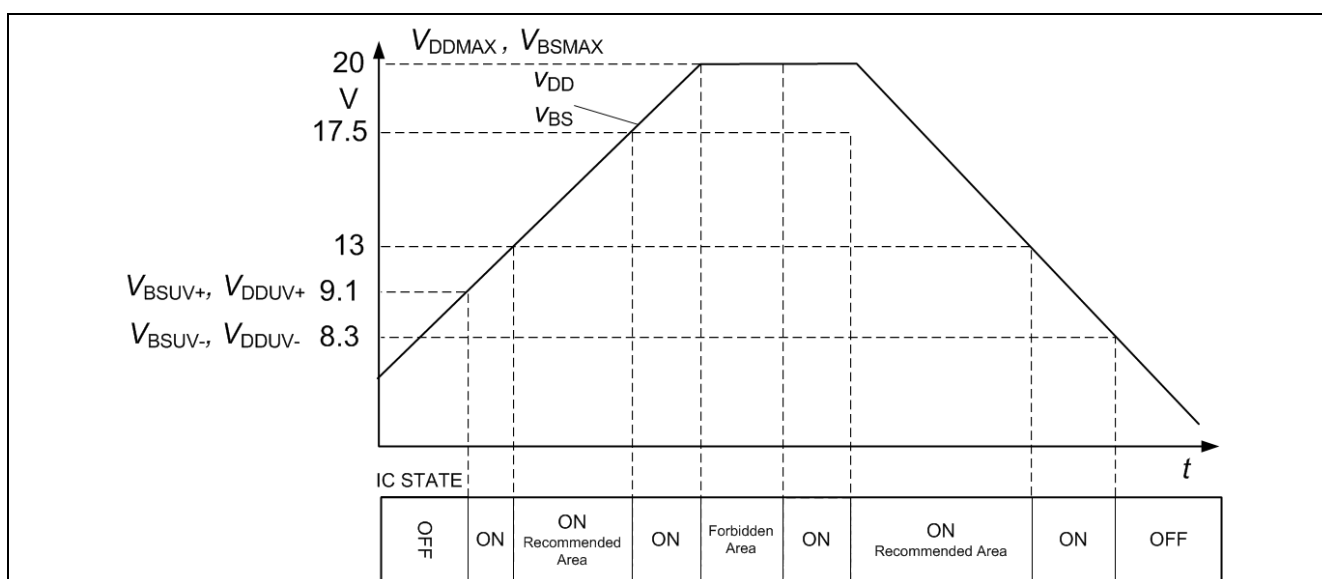


Figure 12 Operating areas (MOSFET UVLO levels)

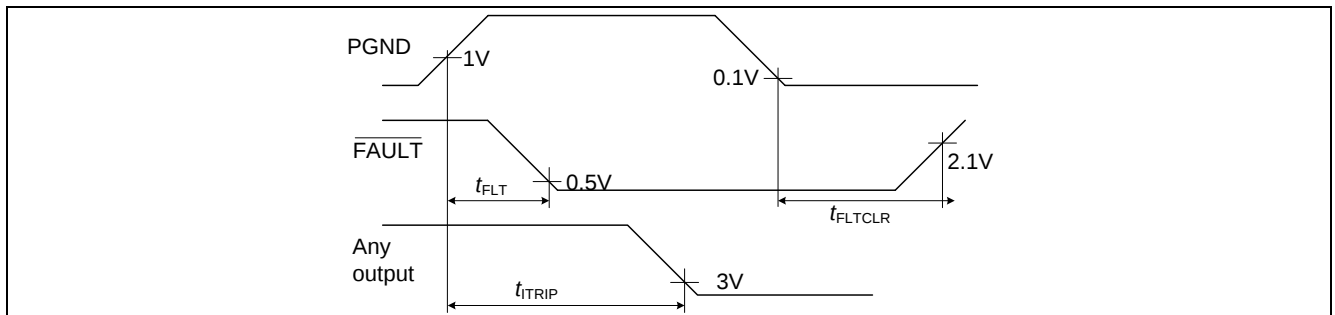


Figure 13 ITRIP-Timing

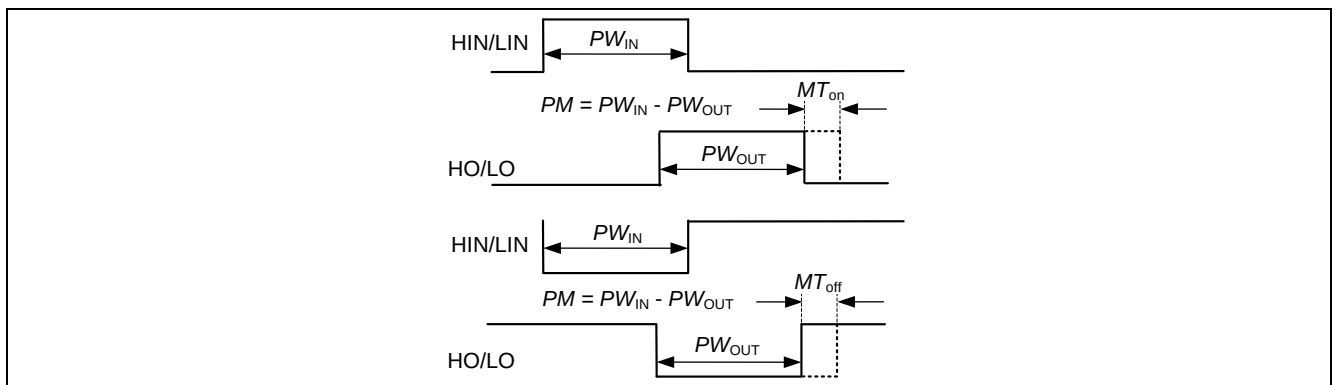


Figure 14 Output pulse width timing and matching delay timing diagram for positive logic

## 6 Package

### 6.1 PG-DSO-14

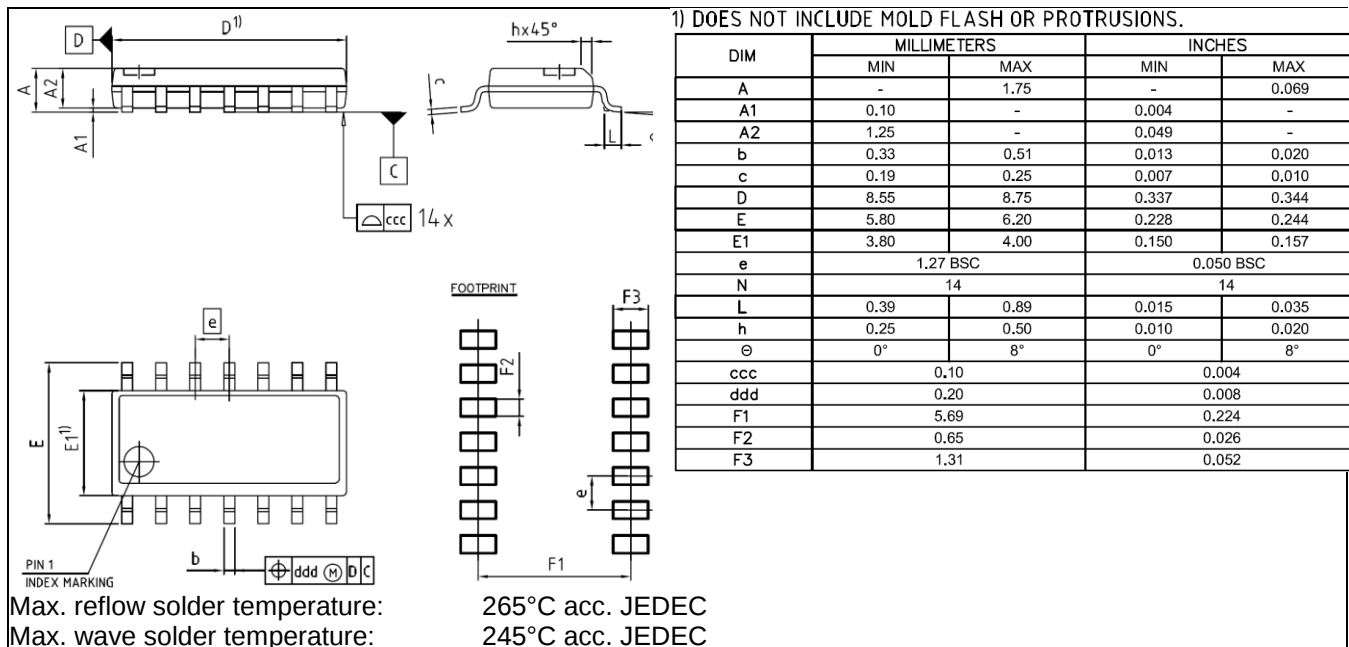


Figure 15 Package drawing

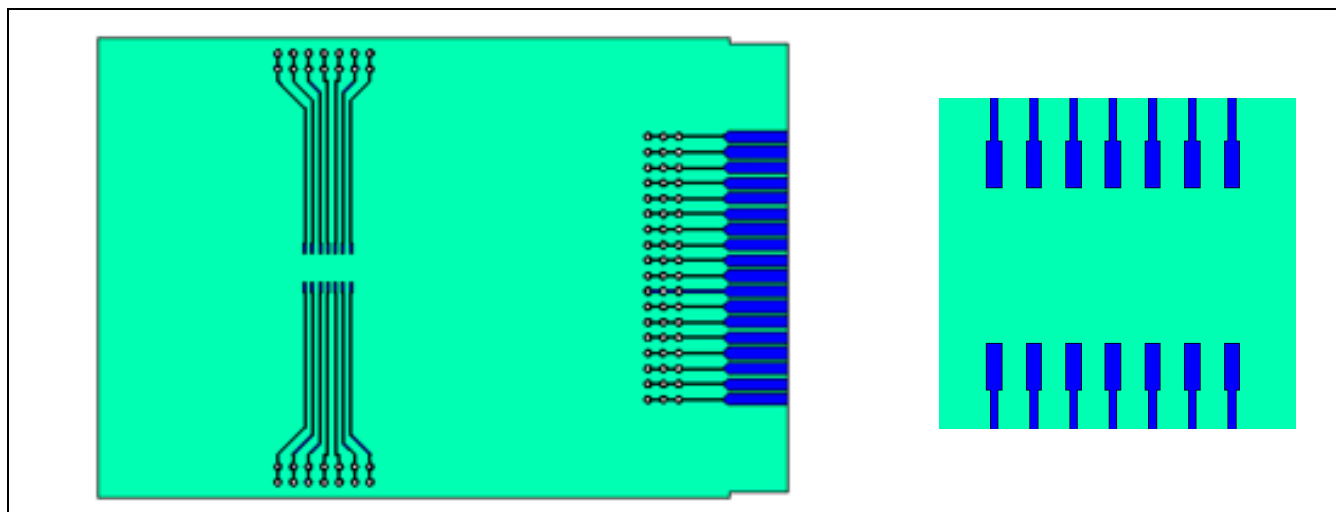


Figure 16 PCB reference layout (according to JEDEC 1s0P)  
left: Reference layout  
right: detail of footprint

The thermal coefficient is used to calculate the junction temperature, when the IC surface temperature is measured. The junction temperature is

$$T_j = \psi_{th(j-top)} \cdot P_d + T_{top}$$

Table 8 Data of reference layout

| Dimensions                         | Material                            | Metal (Copper)                       |
|------------------------------------|-------------------------------------|--------------------------------------|
| 76.2 × 114.3 × 1.5 mm <sup>3</sup> | FR4 ( $\lambda_{therm} = 0.3$ W/mK) | 70μm ( $\lambda_{therm} = 388$ W/mK) |

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