

IRF8113PbF

HEXFET® Power MOSFET

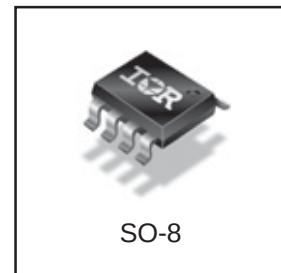
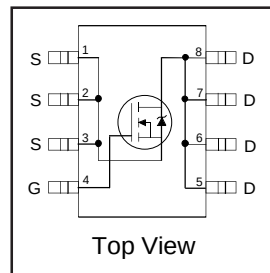
Applications

- Synchronous MOSFET for Notebook Processor Power
- Synchronous Rectifier MOSFET for Isolated DC-DC Converters in Networking Systems

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 100% Tested for R_G
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	Qg Typ.
30V	5.6m Ω @ $V_{GS} = 10V$	24nC



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	17.2	A
I_D @ $T_A = 70^\circ C$	Continuous Drain Current, V_{GS} @ 10V	13.8	
I_{DM}	Pulsed Drain Current ①	135	
P_D @ $T_A = 25^\circ C$	Power Dissipation ④	2.5	W
P_D @ $T_A = 70^\circ C$	Power Dissipation ④	1.6	
	Linear Derating Factor	0.02	W/ $^\circ C$
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	—	20	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient ④⑤	—	50	

Notes ① through ⑤ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.024	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.7	5.6	$m\Omega$	$V_{GS} = 10V, I_D = 17.2A$ ③
		—	5.8	6.8		$V_{GS} = 4.5V, I_D = 13.8A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.5	—	2.2	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	- 5.4	—	$mV/^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	73	—	—	S	$V_{DS} = 15V, I_D = 13.3A$
Q_g	Total Gate Charge	—	24	36	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 13.3A$ See Fig. 16
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	6.2	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.0	—		
Q_{gd}	Gate-to-Drain Charge	—	8.5	—		
Q_{godr}	Gate Charge Overdrive	—	7.3	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	10.5	—		
Q_{oss}	Output Charge	—	10	—	nC	$V_{DS} = 10V, V_{GS} = 0V$
R_G	Gate Resistance	—	0.8	1.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ ③ $I_D = 13.3A$ Clamped Inductive Load
t_r	Rise Time	—	8.9	—		
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		
t_f	Fall Time	—	3.5	—		
C_{iss}	Input Capacitance	—	2910	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	600	—		
C_{rss}	Reverse Transfer Capacitance	—	250	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	48	mJ
I_{AR}	Avalanche Current ①	—	13.3	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	135		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 13.3A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	34	51	ns	$T_J = 25^\circ\text{C}, I_F = 13.3A, V_{DD} = 10V$
Q_{rr}	Reverse Recovery Charge	—	21	32	nC	$di/dt = 100A/\mu s$ ③

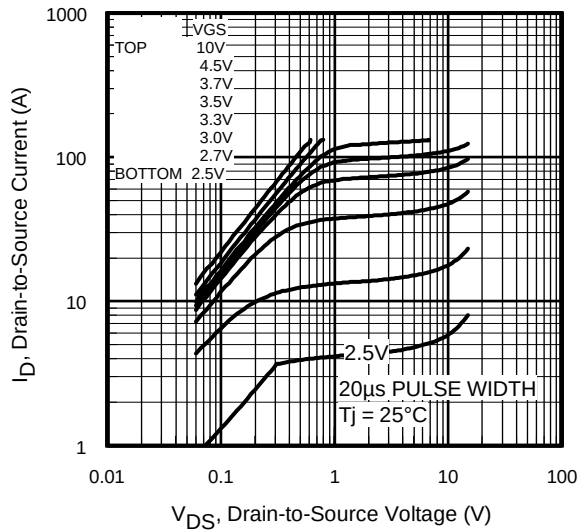


Fig 1. Typical Output Characteristics

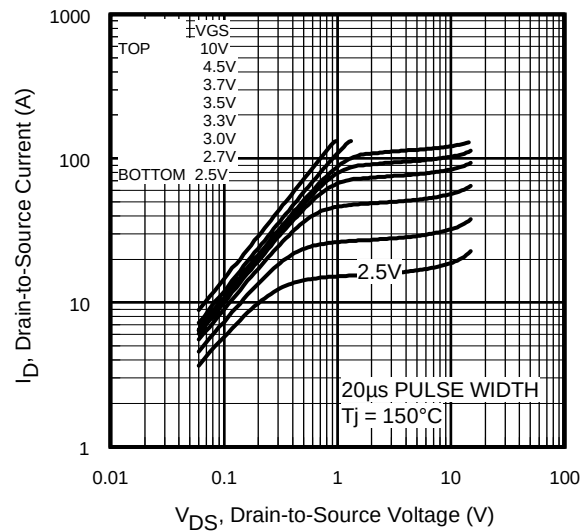


Fig 2. Typical Output Characteristics

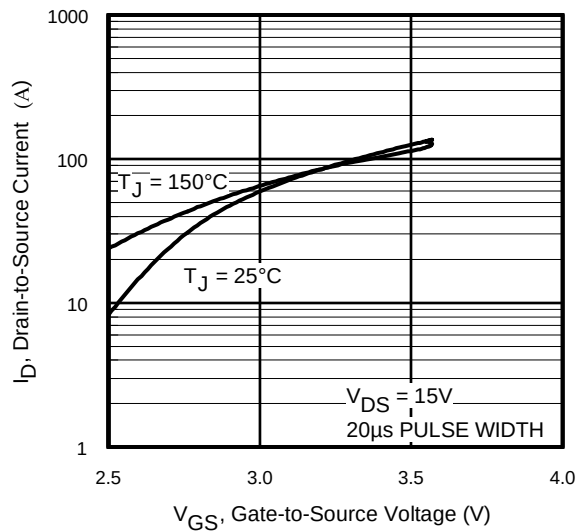


Fig 3. Typical Transfer Characteristics

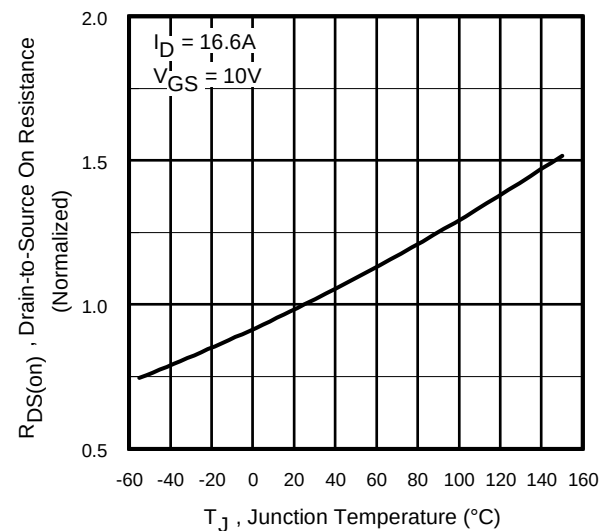


Fig 4. Normalized On-Resistance Vs. Temperature

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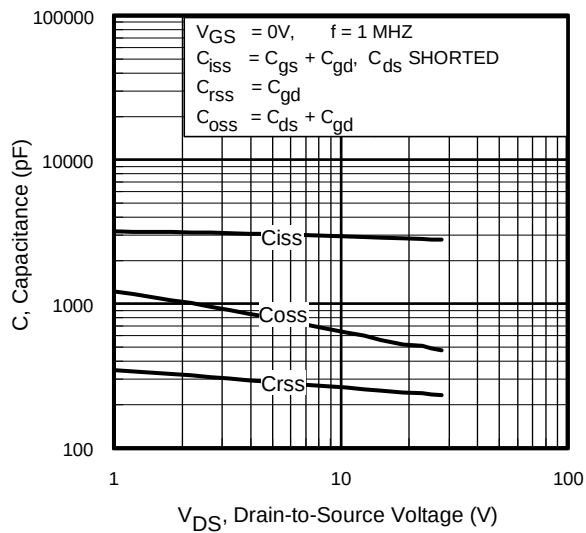


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

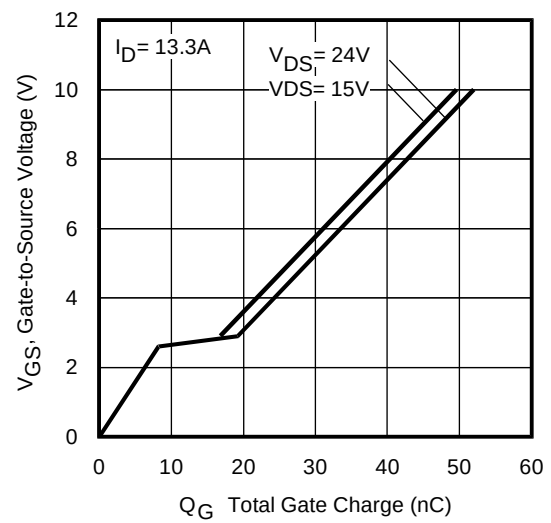


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

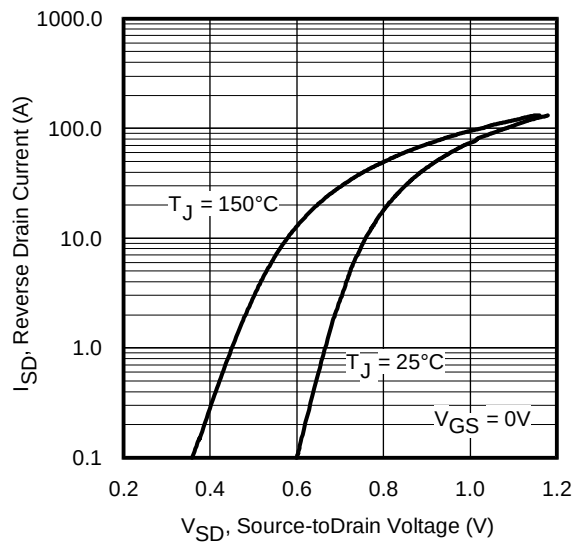


Fig 7. Typical Source-Drain Diode Forward Voltage

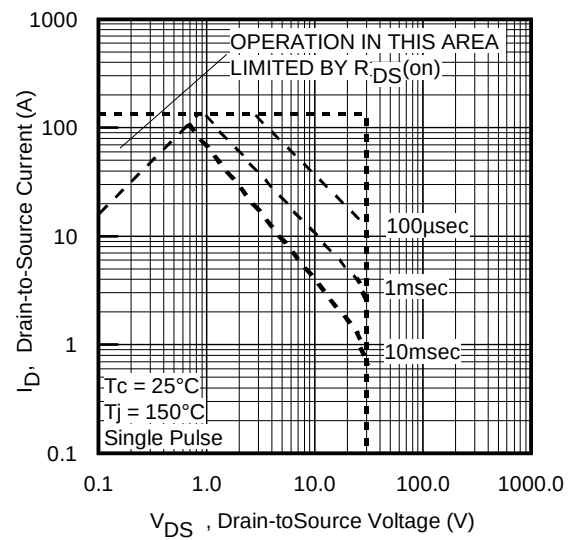
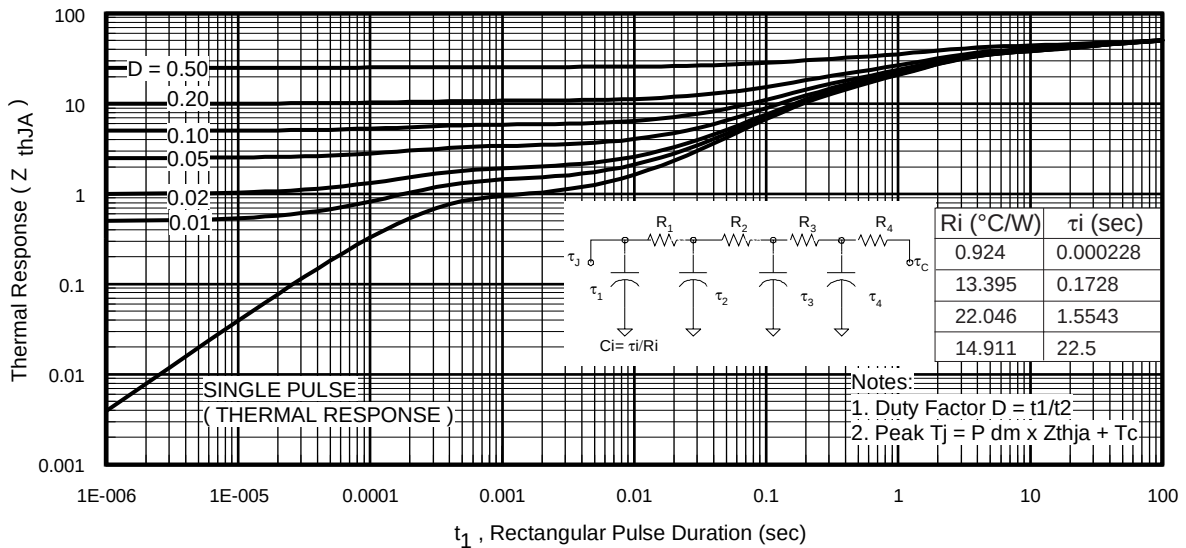
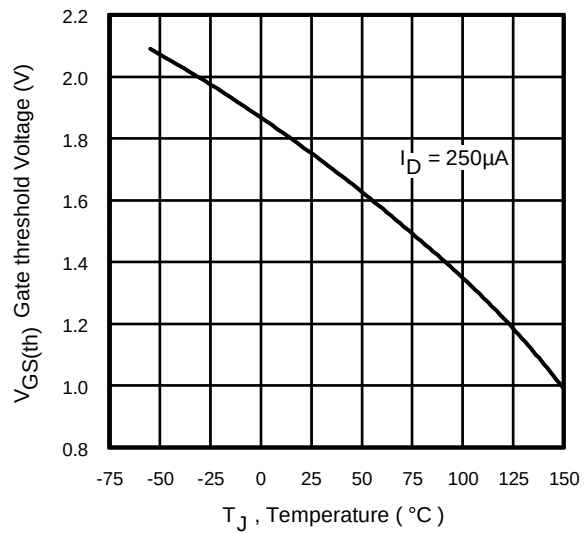
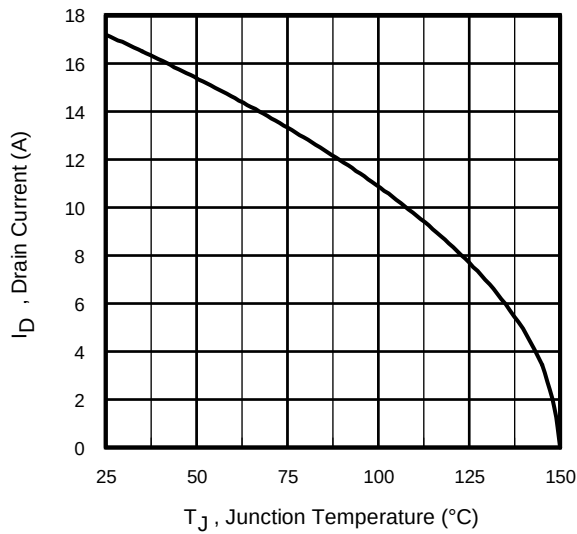


Fig 8. Maximum Safe Operating Area



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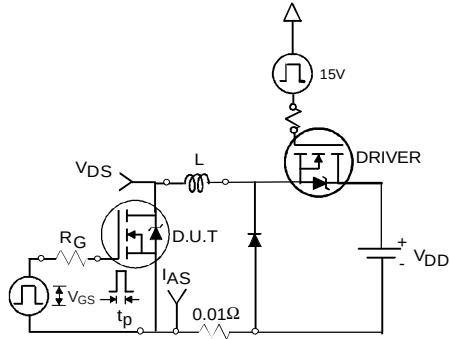


Fig 12a. Unclamped Inductive Test Circuit

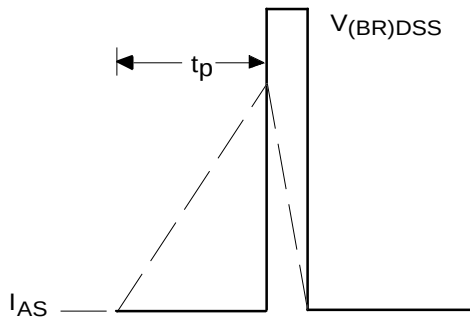


Fig 12b. Unclamped Inductive Waveforms

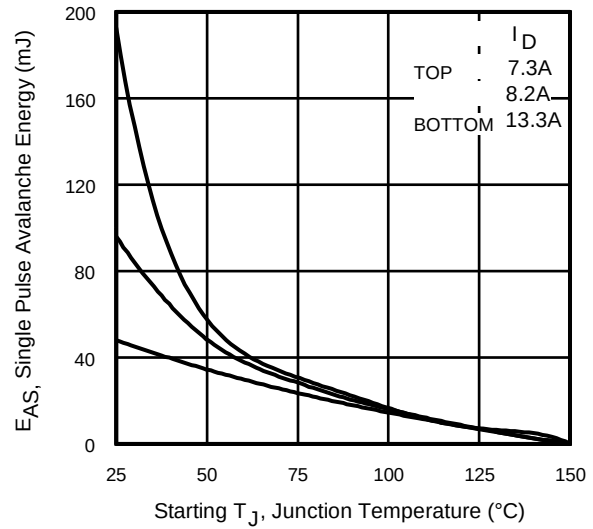


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

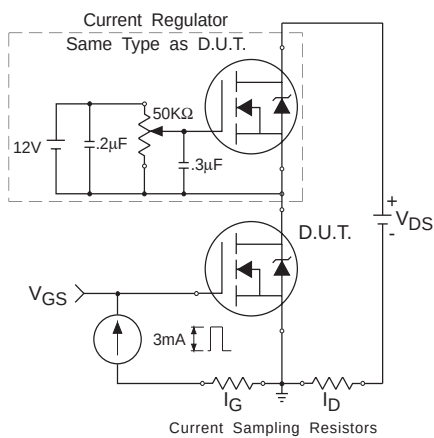


Fig 13. Gate Charge Test Circuit

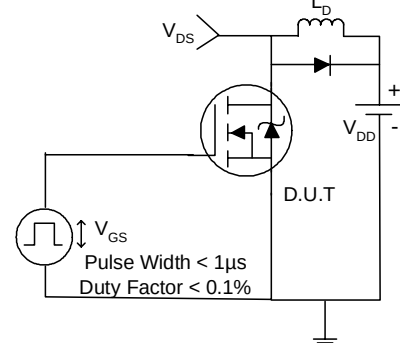


Fig 14a. Switching Time Test Circuit

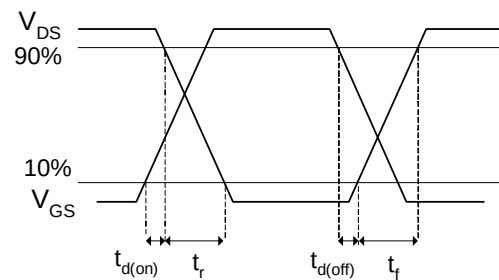


Fig 14b. Switching Time Waveforms

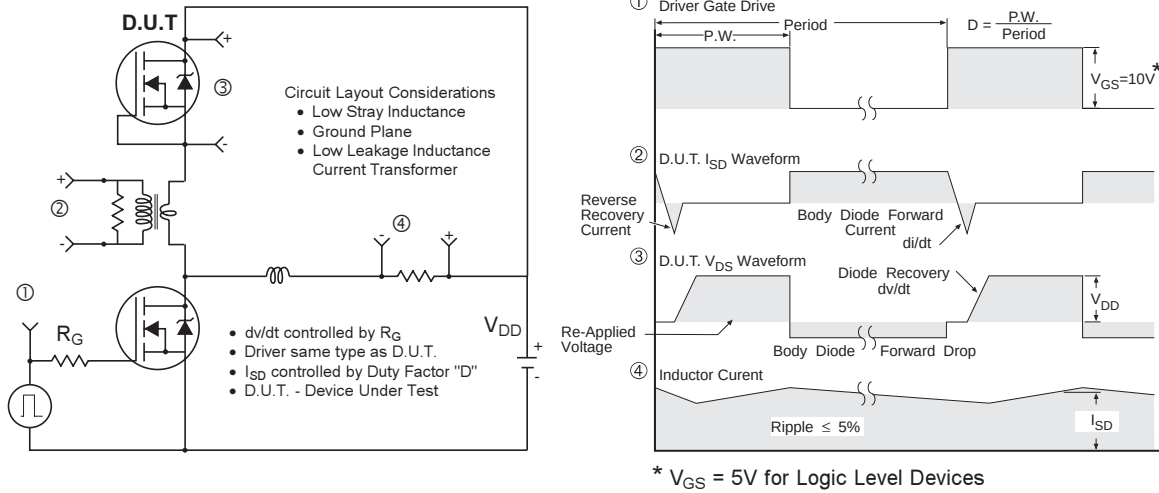


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETS

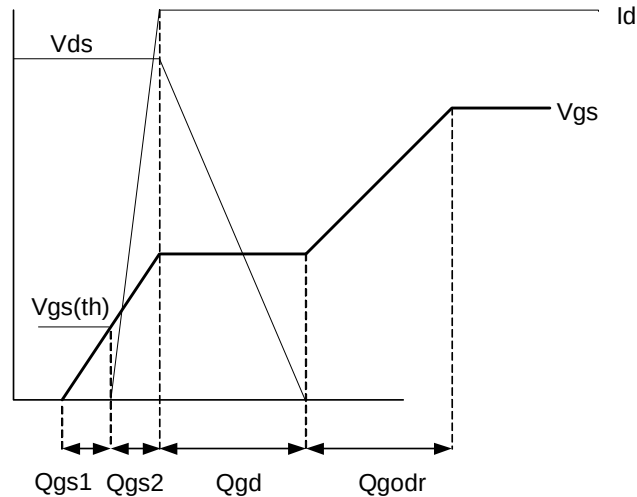


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2} , can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$

$$P_{loss} = (I_{rms}^2 \times R_{ds(on)}) + (Q_g \times V_g \times f) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in} . As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current. The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

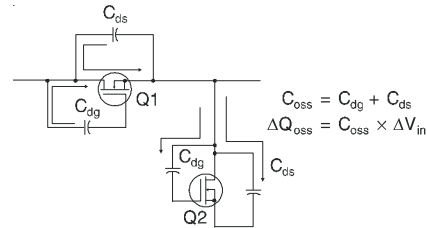
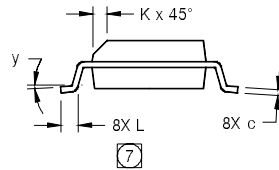


Figure A: Q_{oss} Characteristic

Technical drawing of a mechanical part showing dimensions and tolerances. The drawing includes a cross-section view of a component with a central hole and four smaller holes. Dimensions are given as $e1$ (hole diameter), $8 \times b$ (hole spacing), A (total height), and $A1$ (base height). A surface texture symbol indicates a roughness of $0.10 [0.04]$. A table at the bottom lists tolerances and material specifications.

Φ	0.25 [0.10]	$\textcircled{M}$	C	A	B
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FOOTPRINT

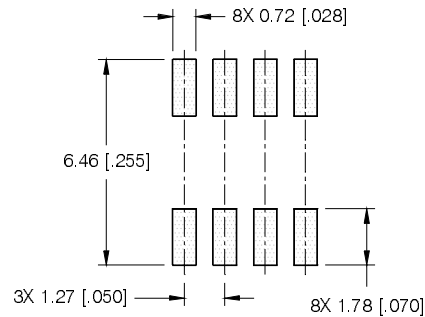


Diagram illustrating the markings on a TOR P7101 rectifier diode:

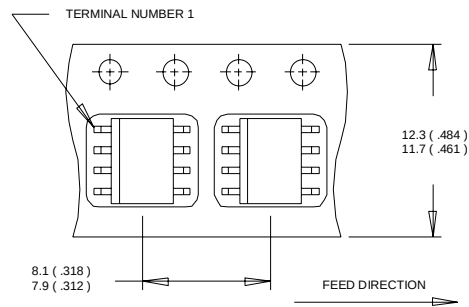
- INTERNATIONAL RECTIFIER LOGO**: Points to the TOR logo.
- DATE CODE (YWW)**: Points to the PYWWA marking.
- P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)**: Points to the 'P' in the date code.
- Y = LAST DIGIT OF THE YEAR**: Points to the 'Y' in the date code.
- WW = WEEK**: Points to the 'WW' in the date code.
- A = ASSEMBLY SITE CODE**: Points to the 'A' in the date code.
- LOT CODE**: Points to the XXXX marking.
- PART NUMBER**: Points to the F7101 marking.

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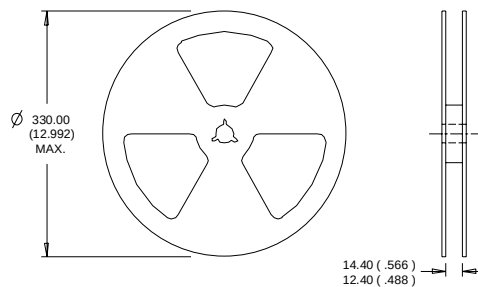
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SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.054\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 13.3\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ R_θ is measured at T_J approximately 90°C

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.

Qualification Standards can be found on IR's Web site.

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