

74LVC373A

Low-Voltage CMOS Octal Transparent Latch

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The 74LVC373A is a high performance, non-inverting octal transparent latch operating from a 1.2 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows 74LVC373A inputs to be safely driven from 5 V devices.

The 74LVC373A contains 8 D-type latches with 3-state outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are enabled. When \overline{OE} is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

Features

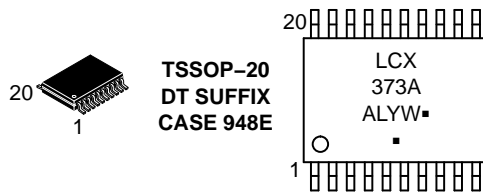
- Designed for 1.2 to 3.6 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- 24 mA Output Sink and Source Capability
- Near Zero Static Supply Current in all Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



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MARKING DIAGRAM



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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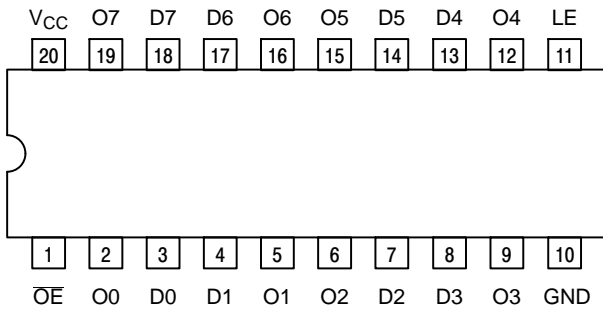


Figure 1. Pinout (Top View)

PIN NAMES

PINS	FUNCTION
OE	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

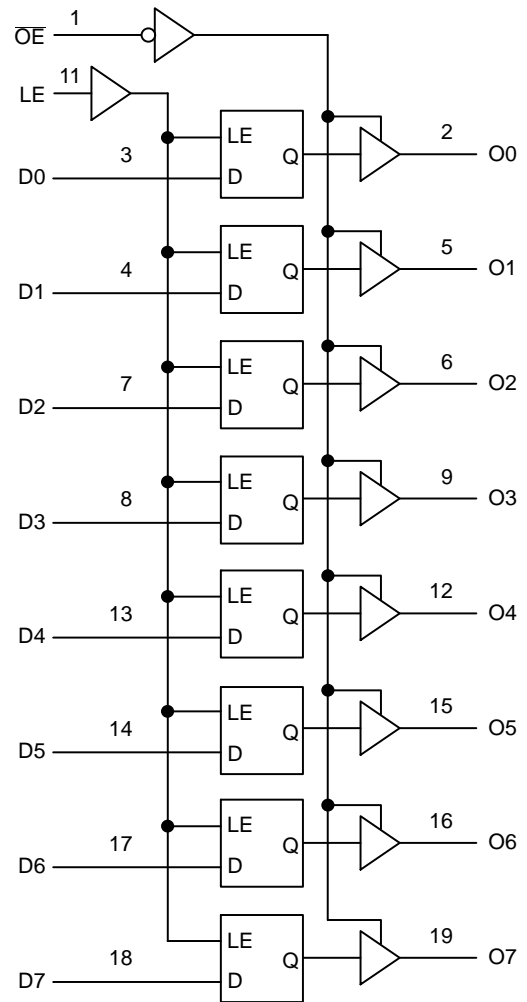


Figure 2. Logic Diagram

TRUTH TABLE

Inputs			Outputs		Operating Mode
OE	LE	Dn	On		
L	H	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	L	
L	L	h	H	H	Latched (Latch Enabled) Read Latch
L	L	l	L	L	
L	L	X	NC	NC	Hold; Read Latch
H	L	X	Z	Z	Hold; Disabled Outputs
H	H	H	Z	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	Z	
H	L	h	Z	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	Z	

H = High Voltage Level
 h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
 L = Low Voltage Level
 l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
 NC = No Change, State Prior to the Latch Enable High-to-Low Transition
 X = High or Low Voltage Level or Transitions are Acceptable
 Z = High Impedance State
 For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +6.5	V
V _I	DC Input Voltage		-0.5 ≤ V _I ≤ +6.5	V
V _O	DC Output Voltage	Output in 3-State	-0.5 ≤ V _O ≤ +6.5	V
		Output in HIGH or LOW State (Note 1)	-0.5 ≤ V _O ≤ V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	V _I < GND	-50	mA
I _{OK}	DC Output Diode Current	V _O < GND	-50	mA
		V _O > V _{CC}	+50	mA
I _O	DC Output Source/Sink Current		±50	mA
I _{CC}	DC Supply Current Per Supply Pin		±100	mA
I _{GND}	DC Ground Current Per Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		T _L = 260	°C
T _J	Junction Temperature Under Bias		T _J = 135	°C
θ _{JA}	Thermal Resistance (Note 2)		110.7	°C/W
MSL	Moisture Sensitivity	Level 1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage Operating Functional	1.65 1.2		3.6 3.6	V
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage HIGH or LOW State 3-State	0 0		V _{CC} 5.5	V
I _{OH}	HIGH Level Output Current V _{CC} = 3.0 V – 3.6 V V _{CC} = 2.7 V – 3.0 V			-24 -12	mA
I _{OL}	LOW Level Output Current V _{CC} = 3.0 V – 3.6 V V _{CC} = 2.7 V – 3.0 V			24 12	mA
T _A	Operating Free-Air Temperature	-40		+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{CC} = 1.65 to 2.7 V V _{CC} = 2.7 to 3.6 V	0 0		20 10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	-40 to +85°C			-40 to +125°C			Unit
			Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	–	–	1.08	–	–	V
		V _{CC} = 1.65 V to 1.95 V	0.65 x V _{CC}	–	–	0.65 x V _{CC}	–	–	
		V _{CC} = 2.3 V to 2.7 V	1.7	–	–	1.7	–	–	
		V _{CC} = 2.7 V to 3.6 V	2.0	–	–	2.0	–	–	
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	–	–	0.12	–	–	0.12	V
		V _{CC} = 1.65 V to 1.95 V	–	–	0.35 x V _{CC}	–	–	0.35 x V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	–	–	0.7	–	–	0.7	
		V _{CC} = 2.7 V to 3.6 V	–	–	0.8	–	–	0.8	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}							V
		I _O = –100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} – 0.2	–	–	V _{CC} – 0.3	–	–	
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	–	–	1.05	–	–	
		I _O = –8 mA; V _{CC} = 2.3 V	1.8	–	–	1.65	–	–	
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	–	–	2.05	–	–	
		I _O = –18 mA; V _{CC} = 3.0 V	2.4	–	–	2.25	–	–	
		I _O = –24 mA; V _{CC} = 3.0 V	2.2	–	–	2.0	–	–	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}							V
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	–	–	0.2	–	–	0.3	
		I _O = 4 mA; V _{CC} = 1.65 V	–	–	0.45	–	–	0.65	
		I _O = 8 mA; V _{CC} = 2.3 V	–	–	0.6	–	–	0.8	
		I _O = 12 mA; V _{CC} = 2.7 V	–	–	0.4	–	–	0.6	
		I _O = 24 mA; V _{CC} = 3.0 V	–	–	0.55	–	–	0.8	
I _I	Input leakage current	V _I = 5.5 V or GND; V _{CC} = 3.6 V	–	±0.1	±5	–	±0.1	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	–	±0.1	±5	–	±0.1	±20	μA
I _{OFF}	Power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0.0 V	–	±0.1	±10	–	±0.1	±20	μA
I _{CC}	Supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V	–	0.1	10	–	0.1	40	μA
ΔI _{CC}	Additional supply current	per input pin; V _I = V _{CC} – 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V	–	5	500	–	5	5000	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. All typical values are measured at T_A = 25°C and V_{CC} = 3.3 V, unless stated otherwise.

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AC ELECTRICAL CHARACTERISTICS ($t_R = t_F = 2.5 \text{ ns}$)

Symbol	Parameter	Conditions	-40 to +85°C			-40 to +125°C			Unit
			Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
t _{pd}	Propagation Delay (Note 5) Dn to On	V _{CC} = 1.2 V	–	14.0	–	–	–	–	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.5	15.8	1.5	–	18.2	
		V _{CC} = 2.3 V to 2.7 V	1.0	3.4	8.2	1.0	–	9.4	
		V _{CC} = 2.7 V	1.5	3.4	7.8	1.5	–	10.0	
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	6.8	1.5	–	8.5	
t _{pd}	Propagation Delay LE to On	V _{CC} = 1.2 V	–	16.0	–	–	–	–	ns
		V _{CC} = 1.65 V to 1.95 V	2.2	7.3	16.8	2.2	–	19.3	
		V _{CC} = 2.3 V to 2.7 V	1.5	3.9	8.6	1.5	–	10.0	
		V _{CC} = 2.7 V	1.5	3.5	8.2	1.5	–	10.5	
		V _{CC} = 3.0 V to 3.6 V	1.5	3.3	7.2	1.5	–	9.0	
t _{en}	Enable Time (Note 6) OE to On	V _{CC} = 1.2 V	–	17.0	–	–	–	–	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.8	17.6	1.5	–	20.3	
		V _{CC} = 2.3 V to 2.7 V	1.5	3.8	9.7	1.5	–	11.2	
		V _{CC} = 2.7 V	1.5	3.8	8.7	1.5	–	11.0	
		V _{CC} = 3.0 V to 3.6 V	1.5	3.1	7.7	1.5	–	10.0	
t _{dis}	Disable Time (Note 7) OE to On	V _{CC} = 1.2 V	–	8.0	–	–	–	–	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	4.3	10.3	1.5	–	11.9	
		V _{CC} = 2.3 V to 2.7 V	1.0	2.4	5.8	1.0	–	6.8	
		V _{CC} = 2.7 V	1.5	3.2	7.1	1.5	–	9.0	
		V _{CC} = 3.0 V to 3.6 V	1.5	3.0	6.1	1.5	–	8.0	
t _w	Pulse Width LE HIGH	V _{CC} = 1.65 V to 1.95 V	5.0	–	–	5.0	–	–	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	–	–	4.0	–	–	ns
		V _{CC} = 2.7 V	3.0	–	–	3.0	–	–	
		V _{CC} = 3.0 V to 3.6 V	3.0	1.5	–	3.0	–	–	
t _{su}	Set-up Time On to LE	V _{CC} = 1.65 V to 1.95 V	4.0	–	–	4.0	–	–	ns
		V _{CC} = 2.3 V to 2.7 V	3.0	–	–	3.0	–	–	
		V _{CC} = 2.7 V	2.0	–	–	2.0	–	–	
		V _{CC} = 3.0 V to 3.6 V	2.0	0.0	–	2.0	–	–	
t _h	Hold Time On to LE	V _{CC} = 1.65 V to 1.95 V	3.0	–	–	3.0	–	–	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	–	–	2.0	–	–	
		V _{CC} = 2.7 V	1.5	–	–	1.5	–	–	
		V _{CC} = 3.0 V to 3.6 V	1.5	0.3	–	1.5	–	–	
t _{sk(0)}	Output Skew Time (Note 8)		–	–	1.0	–	–	1.5	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical values are measured at T_A = 25°C and V_{CC} = 3.3 V, unless stated otherwise.

5. t_{pd} is the same as t_{PLH} and t_{PHL}.

6. t_{en} is the same as t_{PZL} and t_{PZH}.

7. t_{dis} is the same as t_{PLZ} and t_{PHZ}.

8. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
VOLP	Dynamic LOW Peak Voltage (Note 9)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.8 0.6		V
VOLV	Dynamic LOW Valley Voltage (Note 9)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		-0.8 -0.6		V

9. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
CIN	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	5.0	pF
COUT	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	6.0	pF
CPD	Power Dissipation Capacitance (Note 10)	Per flip-flop; V _I = GND or V _{CC}		pF
		V _{CC} = 1.65 V to 1.95 V	16.6	
		V _{CC} = 2.3 V to 2.7 V	19.2	
		V _{CC} = 3.0 V to 3.6 V	21.6	

10. CPD is used to determine the dynamic power dissipation (PD in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

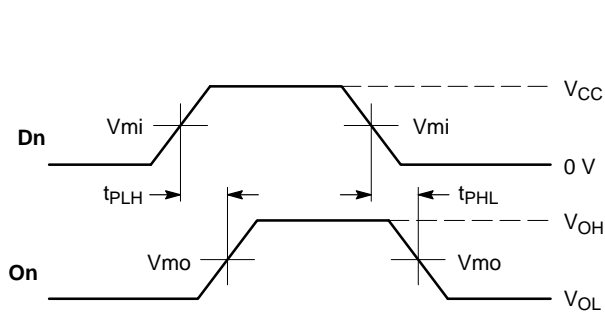
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

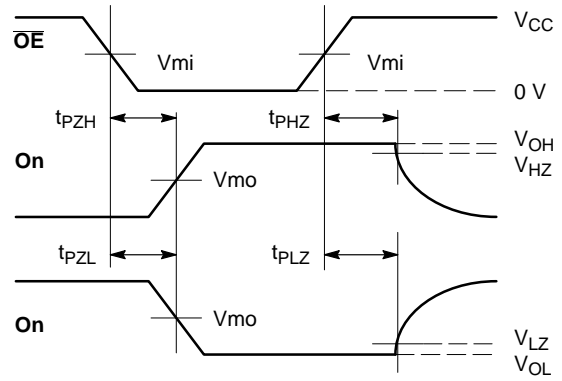
N = number of outputs switching

∑(C_L × V_{CC}² × f_o) = sum of the outputs

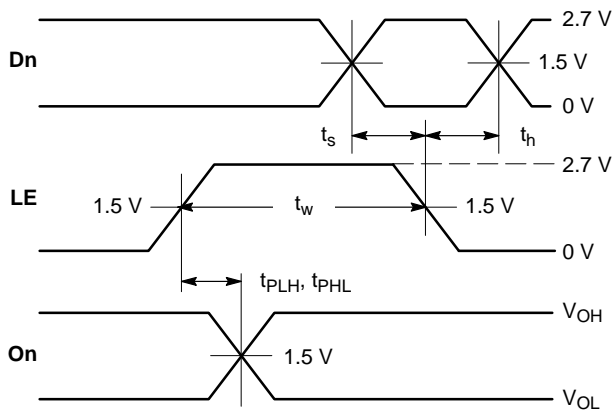
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WAVEFORM 1 – PROPAGATION DELAYS
 $t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$

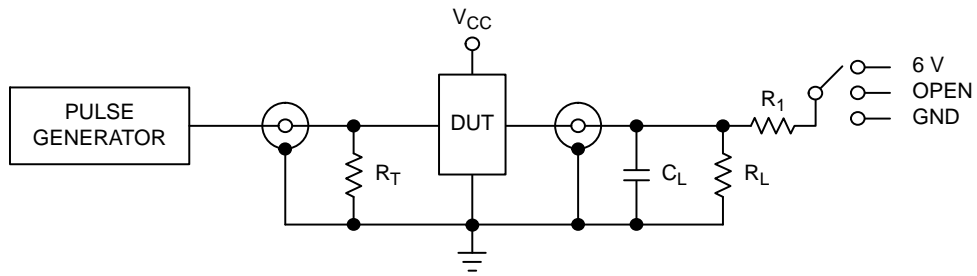


WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
 $t_R = t_F = 2.5 \text{ ns}$, 10% to 90%; $f = 1 \text{ MHz}$; $t_W = 500 \text{ ns}$ except when noted

Symbol	V _{CC}		
	3.3 V ± 0.3 V	2.7 V	V _{CC} < 2.7 V
V _{mi}	1.5 V	1.5 V	V _{CC} /2
V _{mo}	1.5 V	1.5 V	V _{CC} /2
V _{HZ}	V _{OL} + 0.3 V	V _{OL} + 0.3 V	V _{OL} + 0.15 V
V _{LZ}	V _{OH} - 0.3 V	V _{OH} - 0.3 V	V _{OH} - 0.15 V

Figure 3. AC Waveforms

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C_L includes jig and probe capacitance
 $R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)
 $R_1 = R_L$

Supply Voltage	Input		Load		VEXT		
V_{CC} (V)	V_I	t_r, t_f	C_L	R_L	tPLH, tPHL	tPLZ, tPZL	tPHZ, tPZH
1.2	V_{CC}	≤ 2 ns	30 pF	1 k Ω	Open	2 x V_{CC}	GND
1.65 – 1.95	V_{CC}	≤ 2 ns	30 pF	1 k Ω	Open	2 x V_{CC}	GND
2.3 – 2.7	V_{CC}	≤ 2 ns	30 pF	500 Ω	Open	2 x V_{CC}	GND
2.7	2.7 V	≤ 2.5 ns	50 pF	500 Ω	Open	2 x V_{CC}	GND
3.0 – 3.6	2.7 V	≤ 2.5 ns	50 pF	500 Ω	Open	2 x V_{CC}	GND

Figure 4. Test Circuit

ORDERING INFORMATION

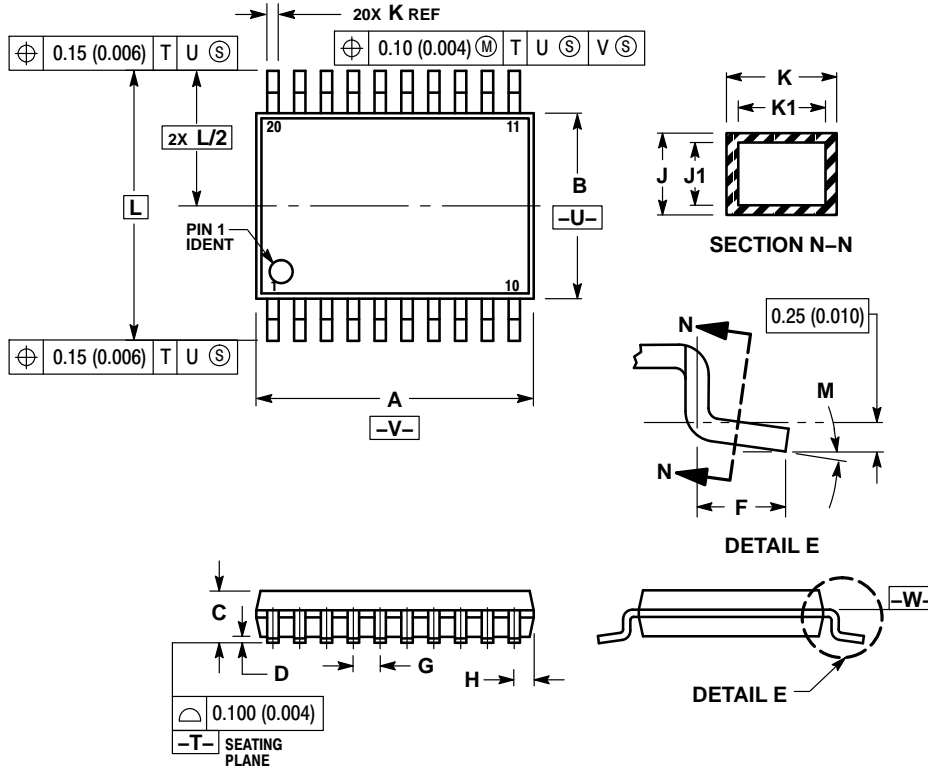
Device	Package	Shipping [†]
74LVC373ADTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE C

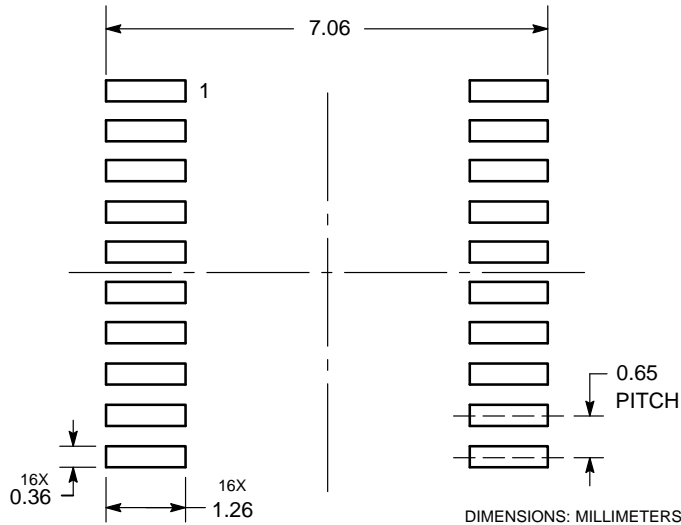


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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