

# Spread Spectrum Clock Generator

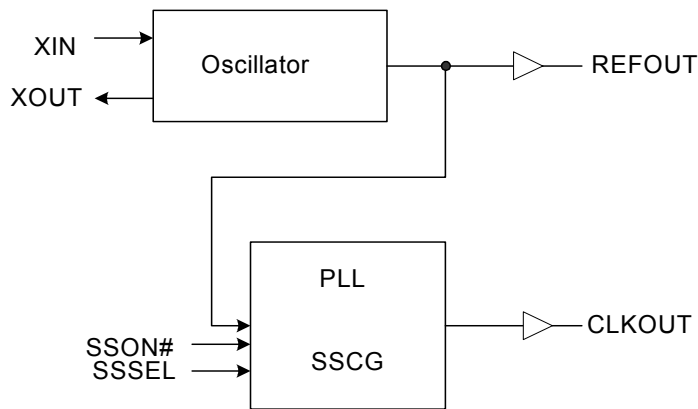
## Features

- Supports clock requirements for printers
- 48-MHz spread spectrum clock output
- 48-MHz reference clock output
- Two selectable spread percentages: -1% and -3%
- Integrated loop filter
- 48-MHz crystal or external clock input
- 3.3-V supply operation (2.5-V functional)
- 8-pin small outline integrated circuit (SOIC) package

## Functional Description

The CY27020 clock generator provides a low EMI clock output for printers. It features spread spectrum technology, a modulation technique designed specifically for reducing EMI at the fundamental frequency and its harmonics.

## Logic Block Diagram

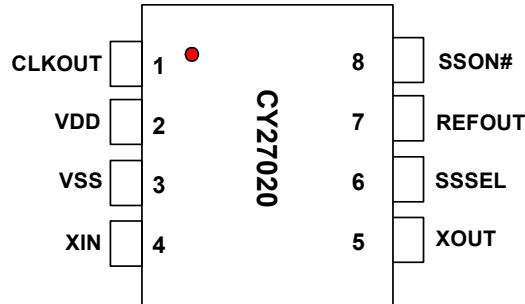


**Table 1. Frequency Table**

XIN	SSON#	SSSEL	REFOUT	CLKOUT
48.00 MHz	0	0	48.00 MHz	48.00 MHz at -1%
48.00 MHz	0	1	48.00 MHz	48.00 MHz at -3%
48.00 MHz	1	0	48.00 MHz	48.00 MHz (No Spread)
48.00 MHz	1	1	48.00 MHz	48.00 MHz (No Spread)

## Pin Configuration

Figure 1. Pin Diagram – CY27020 8-Pin SOIC Package



## Pin Description

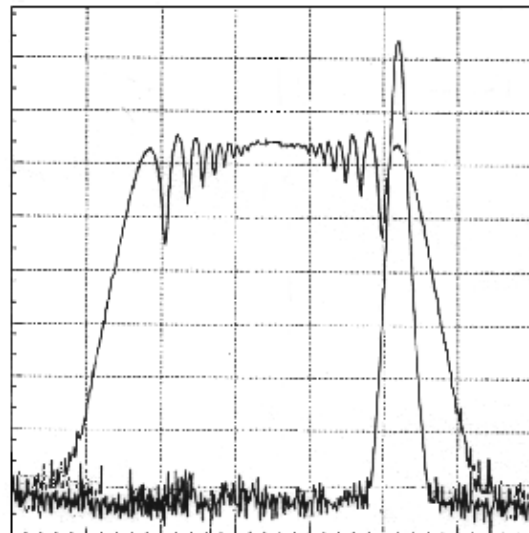
Pin	Name	I/o	Type <sup>[1]</sup>	Description
1	CLKOUT	O		Fixed frequency 48.00 MHz spread spectrum clock output. See <a href="#">Table 1</a> on page 1 for frequency selections
2	VDD	PWR		3.3-V power supply
3	VSS	PWR		Ground
4	XIN	I		Oscillator buffer input. Connect to an external parallel resonant crystal (nominally 48.00 MHz) or externally generated 48 MHz reference clock.
5	XOUT	O		Oscillator buffer output. Connect to an external parallel resonant crystal. Do not connect when an externally generated reference clock is applied at XIN.
6	SSSEL	I	PU	Spread spectrum percentage select input. See <a href="#">Table 1</a> on page 1 for details.
7	REFOUT	O	–	Buffered output of XIN.
8	SSON#	I	PD	Spread spectrum enable input. When asserted LOW, spread spectrum is enabled.

## Spread Spectrum Clock Generation (SSCG)

Spread spectrum clock generation (SSCG) is a frequency modulation technique used to reduce electromagnetic interference radiation generated by repetitive digital signals, mainly clocks. A clock accumulates electromagnetic energy at its center frequency and its harmonics. Spread spectrum distributes this energy over a small frequency band and decreases the peak value of radiated energy over the spectrum. This technique is achieved by modulating the clock around or below the center of its nominal frequency by a certain percentage (which also determines the energy distribution band).

The SSCG function is enabled when SSON# pin is asserted low, resulting in a spread bandwidth that is down spread by either –1% or –3%, selected by SSSEL (see [Table 1](#) on page 1).

Figure 2. No Spread vs Down Spread Example



**Note**

1. PU = Internal pull-up resistor, PD = Internal pull-down resistor.

### Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.<sup>[2]</sup>

- Minimum input voltage relative to V<sub>SS</sub>: ..... V<sub>SS</sub> – 0.3 V
- Maximum input voltage relative to V<sub>DD</sub>: ..... V<sub>DD</sub> + 0.3 V
- Storage temperature: ..... –65 °C to 150 °C
- Operating temperature: ..... 0 °C to 70 °C
- Maximum electrostatic discharge (ESD) protection: ..... 2 kV
- Maximum power supply: ..... 5.5 V
- Operating voltage: ..... 2.5 V–3.6 V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, care should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, the I/O pins should be constrained to the range:

$$V_{SS} < I/O < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>SS</sub> or V<sub>DD</sub>).

### DC Electrical Specifications (V<sub>DD</sub> = 3.3V ± 10%, T<sub>A</sub> = 0°C to 70°C)<sup>[3]</sup>

Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage	SSON#, SSSEL	–	–	0.8	V
V <sub>IH</sub>	Input high voltage		2.2	–	–	V
V <sub>thXIN</sub>	XIN threshold voltage		0.3 × V <sub>DD</sub>	0.5 × V <sub>DD</sub>	0.7 × V <sub>DD</sub>	V
I <sub>IL1</sub>	Input low current	SSON# = V <sub>SS</sub>	–5	0	5	μA
I <sub>IH1</sub>	Input high current	SSON# = V <sub>DD</sub>	3	8	20	μA
I <sub>IL2</sub>	Input low current	SSEL = V <sub>SS</sub>	–36	–16.5	–7.4	μA
I <sub>IH2</sub>	Input high current	SSEL = V <sub>DD</sub>	–5	0	5	μA
I <sub>DD3.3V</sub>	Dynamic supply current	No output load	–	20	25	mA
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 4.0 mA	–	–	0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = –4.0 mA	2.4	–	–	V
C <sub>in</sub>	Input capacitance	Pins 6 and 8	–	3	5	pF
C <sub>x</sub>	XIN, XOUT capacitance	Pins 4 and 5	–	3	5	pF
PU/PD	Pull-up/pull-down resistance	SSON#, SSSEL	100	200	400	kΩ

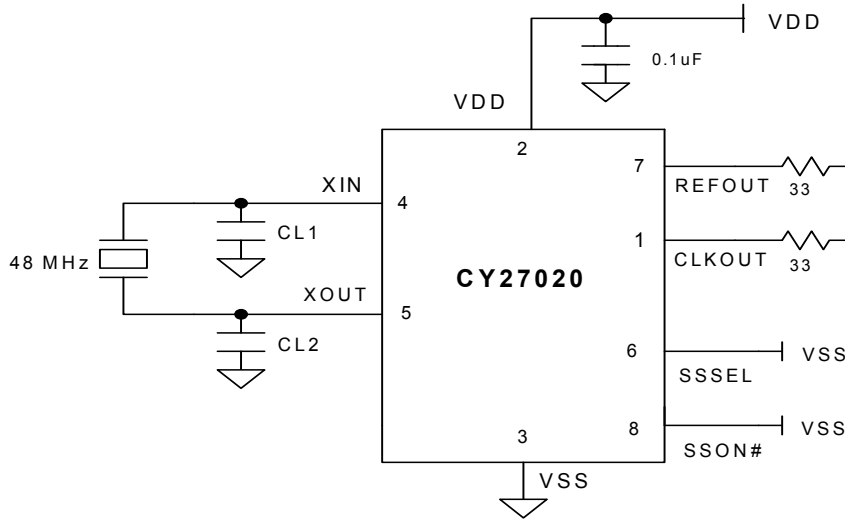
### AC Electrical Specifications (V<sub>DD</sub> = 3.3V ± 10%, T<sub>A</sub> = 0°C to 70°C)

Parameter	Description	Conditions	Min	Typ	Max	Unit
IFR	Input frequency range		44	48	52	MHz
t <sub>r</sub>	Rise time <sup>[4,5]</sup>		–	1	2	ns
t <sub>f</sub>	Fall time <sup>[4,5]</sup>		–	1	2	ns
SS%	Spread spectrum percentage	SSON# = 0, SSSEL = 0	–	–1	–	%
		SSON# = 0, SSSEL = 1	–	–3	–	%
t <sub>PU</sub>	Power-up to stable output <sup>[6]</sup>	All output clocks	–	–	3	ms
t <sub>DC</sub>	Clock duty cycle <sup>[4,6]</sup>	CL = 15 pF	45	50	55	%
t <sub>CCJ</sub>	REFOUT cycle-to-cycle jitter <sup>[4,6]</sup>	CL = 15 pF	–	–	350	ps
	CLKOUT cycle-to-cycle jitter <sup>[4,6]</sup>		–	100	250	ps

**Notes**

2. Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. In applications where a crystal is used for the input reference clock, refer to the crystal manufacturer's specifications for the required crystal load capacitor value.
4. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs. All outputs loaded with 15 pF.
5. Measured between 0.1 × V<sub>DD</sub> and 0.9 × V<sub>DD</sub> volts.
6. Triggering is done at 1.5 V.

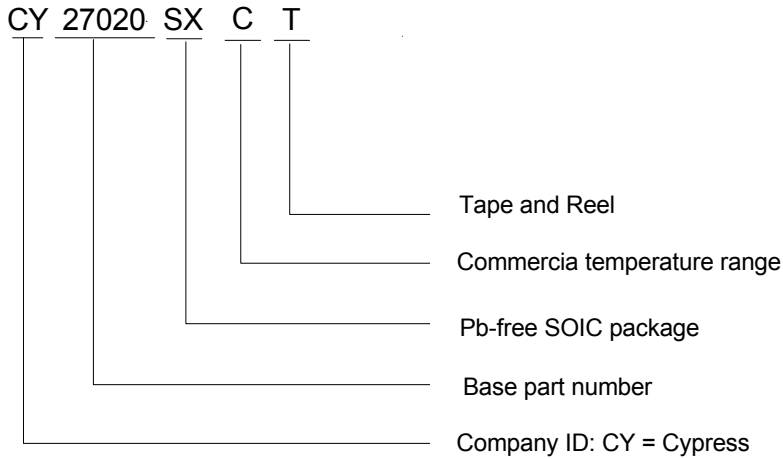
Figure 2. Application Schematic Example<sup>[7,8]</sup>



Ordering Information

Part Number	Package Type	Production Flow
<b>Pb-free</b>		
CY27020SXC	8-pin SOIC	Commercial, 0 °C to 70 °C
CY27020SXCT	8-pin SOIC - Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions

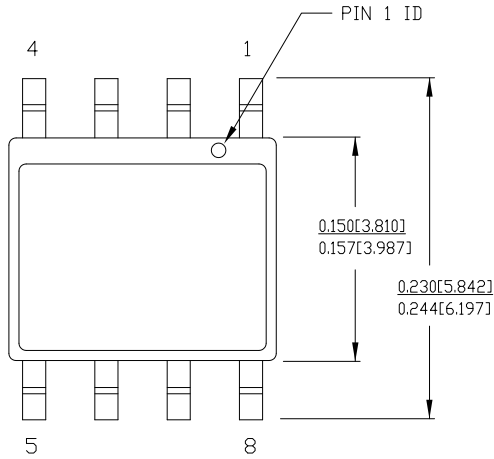


Notes

- 7. The circuit shows -1.0% spread. Refer to Table 1 on page 1 for details.
- 8. Use the crystal manufacturer's recommended values for CL1 and CL2 load capacitors.

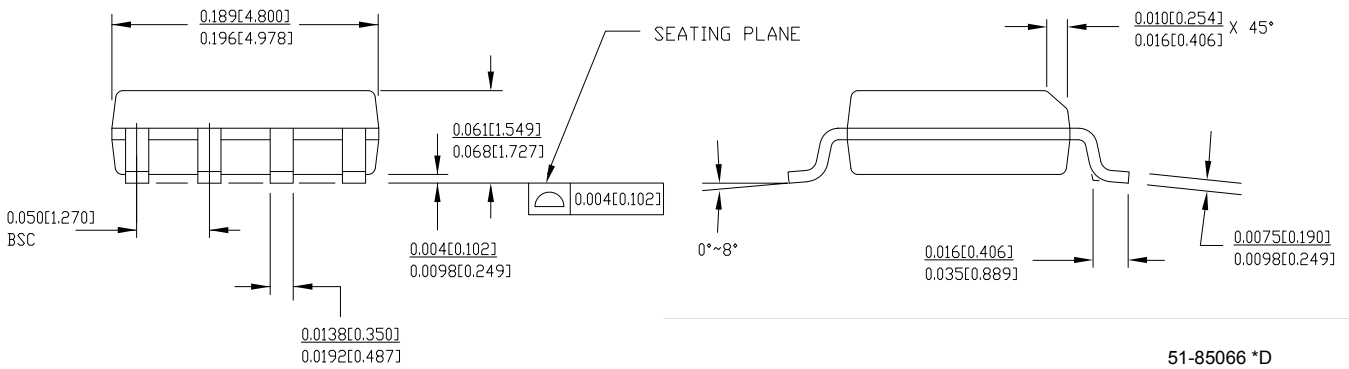
Package Drawing and Dimension

Figure 3. 8-Pin (150-Mil) SOIC



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG.
SZ08.15	LEAD FREE PKG.



## Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
CLKOUT	Reference clock out
EMI	Electromagnetic interference
ESD	Electrostatic discharge
OE	Output enable
PD	Power down
PLL	Phase locked loop
PPM	Parts per million
SS	Spread spectrum
SSC	spread spectrum clock
SSCG	spread spectrum clock generation
SSON	spread spectrum ON

## Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilo ohm
μA	microamperes
μs	microsecond
mA	milliamperes
ms	millisecond
mW	milliwatt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	pico Farad
ps	pico second
V	volts
W	watts

## Document History Page

Document Title: CY27020 Spread Spectrum Clock Generator Document Number: 38-07273				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	110661	02/19/02	XHT	New data sheet
*A	122868	12/21/02	RBI	Add power up requirements to maximum rating information
*B	279429	See ECN	RGL	Added Lead-free Devices
*C	2759365	09/02/2009	TSAI	Updated template. Post to external web.
*D	2899304	03/25/2010	CXQ	Removed inactive parts from <a href="#">Ordering Information</a> Updated <a href="#">Package Drawing and Dimension</a> .
*E	3041840	09/29/2010	CXQ	Removed "IC" from end of document title. Fixed various formatting and typographical errors. Change all SSON pin references to SSON#. Added row to Table 1 for explicit select pin functional explanation. Removed references to Cera-lock input. Removed redundant Note 3.

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