



# PMDPB56XNEA

30 V, dual N-channel Trench MOSFET

19 April 2016

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Leadless medium power SMD plastic package:  $2 \times 2 \times 0.65$  mm
- Tin-plated 100 % solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

## 3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

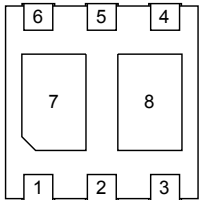
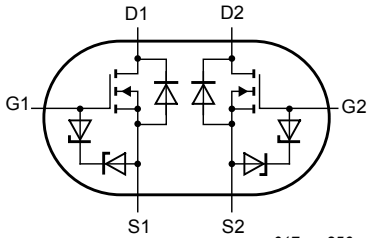
Table 1. Quick reference data

| Symbol                                         | Parameter                        | Conditions                                                      |     | Min | Typ | Max | Unit |
|------------------------------------------------|----------------------------------|-----------------------------------------------------------------|-----|-----|-----|-----|------|
| <b>Per transistor</b>                          |                                  |                                                                 |     |     |     |     |      |
| $V_{DS}$                                       | drain-source voltage             | $T_J = 25\text{ °C}$                                            |     | -   | -   | 30  | V    |
| $V_{GS}$                                       | gate-source voltage              |                                                                 |     | -12 | -   | 12  | V    |
| $I_D$                                          | drain current                    | $V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$                 | [1] | -   | -   | 3.1 | A    |
| <b>Static characteristics (per transistor)</b> |                                  |                                                                 |     |     |     |     |      |
| $R_{DS(on)}$                                   | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}; I_D = 3.1\text{ A}; T_J = 25\text{ °C}$ |     | -   | 55  | 72  | mΩ   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline                                                                                                                             | Graphic symbol                                                                                       |
|-----|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| 1   | S1     | source TR1  |  <p>Transparent top view<br/><b>DFN2020D-6 (SOT1118D)</b></p> |  <p>017aaa256</p> |
| 2   | G1     | gate TR1    |                                                                                                                                                |                                                                                                      |
| 3   | D2     | drain TR2   |                                                                                                                                                |                                                                                                      |
| 4   | S2     | source TR2  |                                                                                                                                                |                                                                                                      |
| 5   | G2     | gate TR2    |                                                                                                                                                |                                                                                                      |
| 6   | D1     | drain TR1   |                                                                                                                                                |                                                                                                      |
| 7   | D1     | drain TR1   |                                                                                                                                                |                                                                                                      |
| 8   | D2     | drain TR2   |                                                                                                                                                |                                                                                                      |

6. Ordering information

Table 3. Ordering information

| Type number | Package    |                                                                                                                           |          |
|-------------|------------|---------------------------------------------------------------------------------------------------------------------------|----------|
|             | Name       | Description                                                                                                               | Version  |
| PMDPB56XNEA | DFN2020D-6 | DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm | SOT1118D |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMDPB56XNEA | 3A           |

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol               | Parameter                                    | Conditions                                                                         |     | Min | Max  | Unit |
|----------------------|----------------------------------------------|------------------------------------------------------------------------------------|-----|-----|------|------|
| Per transistor       |                                              |                                                                                    |     |     |      |      |
| V <sub>DS</sub>      | drain-source voltage                         | T <sub>j</sub> = 25 °C                                                             |     | -   | 30   | V    |
| V <sub>GS</sub>      | gate-source voltage                          |                                                                                    |     | -12 | 12   | V    |
| I <sub>D</sub>       | drain current                                | V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C                                  | [1] | -   | 3.1  | A    |
|                      |                                              | V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C                                 | [1] | -   | 2    | A    |
| I <sub>DM</sub>      | peak drain current                           | T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs                     |     | -   | 12   | A    |
| E <sub>DS(AL)S</sub> | non-repetitive drain-source avalanche energy | I <sub>D</sub> = 0.3 A; T <sub>j(init)</sub> = 25 °C; DUT in avalanche (unclamped) |     | -   | 6.2  | mJ   |
| P <sub>tot</sub>     | total power dissipation                      | T <sub>amb</sub> = 25 °C                                                           | [2] | -   | 485  | mW   |
|                      |                                              |                                                                                    | [1] | -   | 1.15 | W    |
|                      |                                              | T <sub>sp</sub> = 25 °C                                                            |     | -   | 8.33 | W    |
| Per device           |                                              |                                                                                    |     |     |      |      |
| T <sub>j</sub>       | junction temperature                         |                                                                                    |     | -55 | 150  | °C   |
| T <sub>amb</sub>     | ambient temperature                          |                                                                                    |     | -55 | 150  | °C   |
| T <sub>stg</sub>     | storage temperature                          |                                                                                    |     | -65 | 150  | °C   |
| Source-drain diode   |                                              |                                                                                    |     |     |      |      |
| I <sub>S</sub>       | source current                               | T <sub>amb</sub> = 25 °C                                                           | [1] | -   | 1.1  | A    |
| ESD Maximum rating   |                                              |                                                                                    |     |     |      |      |
| V <sub>ESD</sub>     | electrostatic discharge voltage              | HBM                                                                                | [3] | -   | 2000 | V    |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.

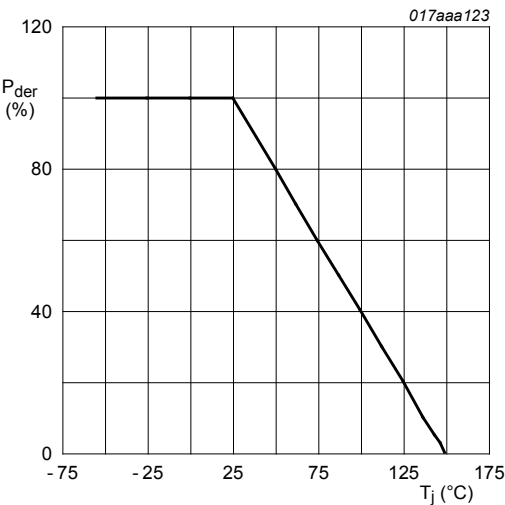


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

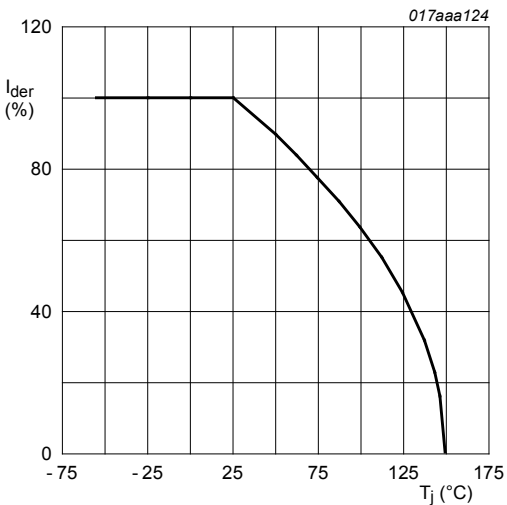


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

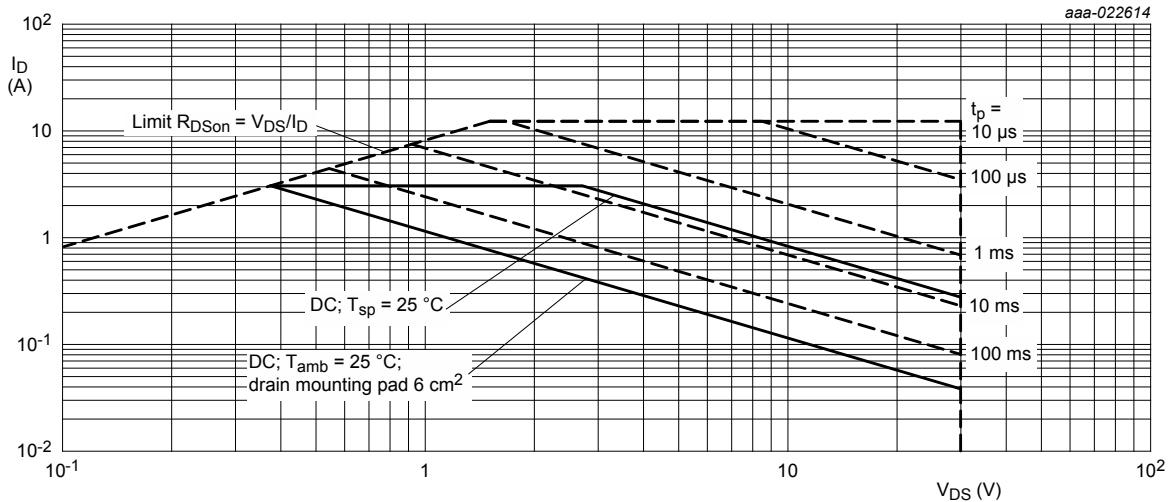


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol                | Parameter                                        | Conditions  |     | Min | Typ | Max | Unit |
|-----------------------|--------------------------------------------------|-------------|-----|-----|-----|-----|------|
| Per transistor        |                                                  |             |     |     |     |     |      |
| R <sub>th(j-a)</sub>  | thermal resistance from junction to ambient      | in free air | [1] | -   | 224 | 257 | K/W  |
|                       |                                                  |             | [2] | -   | 96  | 109 | K/W  |
| R <sub>th(j-sp)</sub> | thermal resistance from junction to solder point |             |     | -   | 12  | 15  | K/W  |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

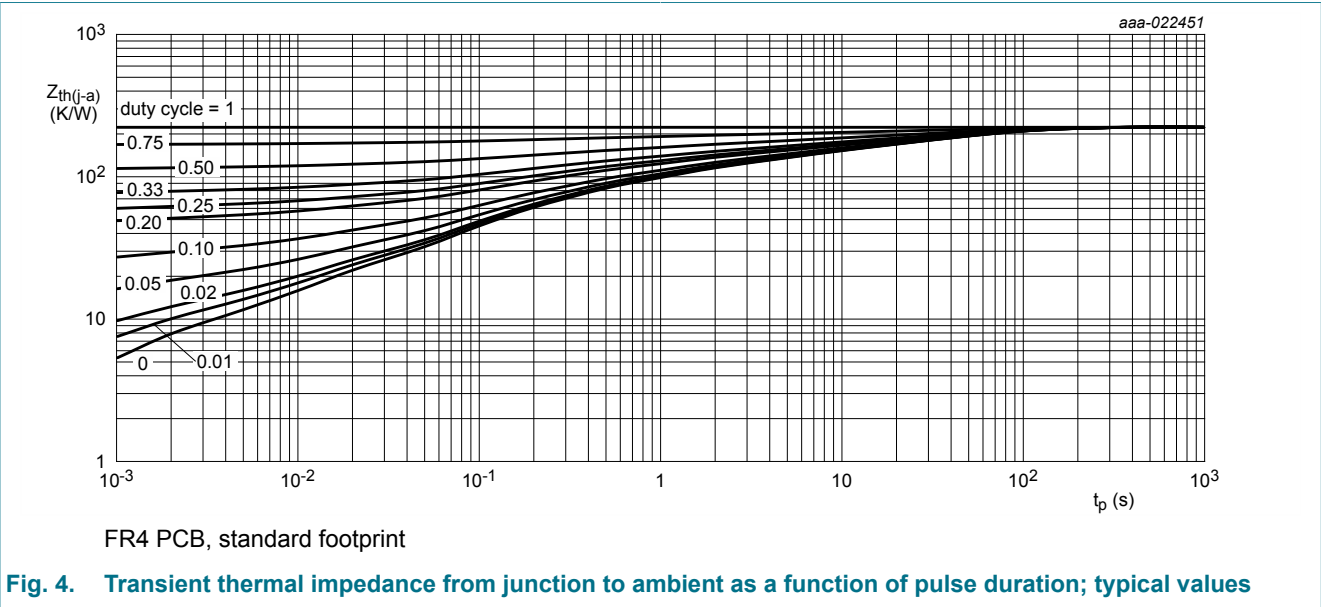
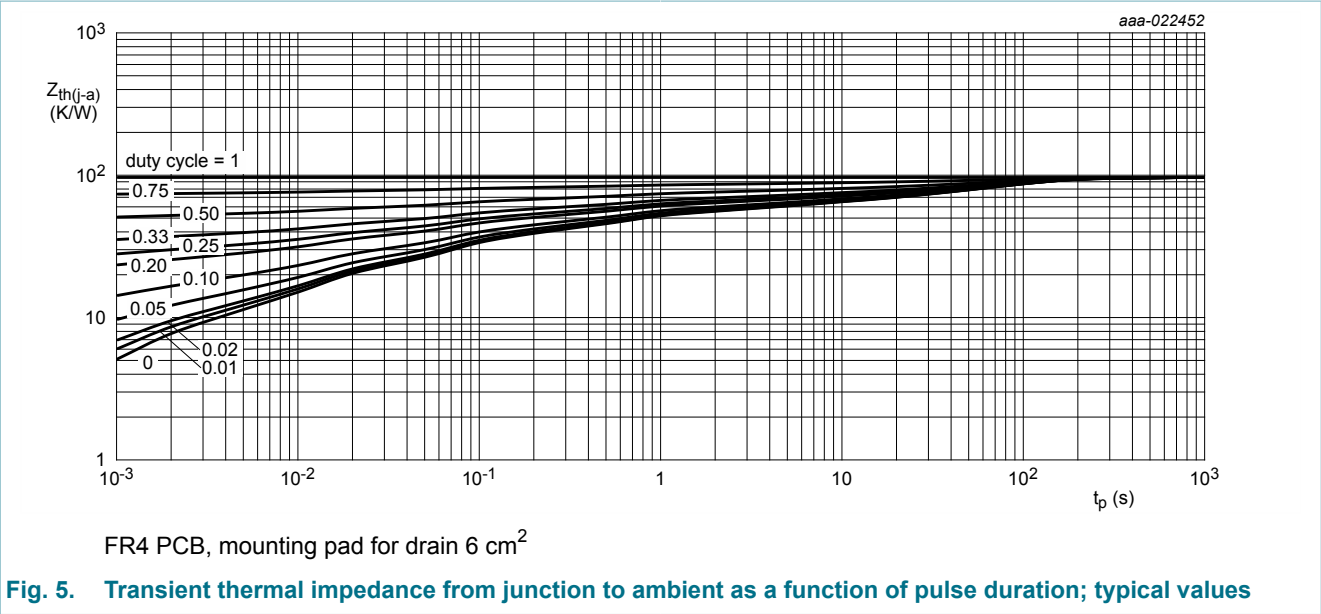


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



## 10. Characteristics

Table 7. Characteristics

| Symbol                                   | Parameter                        | Conditions                                                                                                               |  | Min  | Typ | Max  | Unit |
|------------------------------------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------|--|------|-----|------|------|
| Static characteristics (per transistor)  |                                  |                                                                                                                          |  |      |     |      |      |
| V <sub>(BR)DSS</sub>                     | drain-source breakdown voltage   | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                   |  | 30   | -   | -    | V    |
| V <sub>GSth</sub>                        | gate-source threshold voltage    | I <sub>D</sub> = 250 μA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C                                       |  | 0.75 | 1   | 1.25 | V    |
| I <sub>DSS</sub>                         | drain leakage current            | V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                    |  | -    | -   | 1    | μA   |
| I <sub>GSS</sub>                         | gate leakage current             | V <sub>GS</sub> = 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                    |  | -    | -   | 10   | μA   |
|                                          |                                  | V <sub>GS</sub> = -12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                   |  | -    | -   | -10  | μA   |
|                                          |                                  | V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                   |  | -    | -   | 2    | μA   |
|                                          |                                  | V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                  |  | -    | -   | -2   | μA   |
| R <sub>DSon</sub>                        | drain-source on-state resistance | V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3.1 A; T <sub>j</sub> = 25 °C                                                  |  | -    | 55  | 72   | mΩ   |
|                                          |                                  | V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3.1 A; T <sub>j</sub> = 150 °C                                                 |  | -    | 92  | 121  | mΩ   |
|                                          |                                  | V <sub>GS</sub> = 2.5 V; I <sub>D</sub> = 2.6 A; T <sub>j</sub> = 25 °C                                                  |  | -    | 72  | 102  | mΩ   |
| g <sub>fs</sub>                          | forward transconductance         | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 3.1 A; T <sub>j</sub> = 25 °C                                                   |  | -    | 12  | -    | S    |
| R <sub>G</sub>                           | gate resistance                  | f = 1 MHz; T <sub>j</sub> = 25 °C                                                                                        |  | -    | 9.2 | -    | Ω    |
| Dynamic characteristics (per transistor) |                                  |                                                                                                                          |  |      |     |      |      |
| Q <sub>G(tot)</sub>                      | total gate charge                | V <sub>DS</sub> = 15 V; I <sub>D</sub> = 3.1 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C                          |  | -    | 2.9 | 5    | nC   |
| Q <sub>GS</sub>                          | gate-source charge               |                                                                                                                          |  | -    | 0.4 | -    | nC   |
| Q <sub>GD</sub>                          | gate-drain charge                |                                                                                                                          |  | -    | 0.8 | -    | nC   |
| C <sub>iss</sub>                         | input capacitance                | V <sub>DS</sub> = 15 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                         |  | -    | 256 | -    | pF   |
| C <sub>oss</sub>                         | output capacitance               |                                                                                                                          |  | -    | 31  | -    | pF   |
| C <sub>rss</sub>                         | reverse transfer capacitance     |                                                                                                                          |  | -    | 23  | -    | pF   |
| t <sub>d(on)</sub>                       | turn-on delay time               | V <sub>DS</sub> = 15 V; I <sub>D</sub> = 8 A; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C |  | -    | 9   | -    | ns   |
| t <sub>r</sub>                           | rise time                        |                                                                                                                          |  | -    | 20  | -    | ns   |
| t <sub>d(off)</sub>                      | turn-off delay time              |                                                                                                                          |  | -    | 19  | -    | ns   |
| t <sub>f</sub>                           | fall time                        |                                                                                                                          |  | -    | 7   | -    | ns   |
| Source-drain diode (per transistor)      |                                  |                                                                                                                          |  |      |     |      |      |
| V <sub>SD</sub>                          | source-drain voltage             | I <sub>S</sub> = 1.1 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                    |  | -    | 0.7 | 1.2  | V    |

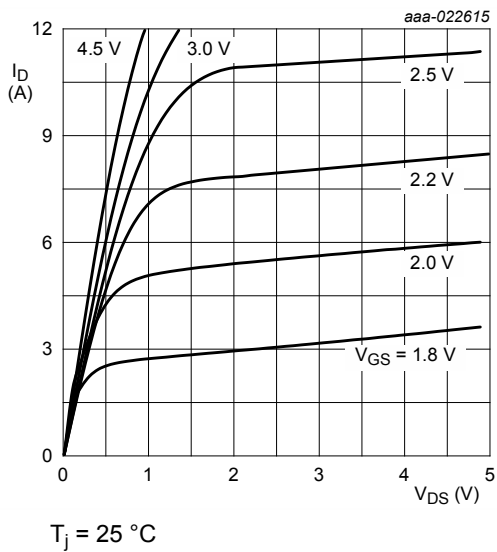


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

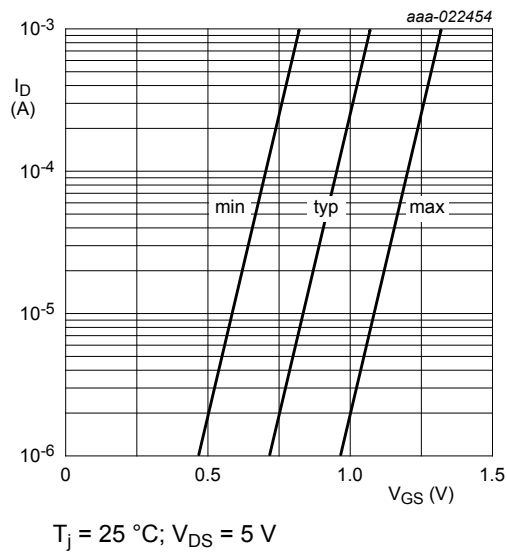


Fig. 7. Subthreshold drain current as a function of gate-source voltage

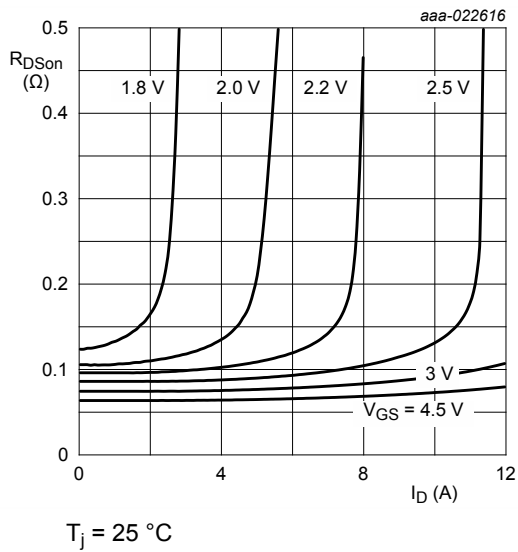


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

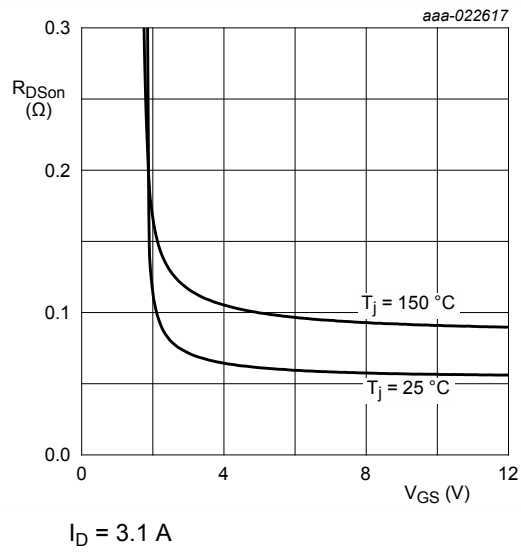


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



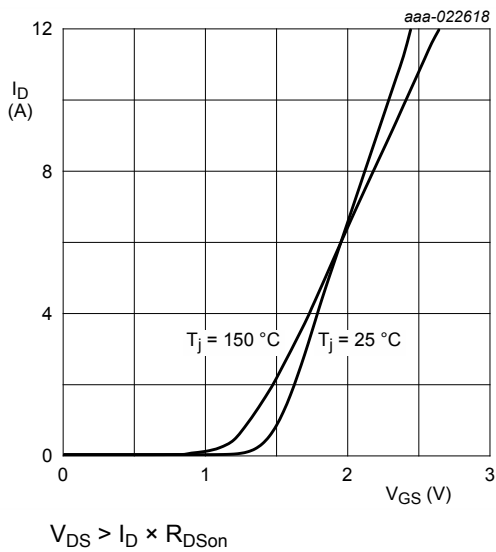


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

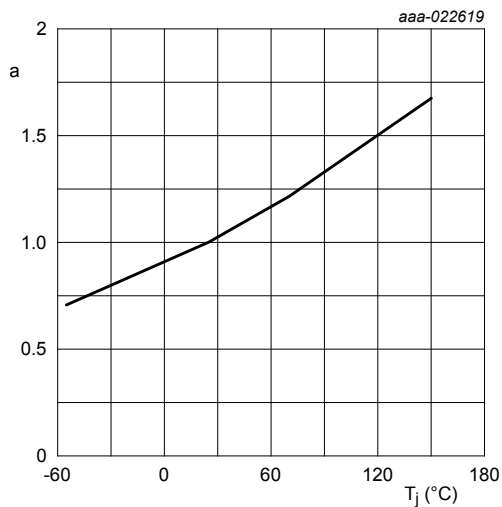


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

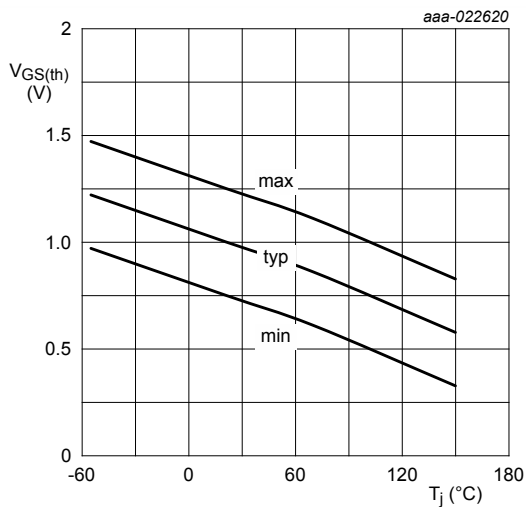


Fig. 12. Gate-source threshold voltage as a function of junction temperature

$$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$$

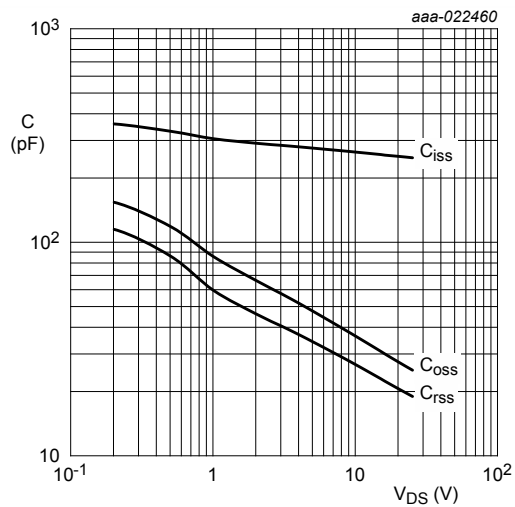


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$$

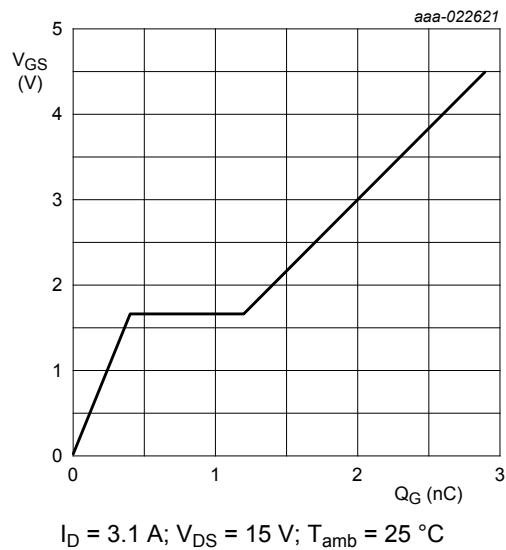


Fig. 14. Gate-source voltage as a function of gate charge; typical values

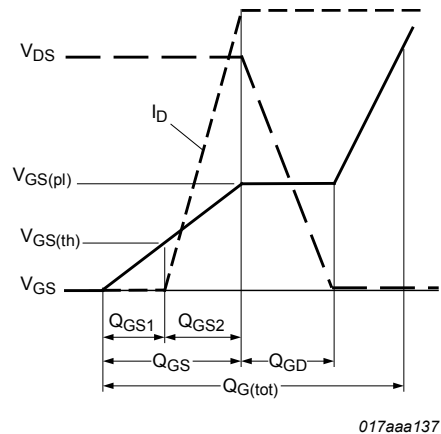
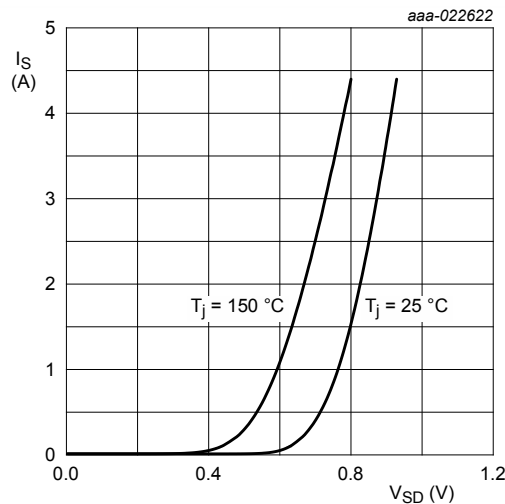


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

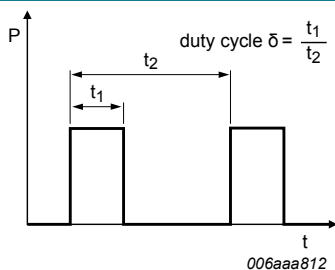


Fig. 17. Duty cycle definition

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

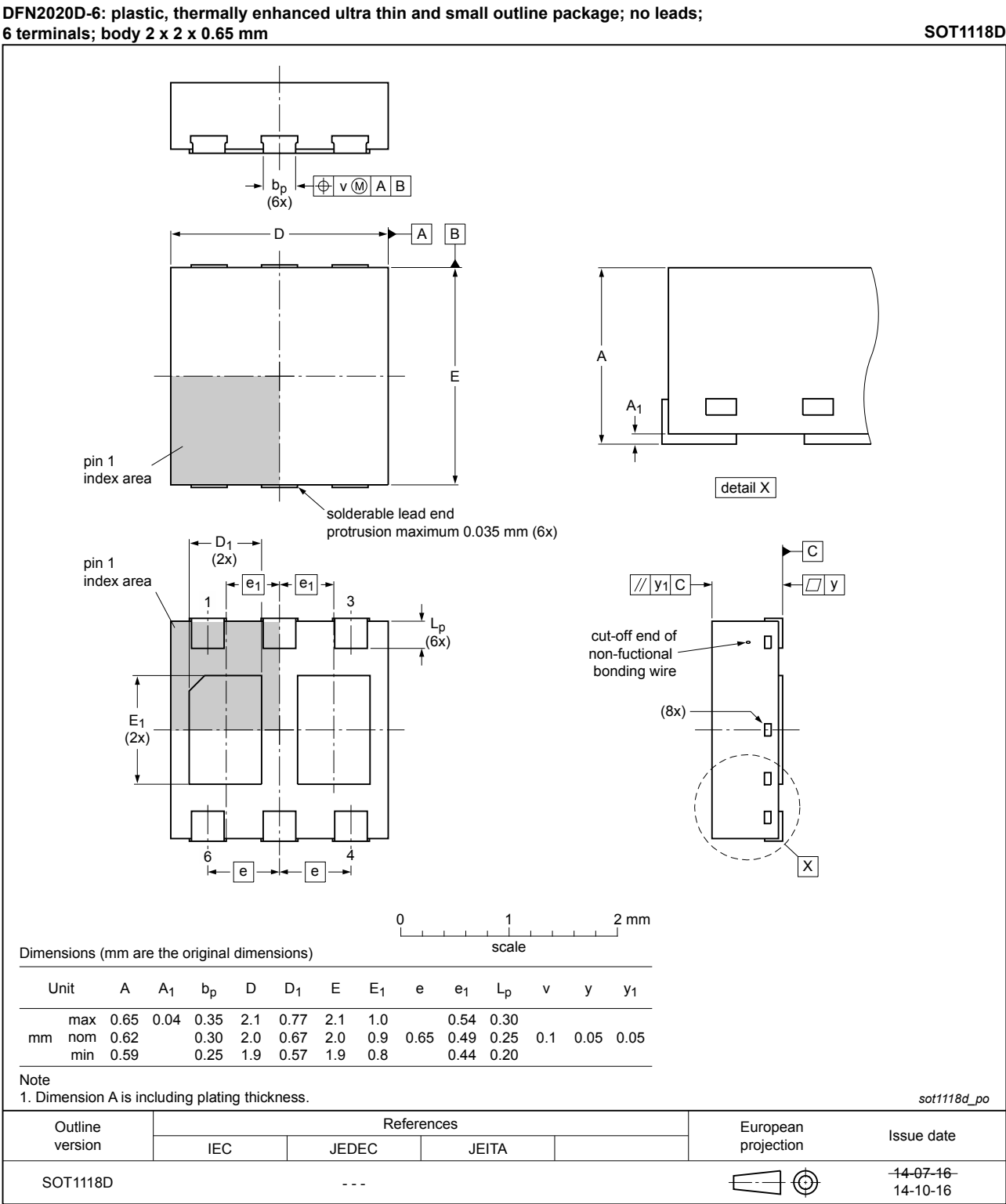
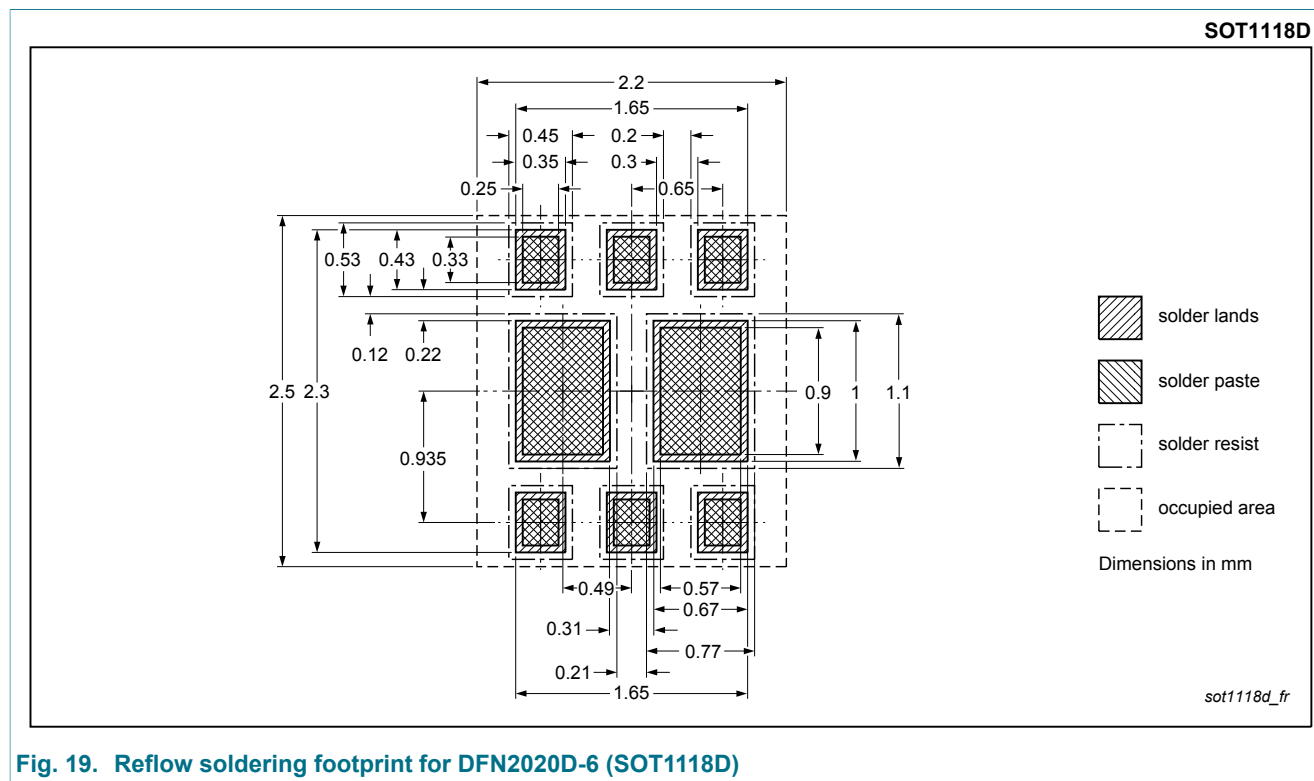


Fig. 18. Package outline DFN2020D-6 (SOT1118D)

## 13. Soldering



14. Revision history

Table 8. Revision history

| Data sheet ID   | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PMDPB56XNEA v.1 | 20160419     | Product data sheet | -             | -          |

## 15. Legal information

### 15.1 Data sheet status

| Document status [1][2]         | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
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