DATASHEET

Description

The 9FGL0641/51/P1 are members of IDT's 3.3V Low-Power (LP) PCIe family. The devices have 6 output enables for clock management and support 2 different spread spectrum levels in addition to spread off. The 9FGL0641/51/P1 supports both Common Clock (CC) with or without spread spectrum and Separate Reference no-Spread (SRnS) PCIe clocking architectures. The 9FGL06P1 can be programmed with a user-defined power up default SMBus configuration.

Recommended Application

3.3V PCIe Gen1-2-3 Clock Generator

Output Features

- 6 – 100 MHz Low-Power HCSL (LP-HCSL) DIF pairs
  - 9FGL0641 default ZOUT = 100Ω
  - 9FGL0651 default ZOUT = 85Ω
  - 9FGL06P1 factory programmable defaults
- 1 - 3.3V LVCMOS REF output w/Wake-On-LAN (WOL) support

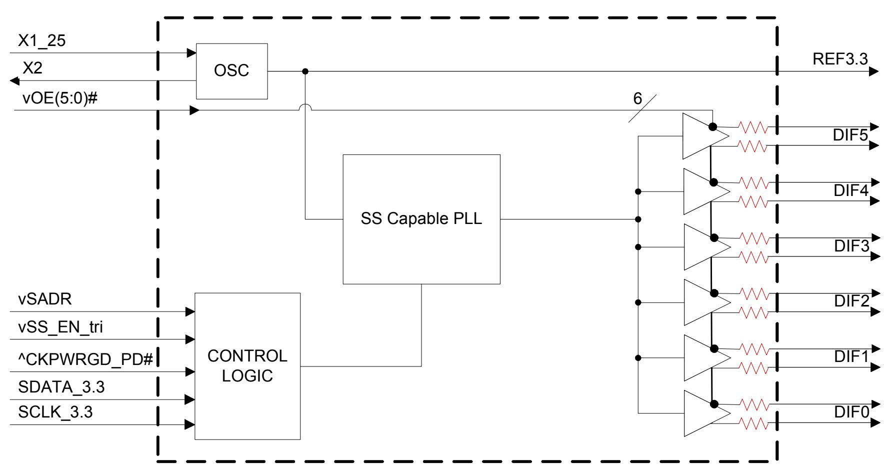
Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew <50ps
- DIF phase jitter is PCIe Gen1-2-3 compliant with SSC on or off
- DIF 12k-20M phase jitter is <2ps rms when SSC is off
- REF phase jitter is <300fs rms, SSC off, and <1.5ps rms, SSC is On
- ±100ppm frequency accuracy on all clocks

Features/Benefits

- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines; saves 24 resistors compared to standard PCIe devices
- 120mW typical power consumption; eliminates thermal concerns
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - differential output amplitude
  - 33, 85 or 100Ω output impedance for each output
  - spread spectrum amount
- 41 and 51 devices contain default configuration; SMBus interface not required for device operation
- P1 device allows factory programming of customer-defined SMBus power up default; allows exact optimization to customer requirements
- Outputs can optionally be supplied from any voltage between 1.05 and 3.3V; maximum power savings
- OE# pins; support DIF power management
- 8MHz - 40MHz input frequency (25MHz default); flexibility
- Pin/SMBus selectable 0%, -0.25% or -0.5% spread on DIF outputs %; minimize EMI and phase jitter for each application
- DIF outputs blocked until PLL is locked; clean system start-up
- Two selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 40-pin 5x5mm VFQFPN; minimal board space

Block Diagram



Note: Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

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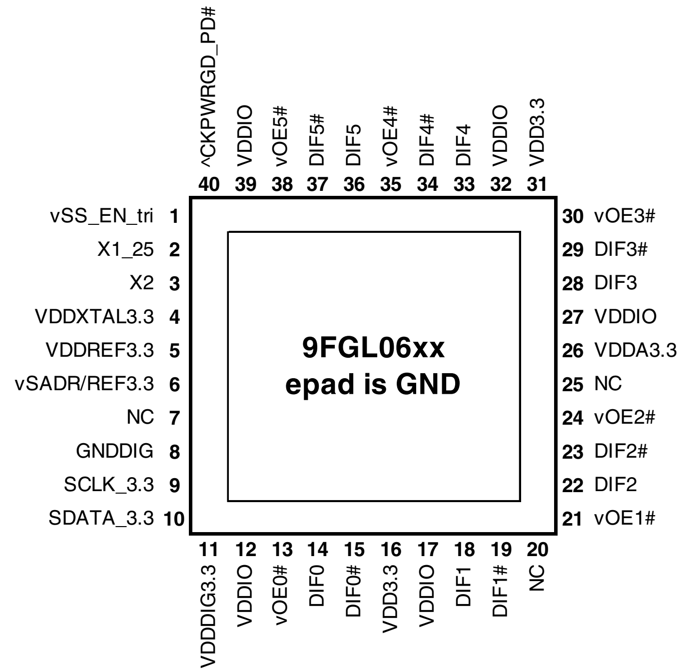
Pin Configuration



40-pin VFQFPN, 5x5 mm, 0.4mm pitch

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	x
	1	1101010	x

Power Management Table[3]

CKPWRGD_PD#	SMBus OE bit	OEx# Pin	DIFx		REF
			True O/P	Comp. O/P	
0	X	X	Low[1]	Low[1]	Hi-Z[2]
1	1	0	Running	Running	Running
1	1	1	Disabled[1]	Disabled[1]	Running
1	0	X	Disabled[1]	Disabled[1]	Disabled[4]

1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5]=1, in which case REF is running.
3. Input polarities defined at default values for 9FGL0641/0651.
4. See SMBus description for Byte 3, bit 4

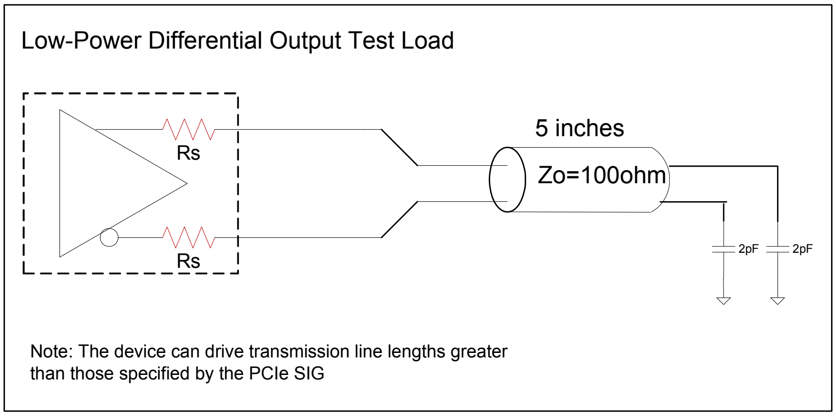
Power Connections

Pin Number			Description
VDD	VDDIO	GND	
4		41	XTAL OSC
5		41	REF Power
11		8	Digital (dirty) Power
	12,17,27,32,39	41	DIF outputs
26		41	PLL Analog

Pin Descriptions (9FGL0641/51 Configuration)

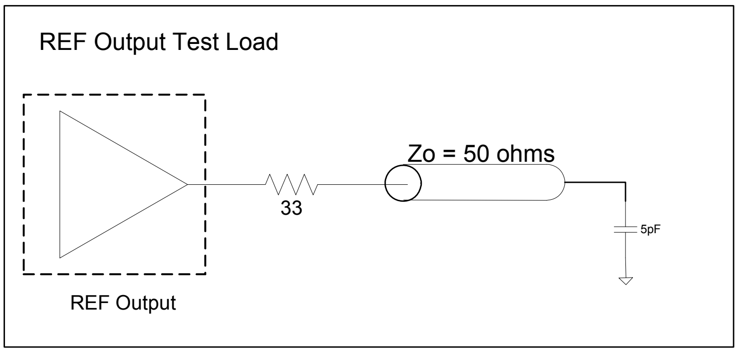
PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	vSS_EN_tri	LATCHED IN	Latched select input to select spread spectrum amount at initial power up : 1 = -0.5% spread, M = -0.25%, 0 = Spread Off
2	X1_25	IN	Crystal input, Nominally 25.00MHz.
3	X2	OUT	Crystal output.
4	VDDXTAL3.3	PWR	Power supply for XTAL, nominal 3.3V
5	VDDREF3.3	PWR	VDD for REF output. nominal 3.3V.
6	vSADR/REF3.3	LATCHED I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin
7	NC	N/A	No Connection.
8	GNDDIG	GND	Ground pin for digital circuitry
9	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
10	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
11	VDDDIG3.3	PWR	3.3V digital power (dirty power)
12	VDDIO	PWR	Power supply for differential outputs
13	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
14	DIF0	OUT	Differential true clock output
15	DIF0#	OUT	Differential Complementary clock output
16	VDD3.3	PWR	Power supply, nominal 3.3V
17	VDDIO	PWR	Power supply for differential outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	NC	N/A	No Connection.
21	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
22	DIF2	OUT	Differential true clock output
23	DIF2#	OUT	Differential Complementary clock output
24	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	NC	N/A	No Connection.
26	VDDA3.3	PWR	3.3V power for the PLL core.
27	VDDIO	PWR	Power supply for differential outputs
28	DIF3	OUT	Differential true clock output
29	DIF3#	OUT	Differential Complementary clock output
30	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
31	VDD3.3	PWR	Power supply, nominal 3.3V
32	VDDIO	PWR	Power supply for differential outputs
33	DIF4	OUT	Differential true clock output
34	DIF4#	OUT	Differential Complementary clock output
35	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
36	DIF5	OUT	Differential true clock output
37	DIF5#	OUT	Differential Complementary clock output
38	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
39	VDDIO	PWR	Power supply for differential outputs
40	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
41	ePAD	GND	Connect paddle to ground.

Test Loads



Terminations

Device	Zo (Ω)	Rs (Ω)
9FGL0641	100	None needed
9FGL0651	100	7.5
9FGL06P1	100	Prog.
9FGL0641	85	N/A
9FGL0651	85	None needed
9FGL06P1	85	Prog.



Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGL06. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Supply Voltage	VDDxx	Applies to VDD, VDDA and VDDIO, if present.	-0.5		3.9	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD} + 0.5V	V	1, 3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.5V.

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency	400			kHz	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2.] The device must be powered up for the SMBus to function.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDxxx	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V	
IO Supply Voltage	VDDIO	Supply voltage for differential Low Power outputs.	0.9975	1.05-3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	$0.75xV_{DD}$		$V_{DD}+0.3$	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	$0.4xV_{DD}$	$0.5xV_{DD}$	$0.6xV_{DD}$	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		$0.25xV_{DD}$	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_{in}	XTAL, or X1 input	8	25	40	MHz	4
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.3	1.8	ms	1,2
SS Modulation Frequency	f_{MOD}	(Triangular Modulation)	30	31.6	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	1,2
Trise	t_R	Rise time of single-ended control inputs			5	ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

[4] The 9FGLxxP1 devices can be programmed for various input frequencies from 8 to 40MHz. The 9FGLxx41/51 devices use 25MHz.

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

<table>
<tr><th>PARAMETER</th><th>SYMBOL</th><th>CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th><th>NOTES</th></tr>
<tr><td rowspan="2">Slew rate</td><td rowspan="2">Trf</td><td>Scope averaging on, fast setting</td><td>2.2</td><td>3.2</td><td>4.5</td><td>V/ns</td><td>2,3</td></tr>
<tr><td>Scope averaging, slow setting</td><td>1.4</td><td>2.1</td><td>3.2</td><td>V/ns</td><td>2,3</td></tr>
<tr><td>Crossing Voltage (abs)</td><td>Vcross_abs</td><td>Scope averaging off</td><td>250</td><td>411</td><td>550</td><td>mV</td><td>1,4,5</td></tr>
<tr><td>Crossing Voltage (var)</td><td>Δ-Vcross</td><td>Scope averaging off</td><td></td><td>11</td><td>140</td><td>mV</td><td>1,4,9</td></tr>
<tr><td>Avg. Clock Period Accuracy</td><td>T_{PERIOD_AVG}</td><td></td><td>-100</td><td>0.0</td><td>+2600</td><td>ppm</td><td>2,10,13</td></tr>
<tr><td>Absolute Period</td><td>T_{PERIOD_ABS}</td><td>Includes jitter and Spread Spectrum Modulation</td><td>9.94906</td><td>10.0</td><td>10.1011</td><td>ns</td><td>2,6</td></tr>
<tr><td>Jitter, Cycle to cycle</td><td>$t_{jcyc-cyc}$</td><td></td><td></td><td>34</td><td>50</td><td>ps</td><td>2</td></tr>
<tr><td>Voltage High</td><td>V_{HIGH}</td><td rowspan="2">Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)</td><td>660</td><td>771</td><td>850</td><td rowspan="2">mV</td><td>1</td></tr>
<tr><td>Voltage Low</td><td>V_{LOW}</td><td>-150</td><td>18</td><td>150</td><td>1</td></tr>
<tr><td>Absolute Max Voltage</td><td>Vmax</td><td rowspan="2">Measurement on single ended signal using absolute value. (Scope averaging off)</td><td></td><td>821</td><td>1150</td><td rowspan="2">mV</td><td>1,7,15</td></tr>
<tr><td>Absolute Min Voltage</td><td>Vmin</td><td>-300</td><td>-30</td><td></td><td>1,8,15</td></tr>
<tr><td>Duty Cycle</td><td>t_{DC}</td><td></td><td>45</td><td>49</td><td>55</td><td>%</td><td>2</td></tr>
<tr><td>Slew rate matching</td><td>ΔTrf</td><td></td><td></td><td>7</td><td>20</td><td>%</td><td>1,14</td></tr>
<tr><td>Skew, Output to Output</td><td>t_{sk3}</td><td>Averaging on, V_T = 50%</td><td></td><td>23</td><td>50</td><td>ps</td><td>2</td></tr>
</table>

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 4.3.7.1.1 of the PCI Express Base Specification, Revision 3.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.

[12] T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range.

[13] PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then we have an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,800 PPM.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default SMBus amplitude settings.

Electrical Characteristics–DIF LP-HCSL Output Phase Jitter Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	IND. LIMIT	UNITS	Notes
Phase Jitter, PCI Express (Common Clock Architecture)[1]	$t_{jphPCIeG1}$	PCIe Gen 1		19	23	86	ps (p-p)	1,3,4,6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.5	0.7	3	ps (rms)	1,3,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.2	1.8	3.1	ps (rms)	1,3,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.3	0.5	1	ps (rms)	1,3,6
Phase Jitter, 12k-20M	$t_{jph12k20M}$	100MHz, REF output enabled		1.5	2	N/A	ps (rms)	2,6

[1] Defined for Spread Spectrum On or Off
[2] Only defined for Spread Spectrum Off.
[3] See http://www.pcisig.com for complete specs
[4] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.
[5] Calculated from Intel-supplied Clock Jitter Tool
[6] Applies to all differential outputs

Electrical Characteristics–Current Consumption

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDAOP}	VDDA, All outputs active @100MHz		13	16	mA	
	I_{DDOP}	All VDD, except VDDA and VDDIO, All outputs active @100MHz		16	21	mA	
	I_{DDIOOP}	VDDIO, All outputs active @100MHz		23	29	mA	
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	VDDA, DIF outputs off, REF output running		0.8	1	mA	1
	I_{DDPD}	All VDD, except VDDA and VDDIO, DIF outputs off, REF output running		7.5	9	mA	1
	I_{DDIOPD}	VDDIO, DIF outputs off, REF output running		0.06	0.1	mA	1
Powerdown Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	VDDA, all outputs off		0.8	1.1	mA	
	I_{DDPD}	All VDD, except VDDA and VDDIO, all outputs off		2.4	3	mA	
	I_{DDIOPD}	VDDIO, all outputs off		0.05	0.1	mA	

[1] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1)

Electrical Characteristics– REF

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values		0		ppm	1,2
Clock period	T_{period}	REF output		40		ns	2
High output Voltage	V_{HIGH}	Ioh = -2mA	0.8xV_{DDREF}			V	
Low output Voltage	V_{LOW}	Iol = 2mA			0.2xV_{DDREF}	V	
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 1F, V_{OH} = 0.8*VDD, V_{OL} = 0.2*VDD	0.5	0.8	1.2	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 5F, VOH = 0.8*VDD, VOL = 0.2*VDD	1.0	1.4	2.0	V/ns	1,3
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 9F, VOH = 0.8*VDD, VOL = 0.2*VDD	1.5	2.0	2.6	V/ns	1
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = DF, VOH = 0.8*VDD, VOL = 0.2*VDD	2.0	2.6	3.2	V/ns	1
Duty Cycle	d_{t1X}	V_T = VDD/2 V	45	49.8	55	%	1,4
Duty Cycle Distortion	d_{tcd}	V_T = VDD/2 V	-1	-0.5	0	%	1,5
Jitter, cycle to cycle	$t_{jcyc-cyc}$	V_T = VDD/2 V		70	150	ps	1,4
Noise floor	t_{jdBc1k}	1kHz offset		-145	-135	dBc	1,4
Noise floor	$t_{jdBc10k}$	10kHz offset to Nyquist		-150	-140	dBc	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, DIF SSC Off		0.13	0.3	ps (rms)	1,4
Jitter, phase	t_{jphREF}	12kHz to 5MHz, DIF SSC On		1.4	1.5	ps (rms)	1,4

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00 MHz

[3] Default SMBus Value

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus Address is Latched on SADR pin. Unless otherwise indicated, default values are for the xx41 and xx51. P1 devices are fully factory programmable.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE5	Output Enable	RW	See B11[1:0]	Enabled	1
Bit 6	DIF OE4	Output Enable	RW		Enabled	1
Bit 5	Reserved					X
Bit 4	DIF OE3	Output Enable	RW	See B11[1:0]	Enabled	1
Bit 3	DIF OE2	Output Enable	RW		Enabled	1
Bit 2	DIF OE1	Output Enable	RW		Enabled	1
Bit 1	Reserved					X
Bit 0	DIF OE0	Output Enable	RW	See B11[1:0]	Enabled	1

1. A low on these bits will overide the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: SS Readback and Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SSENRB1	SS Enable Readback Bit1	R	00' for SS_EN_tri = 0, '01' for SS_EN_tri = 'M', '11 for SS_EN_tri = '1'		Latch
Bit 6	SSENRB1	SS Enable Readback Bit0	R			Latch
Bit 5	SSEN_SWCNTRL	Enable SW control of SS	RW	SS control locked	Values in B1[4:3] control SS amount.	0
Bit 4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	00' = SS Off, '01' = -0.25% SS, '10' = Reserved, '11'= -0.5% SS		0
Bit 3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]			0
Bit 2	Reserved					X
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.55V	01= 0.65V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.7V	11 = 0.8V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE5	Output Enable	RW	See B11[1:0]	Enabled	1
Bit 6	DIF OE4	Output Enable	RW		Enabled	1
Bit 5	Reserved					X
Bit 4	DIF OE3	Output Enable	RW	See B11[1:0]	Enabled	1
Bit 3	DIF OE2	Output Enable	RW		Enabled	1
Bit 2	DIF OE1	Output Enable	RW		Enabled	1
Bit 1	Reserved					X
Bit 0	DIF OE0	Output Enable	RW	See B11[1:0]	Enabled	1

Note: See "Low-Power HCSL Outputs" table for slew rates.

SMBus Table: Nominal Vhigh Amplitude Control/ REF Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF	Slew Rate Control	RW	00 = Slowest	01 =Slow	0
Bit 6			RW	10 = Fast	11 = Fastest	1
Bit 5	REF Power Down Function	Wake-on-Lan Enable for REF	RW	REF disabled in Power Down	REF runs in Power Down	0
Bit 4	REF OE	REF Output Enable	RW	Disabled[1]	Enabled	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=HIgh

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx, 10 = DMx, 11= DBx w/oPLL		0
Bit 6	Device Type0		R			0
Bit 5	Device ID5	Device ID	R	001000 binary or 06 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			1
Bit 2	Device ID2		R			0
Bit 1	Device ID1		R			0
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved.

SMBus Table: PLL MN Enable, PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	PLL M/N En	M/N Programming Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

SMBus Table: Stop State Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF2_imp[1]	DIF2 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF2_imp[0]	DIF2 Zout	RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	DIF1_imp[1]	DIF1 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 4	DIF1_imp[0]	DIF1 Zout	RW	01=85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	DIF0_imp[1]	DIF0 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 0	DIF0_imp[0]	DIF0 Zout	RW	01=85Ω DIF Zout	11 = Reserved	

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	DIF5_imp[1]	DIF5 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF5_imp[0]	DIF5 Zout	RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	DIF4_imp[1]	DIF4 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 4	DIF4_imp[0]	DIF6 Zout	RW	01=85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	DIF3_imp[1]	DIF3 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 0	DIF3_imp[0]	DIF3 Zout	RW	01=85Ω DIF Zout	11 = Reserved	

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE2_pu/pd[1]	OE2 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 6	OE2_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE1_pu/pd[1]	OE1 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 4	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	OE0_pu/pd[1]	OE0 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 0	OE0_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	OE5_pu/pd[1]	OE5 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 6	OE5_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE4_pu/pd[1]	OE4 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 4	OE4_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	OE3_pu/pd[1]	OE3 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 0	OE3_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	0

Bytes 17 is Reserved

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	OE5_polarity	Sets OE5 polarity	RW	Enabled when Low	Enabled when High	0
Bit 6	OE4_polarity	Sets OE4 polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	Reserved					X
Bit 4	OE3_polarity	Sets OE3 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE2_polarity	Sets OE2 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	Reserved					X
Bit 0	OE0_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0

SMBus Table: Polarity Control

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

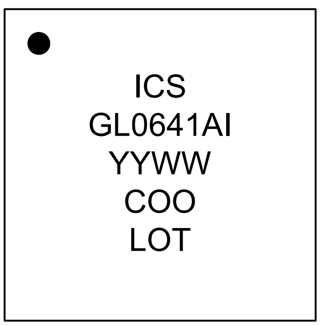
Recommended Crystal Characteristics (3225 package)

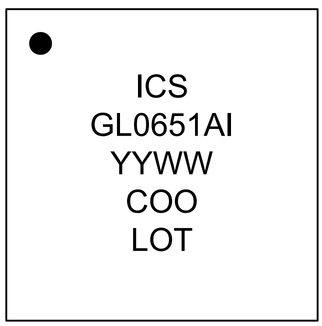
PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commerical)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	1
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

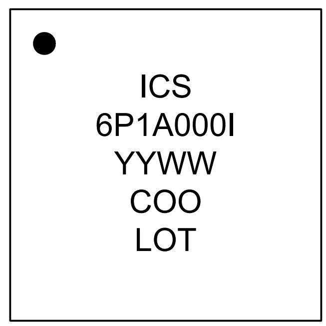
Notes:

1. IDT 603-25-150JA4C or 603-25-150JA4I

Marking Diagrams







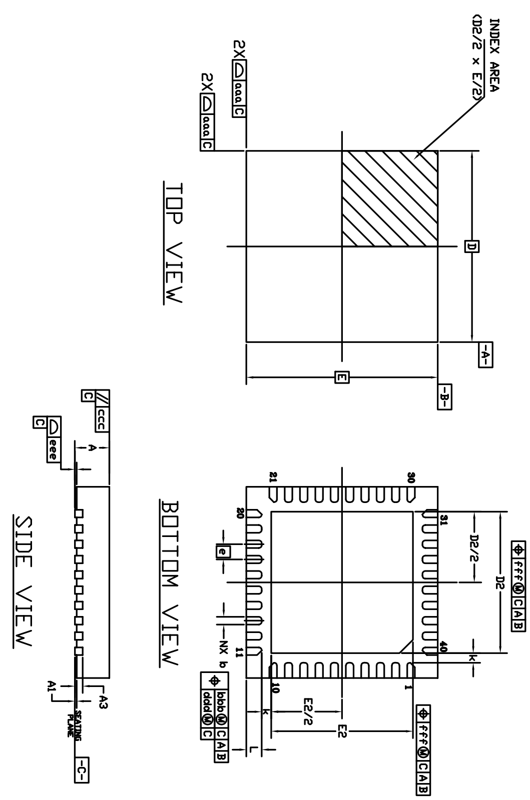
Notes:
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.
7. “P” denotes factory programmable defaults

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP.	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NDG40	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1]ePad soldered to board

Package Outline and Package Dimensions (NDG40) – use EPAD Option P1



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

COMMON DIMENSION

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D2		SEE EPAD OPTION	
E2		SEE EPAD OPTION	
L	0.30	0.40	0.50
e		0.40 BSC	
N		40	
ND		10 (note 3)	
NE		10 (note 3)	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k		0.25	
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

EPAD OPTION:

SYMBOL	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
D2	3.55	3.65	3.80	3.40	3.50	3.60
E2	3.55	3.65	3.80	3.40	3.50	3.60

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE		RC
01	Add tolerance and details	05/31/10	RC
02	ADD EPAD OPTION	11/29/12	RC
03	COMBINE POD & LAND PATTERN	1/24/14	J.H
04	ADJUST LINE WIDTH on PDF	5/16/14	J.H

TOLERANCES UNLESS SPECIFIED
DECIMAL X±.1 XX±.05 XXX± .030
ANGULAR ±1°

APPROVALS	DATE
DRAWN ma	05/31/10
CHECKED	

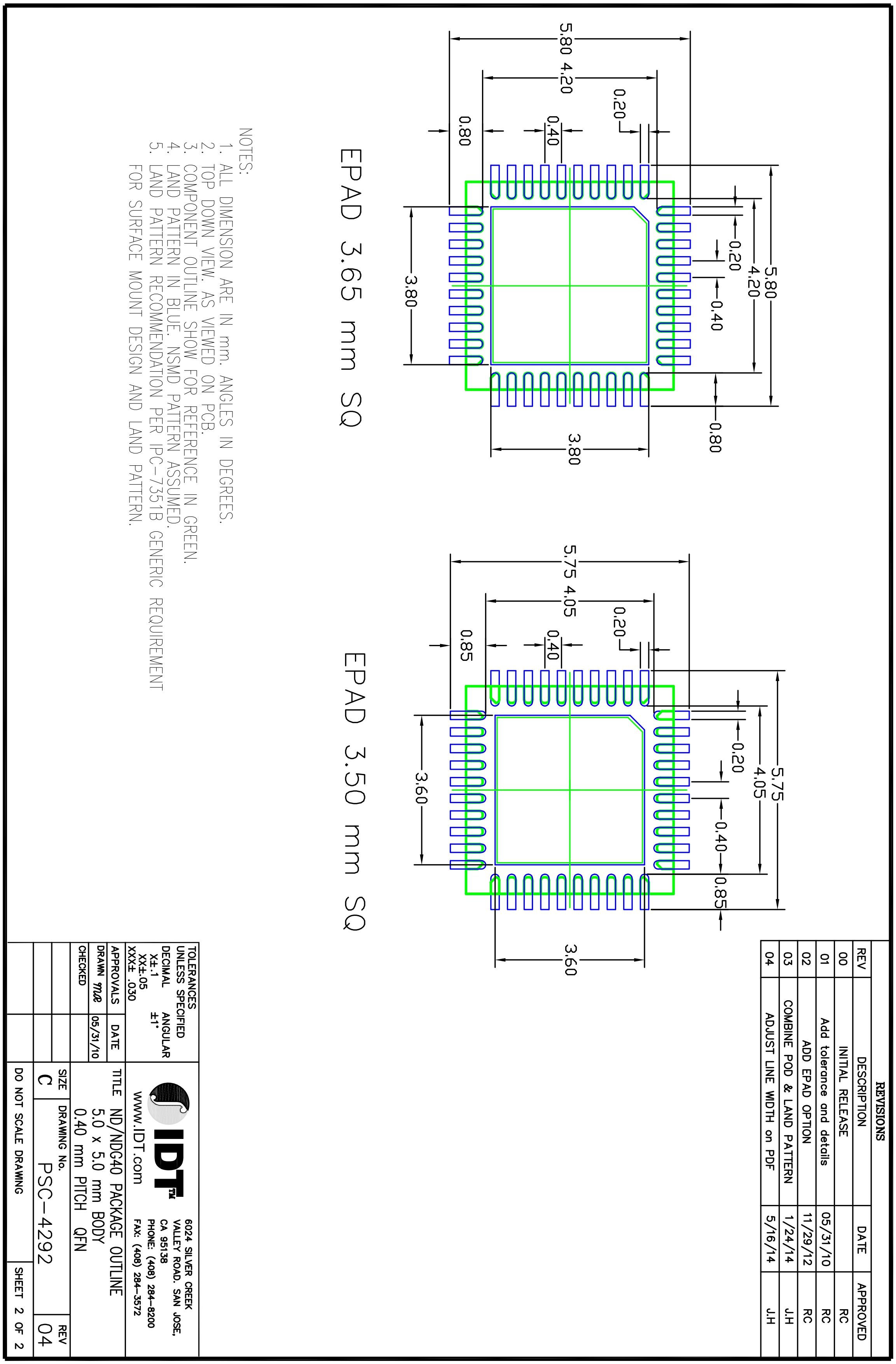
IDT™ www.IDT.com
6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE ND/NDG40 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.40 mm PITCH QFN

SIZE C | DRAWING No. PSC-4292 | REV 04

DO NOT SCALE DRAWING | SHEET 1 OF 2

Package Outline and Package Dimensions (NDG40) – use EPAD 3.65 mm SQ



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FGL0641AKILF	Trays	40-pin VFQFPN	-40 to +85° C
9FGL0641AKILFT	Tape and Reel	40-pin VFQFPN	-40 to +85° C
9FGL0651AKILF	Trays	40-pin VFQFPN	-40 to +85° C
9FGL0651AKILFT	Tape and Reel	40-pin VFQFPN	-40 to +85° C
9FGL06P1A000KILF	Trays	40-pin VFQFPN	-40 to +85° C
9FGL06P1A000KILFT	Tape and Reel	40-pin VFQFPN	-40 to +85° C
9FGL06P1AxxxKILF	Trays	40-pin VFQFPN	-40 to +85° C
9FGL06P1AxxxKILFT	Tape and Reel	40-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).
"000" is a blank device.
"xxx" is a unique factory assigned number to identify a particular default configuration.

Revision History

Rev.	Issue Date	Intiator	Description	Page #
A	6/9/2015	RDW	1. Updated electrical tables to final 2. Updated Power management table and SMBus to final 3. Updated Pin Description title 4. Updated RS values in test loads 5. Added note for Byte 3, bit 4, changed definition of '0' condition. 6. Updated ordering information for '000' part. 7. Added Voh and Vol paramters to REF electrical table, inadvertantly left out.	2-4, 6-9, 11, 18
B	7/17/2015	RDW	1. Added Voh and Ioh to REF table. 2. Minor formatting updates for readability and consistency. 3. Added I-temp crystal part number to crystal characteristics table 4. Added reference to AN-891 for terminating to other logic families. 5. Removed LVDS termination drawing (now in AN-891)	Various

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