3.3 VOLT CMOS SyncFIFO™
256 x 9, 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9 and 8,192 x 9

IDT72V201, IDT72V211
IDT72V221, IDT72V231
IDT72V241, IDT72V251

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:

- **256 x 9-bit organization IDT72V201**
- **512 x 9-bit organization IDT72V211**
- **1,024 x 9-bit organization IDT72V221**
- **2,048 x 9-bit organization IDT72V231**
- **4,096 x 9-bit organization IDT72V241**
- **8,192 x 9-bit organization IDT72V251**
- **10 ns read/write cycle time**
- **5V input tolerant**
- **Read and Write clocks can be independent**
- **Dual-Ported zero fall-through time architecture**
- **Empty and Full Flags signal FIFO status**
- **Programmable Almost-Empty and Almost-Full flags can be set to any depth**
- **Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively**
- **Output Enable puts output data bus in high-impedance state**
- **Advanced submicron CMOS technology**
- **Available in 32-pin plastic leaded chip carrier (PLCC) and 32-pin plastic Thin Quad FlatPack (TQFP)**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

DESCRIPTION:

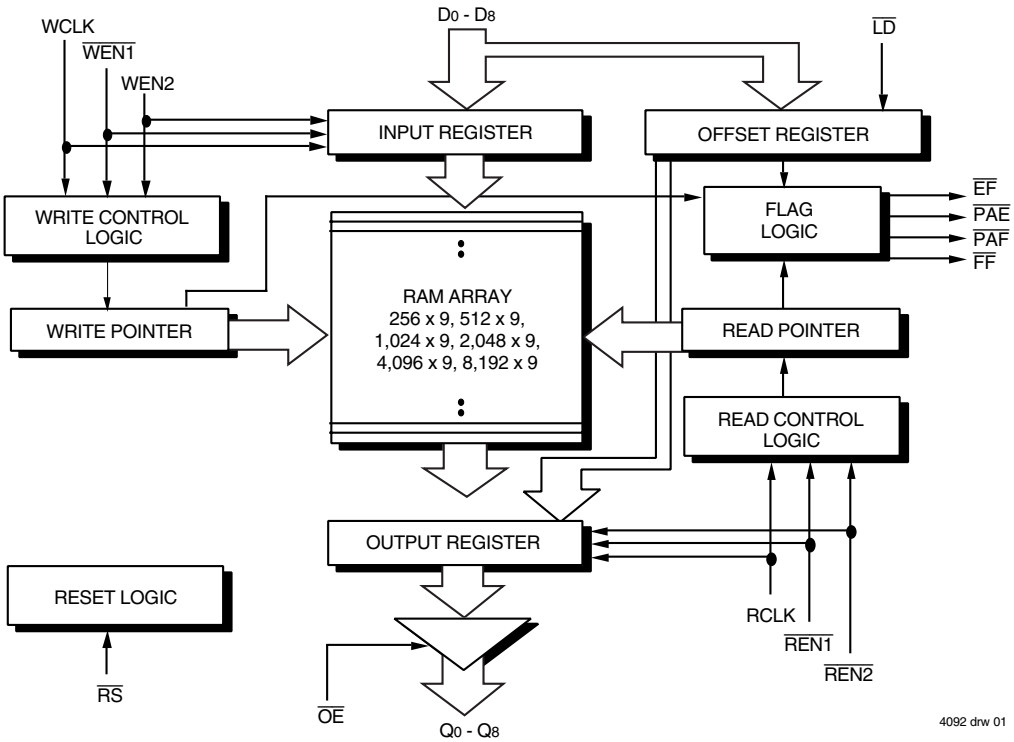
The IDT72V201/72V211/72V221/72V231/72V241/72V251 SyncFIFOs™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. The architecture, functional operation and pin assignments are identical to those of the IDT72201/72211/72221/72231/72241/72251, but operate at a power supply voltage (Vcc) between 3.0V and 3.6V. These devices have a 256, 512, 1,024, 2,048, 4,096 and 8,192 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks and interprocessor communication.

These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two Write Enable pins ($\overline{WEN1}$, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the Write Enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two Read Enable pins ($\overline{REN1}$, $\overline{REN2}$). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full (PAF), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the Load pin ($\overline{LD}$).

These FIFOs are fabricated using high-speed submicron CMOS technology.

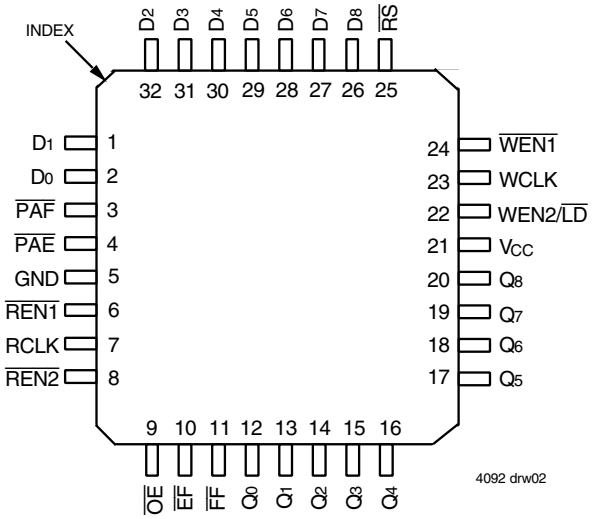
FUNCTIONAL BLOCK DIAGRAM



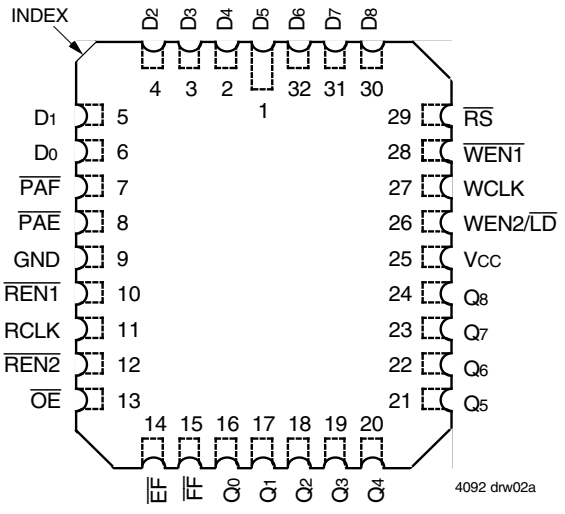
IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc. SyncFIFO is a trademark of Integrated Device Technology, Inc.

©2018 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice.

PIN CONFIGURATION



TQFP (PR32-1, order code: PF)
TOP VIEW



PLCC (J32-1, order code: J)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0-D_8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A Reset is required before an initial Write after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only Write Enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2/ Load	I	The FIFO is configured at Reset to have either two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at Reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at Reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
Q_0-Q_8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are asserted.
$\overline{REN1}$	Read Enable 1	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{REN2}$	Read Enable 2	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost-empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost-full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
V_{CC}	Power		One 3.3V volt power supply pin.
GND	Ground		One 0 volt ground pin.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Commercial/Industrial	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial/Industrial	2.0	—	5.5	V
V_{IL}	Input Low Voltage Commercial/Industrial	-0.5	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	-40	—	85	°C

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C;Industrial: V_{CC} = 3.3V ± 0.3V, T_A = -40°C to +85°C)

		IDT72V201 IDT72V211 IDT72V221 IDT72V231 IDT72V241 IDT72V251 Commercial and Industrial(1) t_{CLK} = 10, 15, 20 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}(2)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{LO}(3)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	V
I_{CC1}(4,5,6)	Active Power Supply Current	—	—	20	mA
I_{CC2}(4,7)	Standby Current	—	—	5	mA

NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Measurements with 0.4 ≤ VIN ≤ VCC.
3. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Tested with outputs disabled (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 0.17 + 0.48*fs + 0.02*C_L*fs (in mA) with V_{CC} = 3.3V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

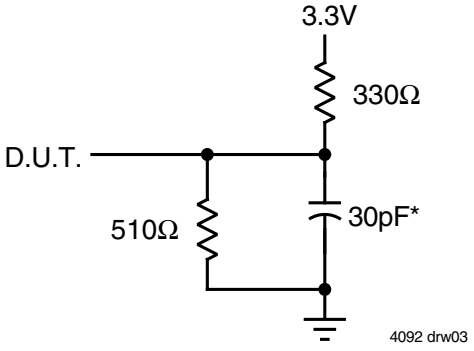
(Commercial: V_{CC} = 3.3 ±0.3V, TA = 0°C to + 70°C;Industrial: V_{CC} = 3.3 ±0.3V, TA = -40°C to + 85°C)

		Commercial		Com'l & Ind'l[2]		Commercial		
		IDT72V201L10 IDT72V211L10 IDT72V221L10 IDT72V231L10 IDT72V241L10 IDT72V251L10		IDT72V201L15 IDT72V211L15 IDT72V221L15 IDT72V231L15 IDT72V241L15 IDT72V251L15		IDT72V201L20 IDT72V211L20 IDT72V221L20 IDT72V231L20 IDT72V241L20 IDT72V251L20		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Clock Cycle Frequency	—	100	—	66.7	—	50	MHz
t_A	Data Access Time	2	6.5	2	10	2	12	ns
t_{CLK}	Clock Cycle Time	10	—	15	—	20	—	ns
t_{CLKH}	Clock High Time	4.5	—	6	—	8	—	ns
t_{CLKL}	Clock Low Time	4.5	—	6	—	8	—	ns
t_{DS}	Data Setup Time	3	—	4	—	5	—	ns
t_{DH}	Data Hold Time	0.5	—	1	—	1	—	ns
t_{ENS}	Enable Setup Time	3	—	4	—	5	—	ns
t_{ENH}	Enable Hold Time	0.5	—	1	—	1	—	ns
t_{RS}	Reset Pulse Width[1]	10	—	15	—	20	—	ns
t_{RSS}	Reset Setup Time	8	—	10	—	12	—	ns
t_{RSR}	Reset Recovery Time	8	—	10	—	12	—	ns
t_{RSF}	Reset to Flag and Output Time	—	10	—	15	—	20	ns
t_{OLZ}	Output Enable to Output in Low-Z[3]	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	—	3	8	3	10	ns
t_{OHZ}	Output Enable to Output in High-Z[3]	3	—	3	8	3	10	ns
t_{WFF}	Write Clock to Full Flag	—	6.5	—	10	—	12	ns
t_{REF}	Read Clock to Empty Flag	—	6.5	—	10	—	12	ns
t_{AF}	Write Clock to Almost-Full Flag	—	6.5	—	10	—	12	ns
t_{AE}	Read Clock to Almost-Empty Flag	—	6.5	—	10	—	12	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag &Full Flag	5	—	6	—	8	—	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	14	—	18	—	20	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Industrial temperature range is available by special order for speed grades faster than 15ns.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D0 - D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET (RS)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the Write Clock (WCLK). Data setup and hold times must be met in respect to the LOW-to-HIGH transition of the Write Clock (WCLK). The Full Flag (FF) and Programmable Almost-Full Flag (PAF) are synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK).

The Write and Read clocks can be asynchronous or coincident.

WRITE ENABLE 1 ($\overline{WEN1}$)

If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is low, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write Clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the Read Clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the Read Clock (RCLK).

The Write and Read clocks can be asynchronous or coincident.

READ ENABLES ($\overline{REN1}$, $\overline{REN2}$)

When both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the Read Clock (RCLK).

When either Read Enable ($\overline{REN1}$, $\overline{REN2}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enables ($\overline{REN1}$, $\overline{REN2}$) are ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

WRITE ENABLE 2/LOAD (WEN2/$\overline{LD}$)

This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set high at Reset ($\overline{RS}$ = LOW), this pin operates as a second Write Enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write Clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is HIGH and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is LOW, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set LOW at Reset ($\overline{RS}$ = LOW). The IDT72V201/72V211/72V221/72V231/72V241/72V251 devices contain four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set low, data on the inputs D is written into the Empty (Least Significant Bit) Offset register on the first LOW-to-HIGH transition of the Write Clock (WCLK). Data is written into the Empty (Most Significant Bit) Offset register on the second LOW-to-HIGH transition of the Write Clock (WCLK), into the Full (Least Significant Bit) Offset register on the third transition, and into the Full (Most Significant Bit) Offset register on the fourth transition. The fifth transition of the Write Clock (WCLK) again writes to the Empty (Least Significant Bit) Offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin HIGH, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW, and Write Enable 1 ($\overline{WEN1}$) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low and both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are set LOW. Data can be read on the LOW-to-HIGH transition of the Read Clock (RCLK).

A read and write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN1}$	WCLK	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

NOTES:
1. For the purposes of this table, WEN2 = V_{IH}.
2. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

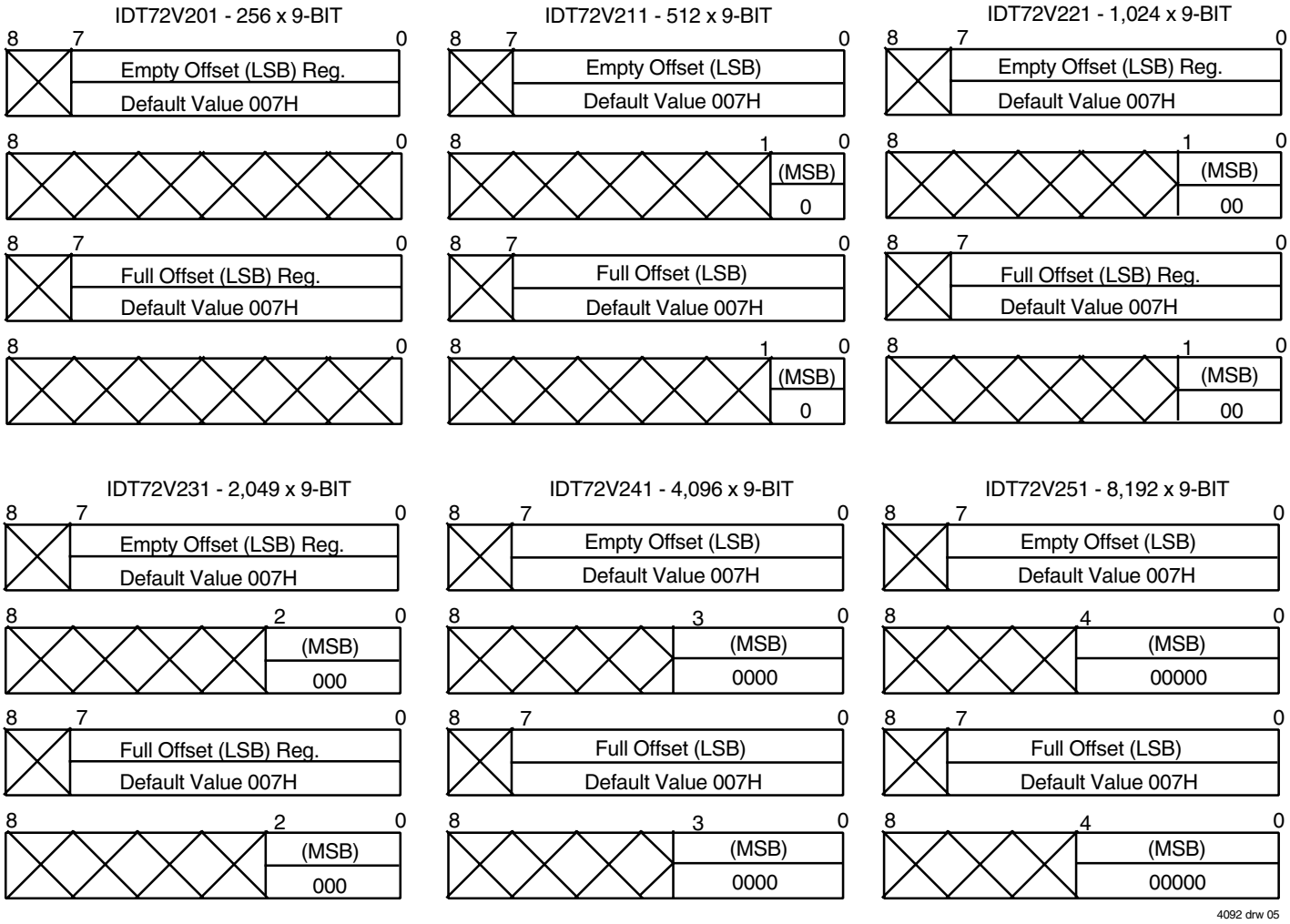


Figure 3. Offset Register Location and Default Values

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 256 writes for the IDT72V201, 512 writes for the IDT72V211, 1,024 writes for the IDT72V221, 2,048 writes for the IDT72V231, 4,096 writes for the IDT72V241 and 8,192 writes for the IDT72V251.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK).

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock (RCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full flag ($\overline{PAF}$) will go LOW when the FIFO reaches the almost-full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full flag ($\overline{PAF}$) will go LOW after (256-m) writes for the IDT72V201, (512-m) writes for the IDT72V211, (1,024-m) writes for the IDT72V221, (2,048-m) writes for the IDT72V231, (4,096-m) writes for the IDT72V241 and (8,192-m) writes for the IDT72V251. The offset "m" is defined in the Full Offset registers.

If there is no full offset specified, the Programmable Almost-Full flag ($\overline{PAF}$) will go LOW at Full-7 words.

The Programmable Almost-Full flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK).

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset registers. If no reads are performed after Reset the Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after "n+1" for the IDT72V201/72V211/72V221/72V231/72V241/72V251.

If there is no empty offset specified, the Programmable Almost-Empty flag ($\overline{PAE}$) will go LOW at Empty+7 words.

The Programmable Almost-Empty flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock (RCLK).

DATA OUTPUTS (Q_0 - Q_8)

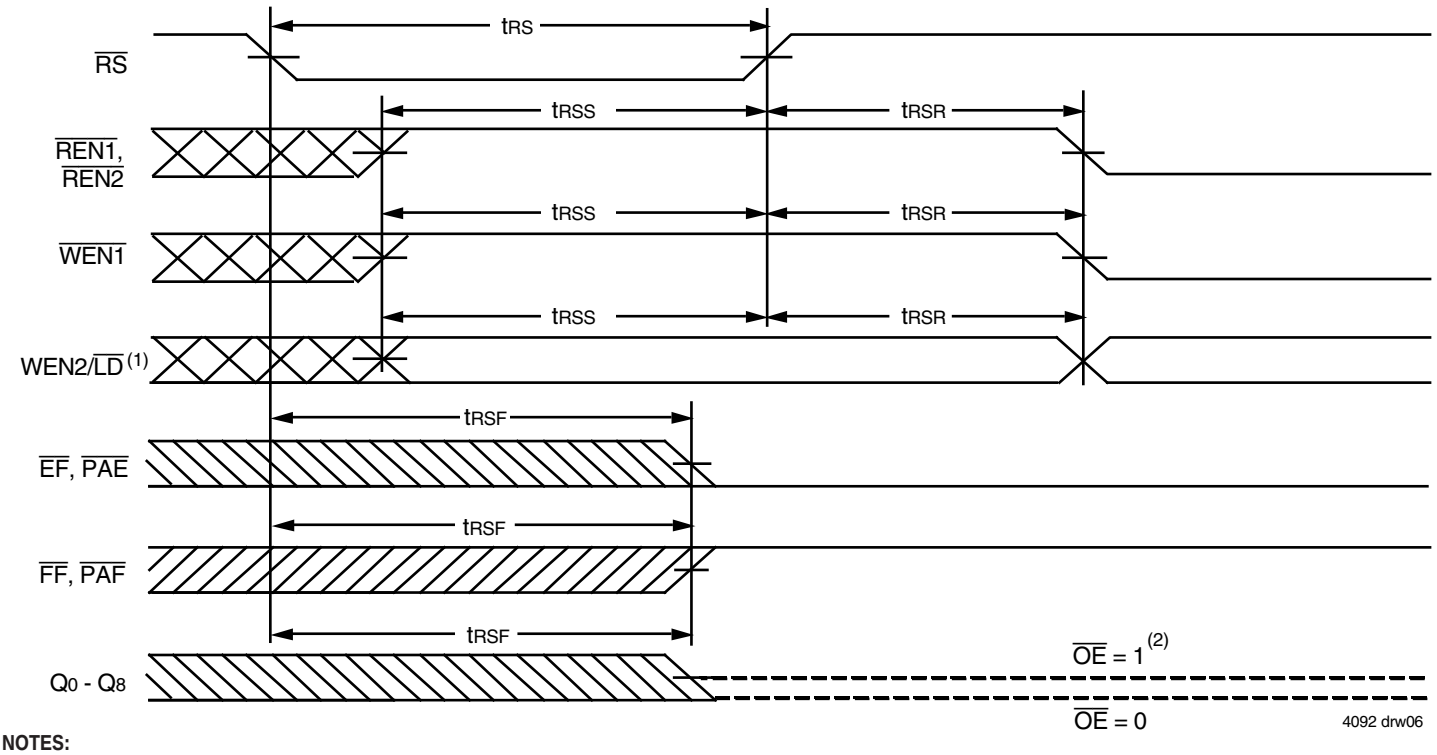
Data outputs for a 9-bit wide data.

TABLE 1 — STATUS FLAGS

NUMBER OF WORDS IN FIFO						
IDT72V201	IDT72V211	IDT72V221	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (1,024-(m+1))	H	H	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1,024-m)[2] to 1,023	H	L	H	H
256	512	1,024	L	L	H	H

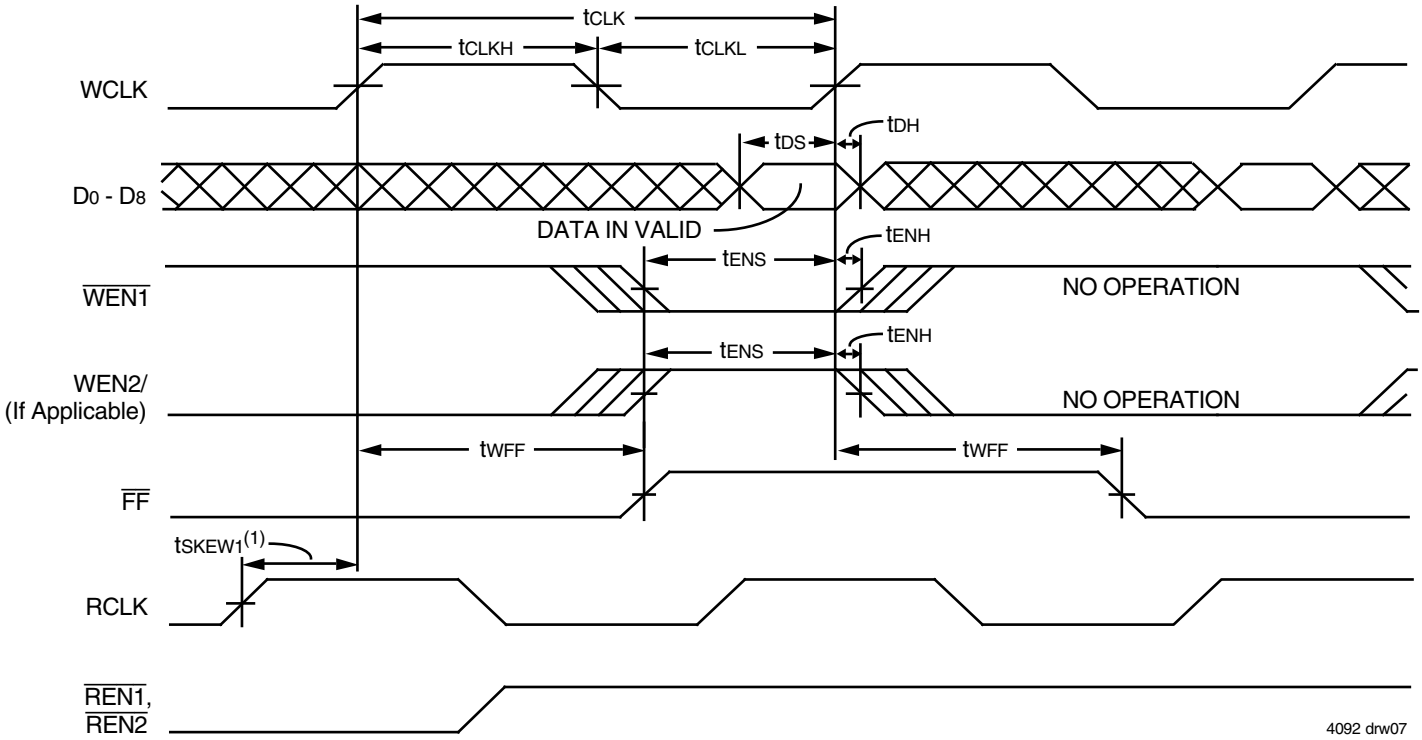
NUMBER OF WORDS IN FIFO						
IDT72V231	IDT72V241	IDT72V251	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (2,048-(m+1))	(n+1) to (4,096-(m+1))	(n+1) to (8,192-(m+1))	H	H	H	H
(2,048-m)[2] to 2,047	(4,096-m)[2] to 4,095	(8,192-m)[2] to 8,191	H	L	H	H
2,048	4,096	8,192	L	L	H	H

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



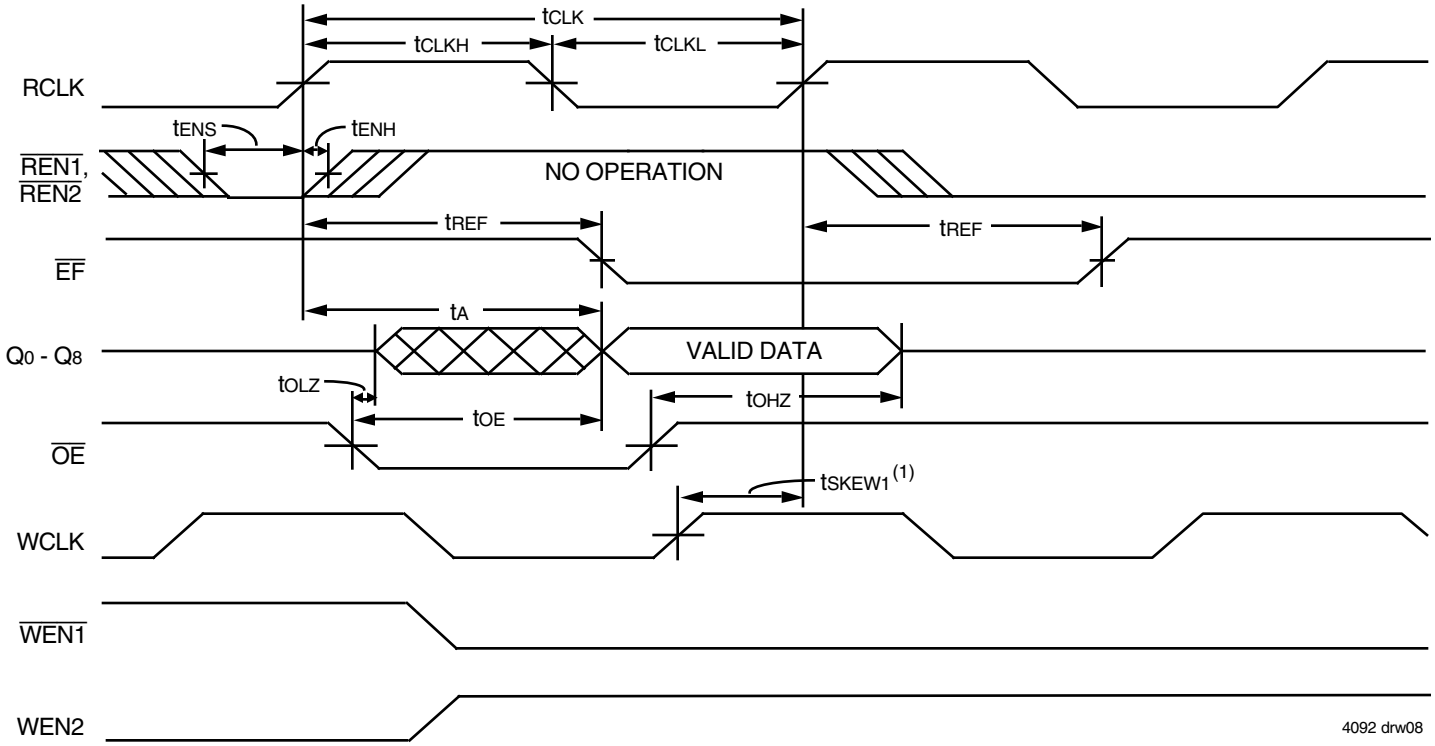
NOTES:
1. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and high-impedance if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

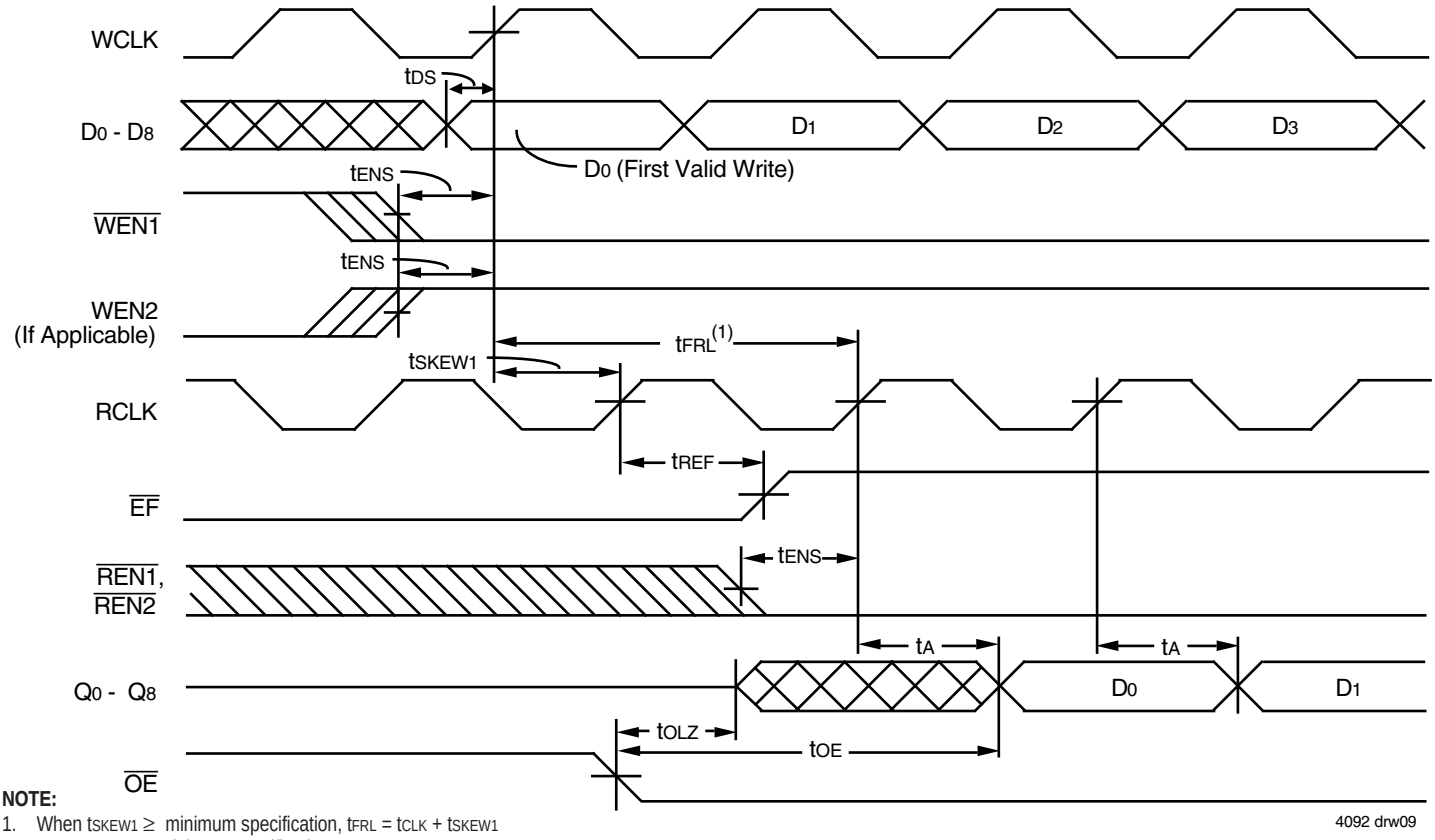
Figure 5. Write Cycle Timing



NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

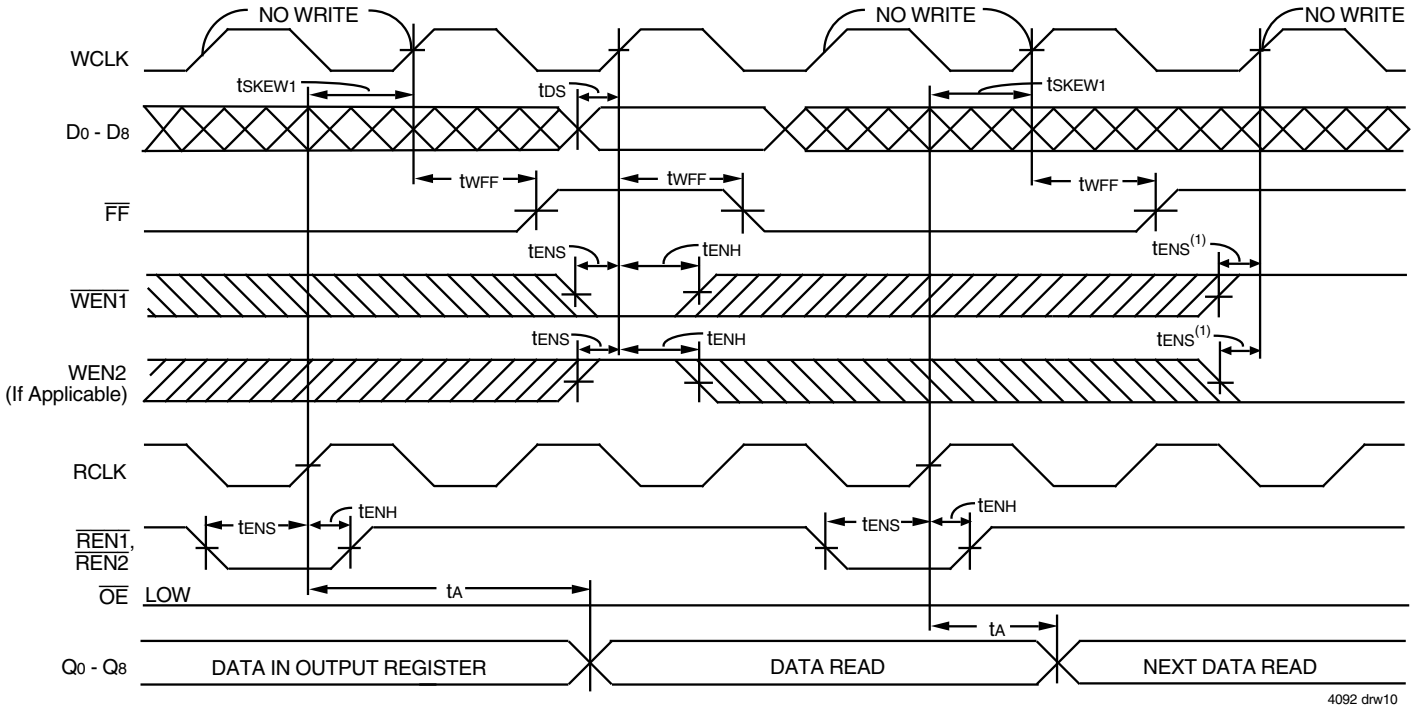
Figure 6. Read Cycle Timing



NOTE:

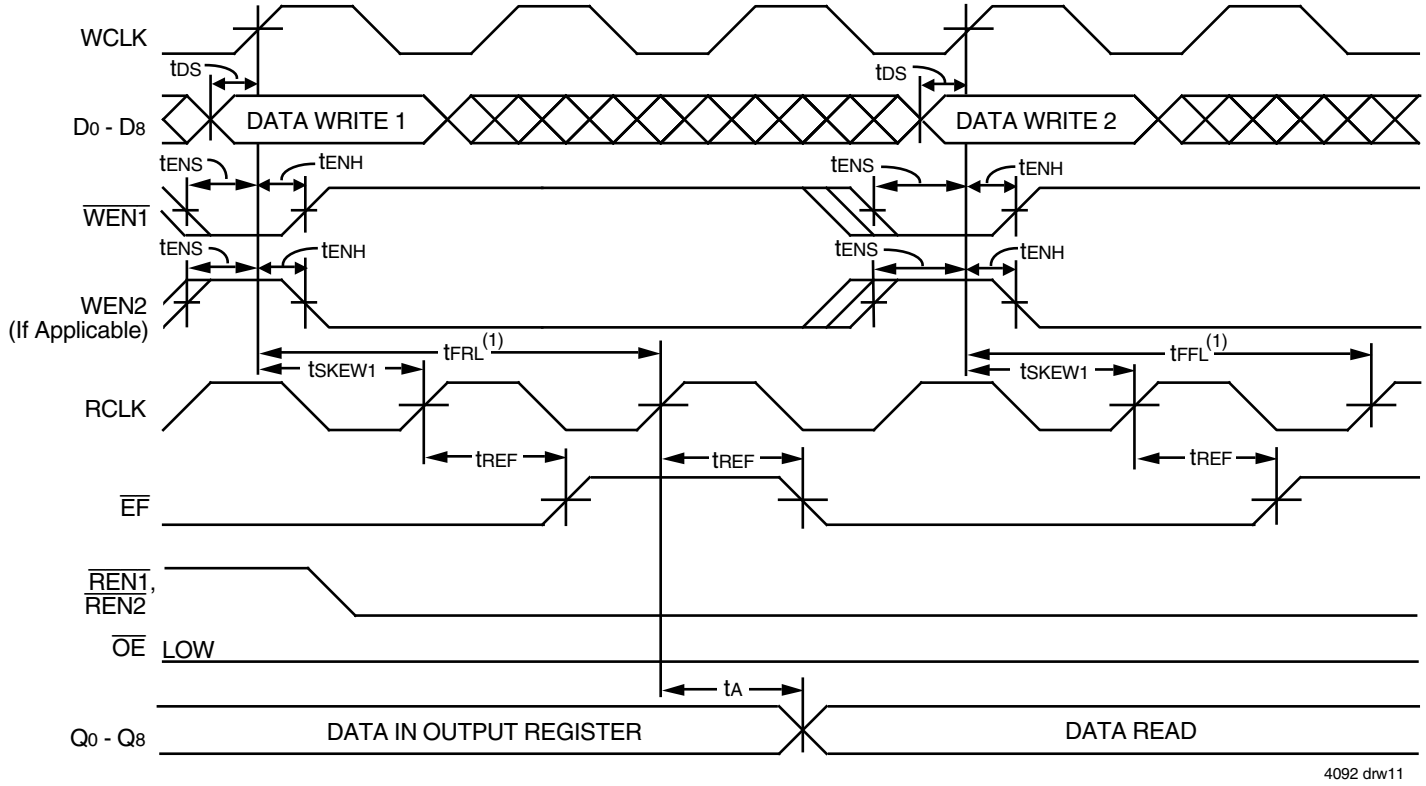
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing



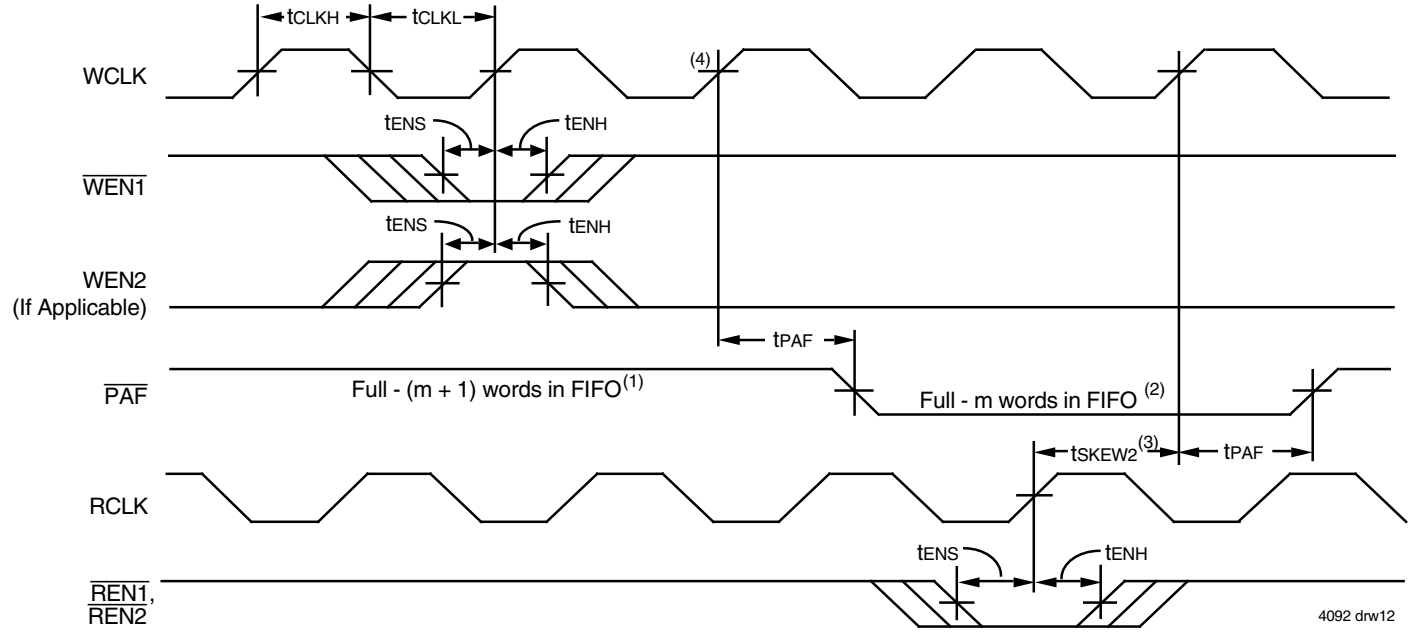
NOTE:
1. Only one of the two Write Enable inputs, $\overline{WEN1}$ or $\overline{WEN2}$, needs to go inactive to inhibit writes to the FIFO.

Figure 8. Full Flag Timing



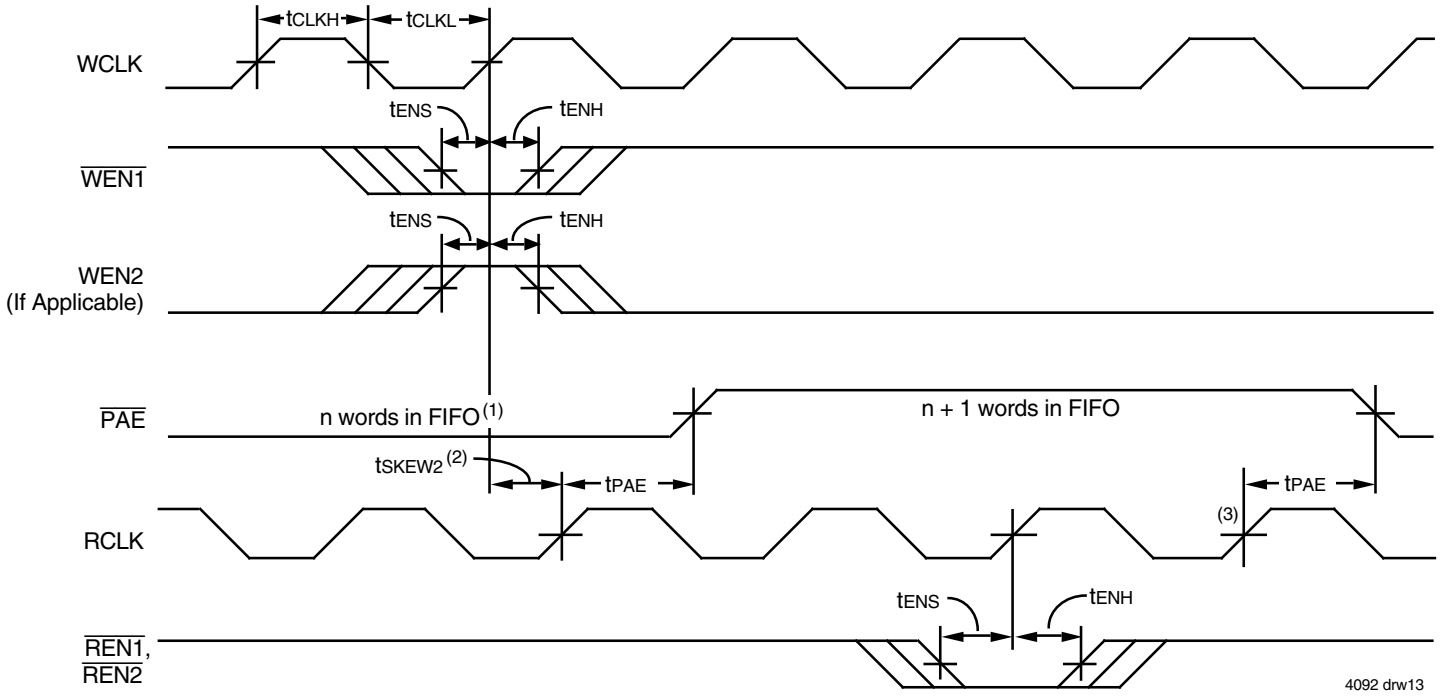
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. Empty Flag Timing



NOTES:
1. m = $\overline{PAF}$ offset.
2. 256 - m words in FIFO for IDT72V201, 512 - m words for IDT72V211, 1,024 - m words for IDT72V221, 2,048 - m words for IDT72V231, 4,096 - m words for IDT72V241, 8,192 - m words for IDT72V251.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. n = $\overline{PAE}$ offset.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes LOW.

Figure 11. Programmable Empty Flag Timing

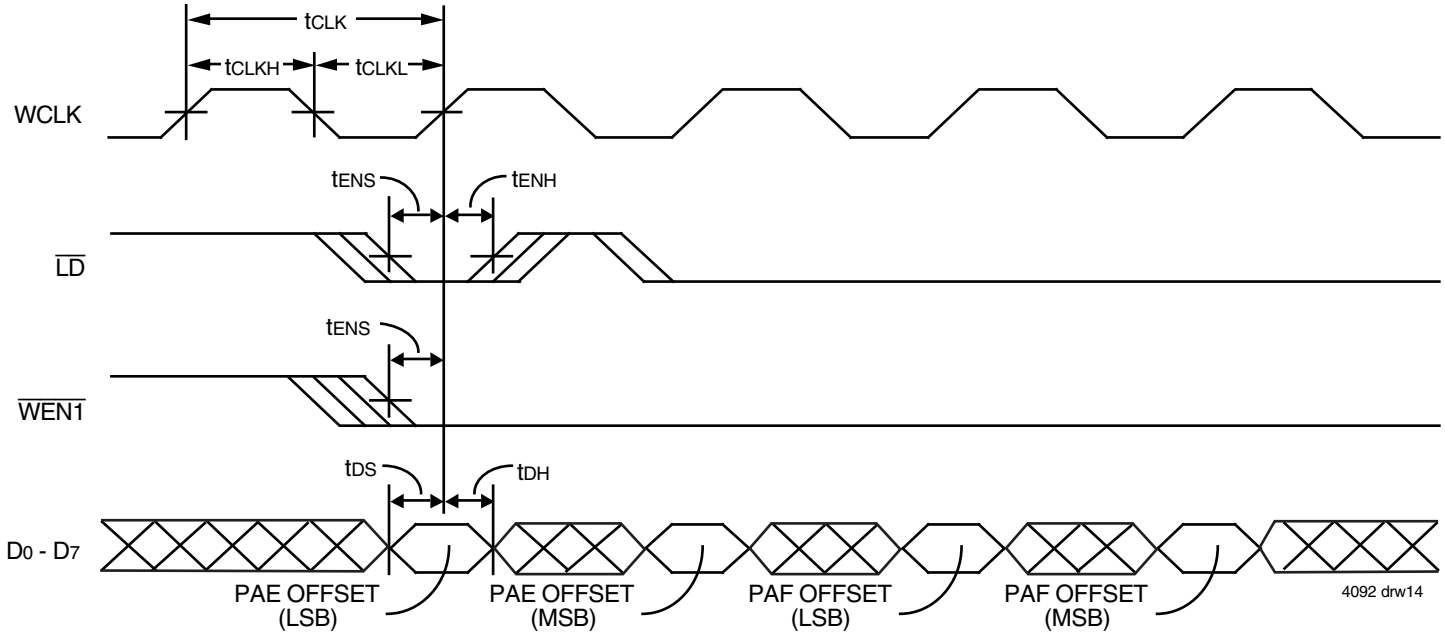


Figure 12. Write Offset Registers Timing

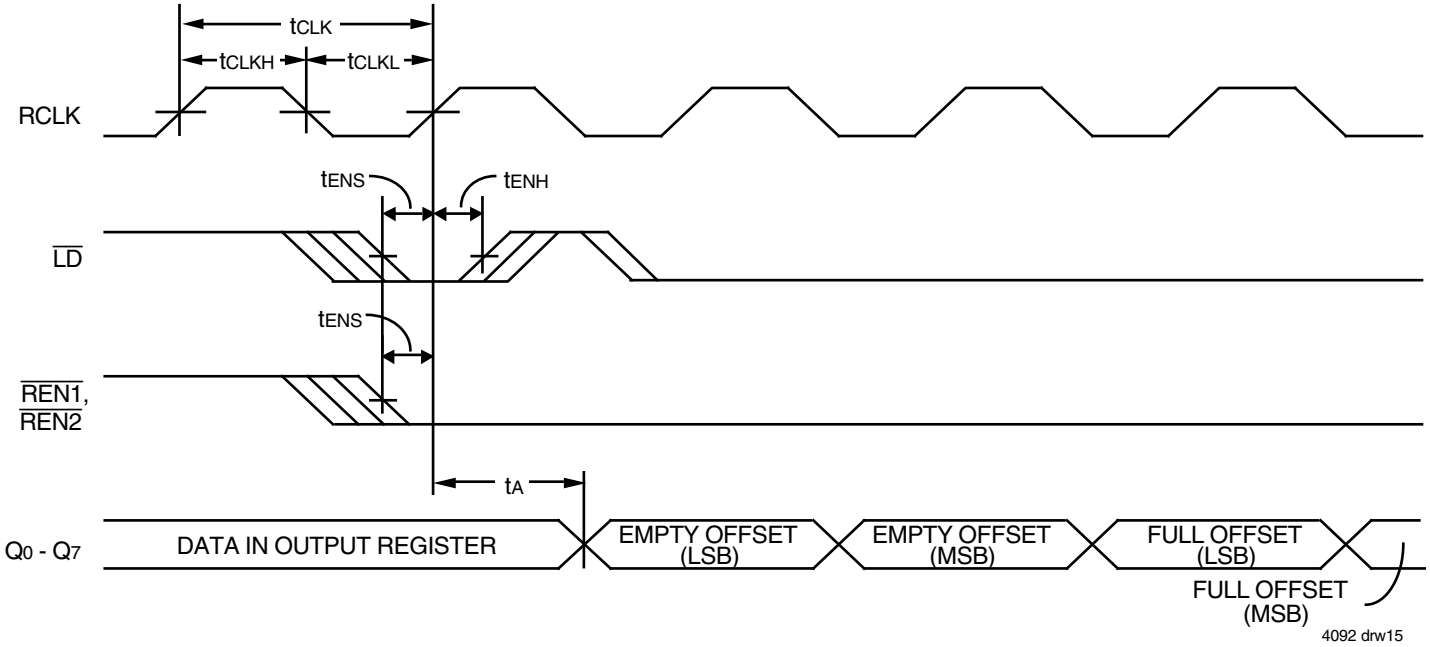


Figure 13. Read Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72V201/72V211/72V221/72V231/72V241/72V251 may be used when the application requirements are for 256/512/1,024/2,048/4,096/8,192 words or less. When these FIFOs are in a Single Device Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

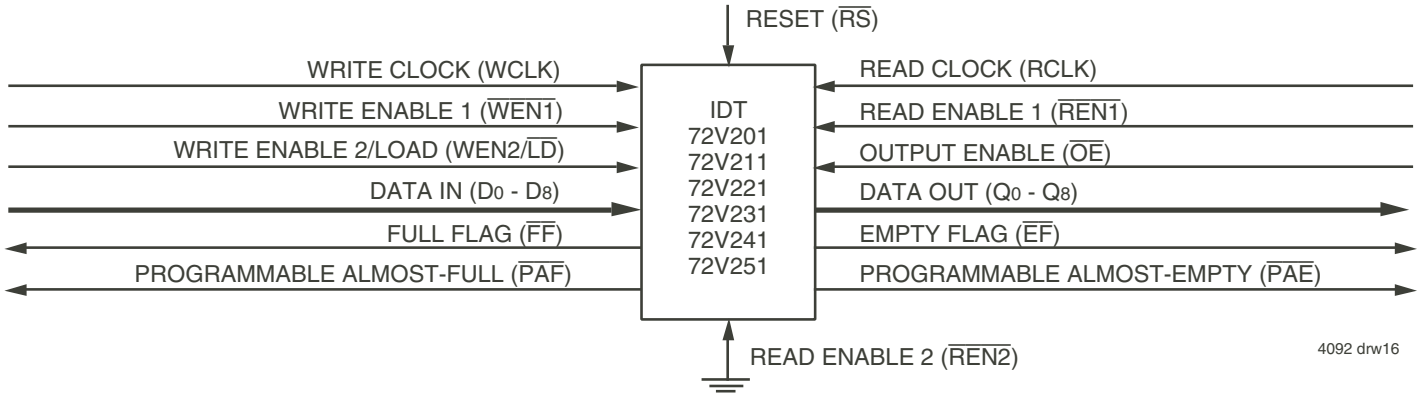


Figure 14. Block Diagram of Single 256 x 9, 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9 and 8,192 x 9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{AE}$ and $\overline{AF}$) can be detected from any one device. Figure 15 demonstrates a 18-bit word width by using two IDT72V201/72V211/72V221/72V231/72V241/72V251s. Any word width can be attained by adding additional IDT72V201/72V211/72V221/72V231/72V241/72V251s.

When these devices are in a Width Expansion Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

DEPTH EXPANSION

The IDT72V201/72V211/72V221/72V231/72V241/72V251 can be adapted to applications when the requirements are for greater than 256/512/1,024/2,048/4,096/8,192 words. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. These FIFOs operate in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

Please see the Application Note" DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

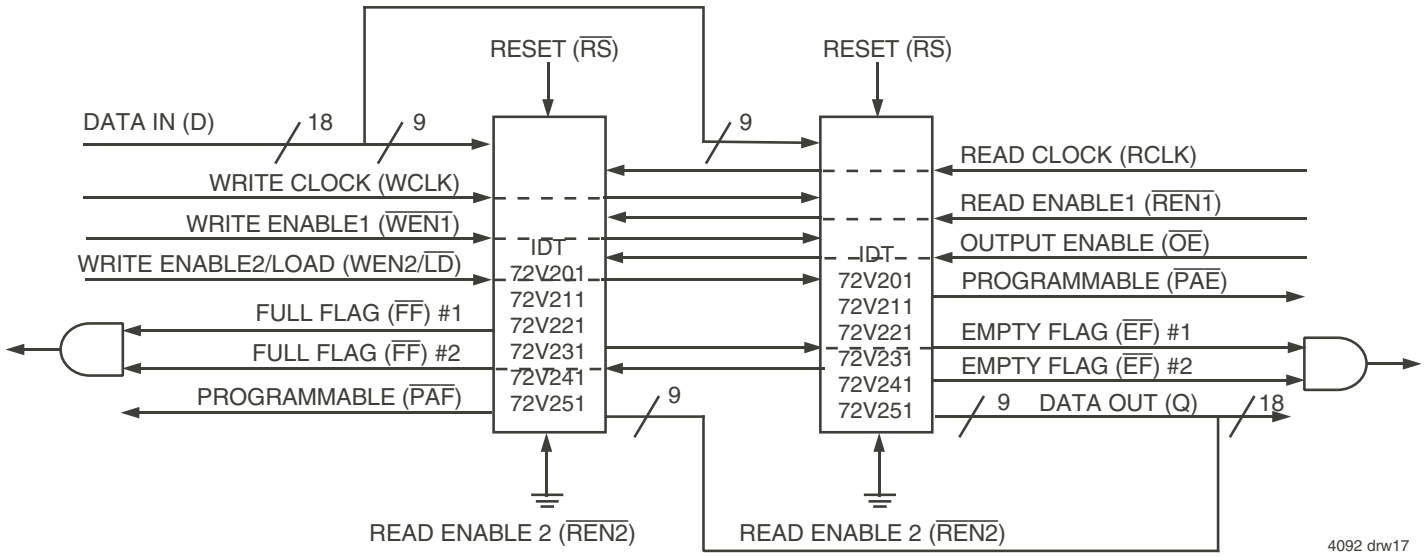
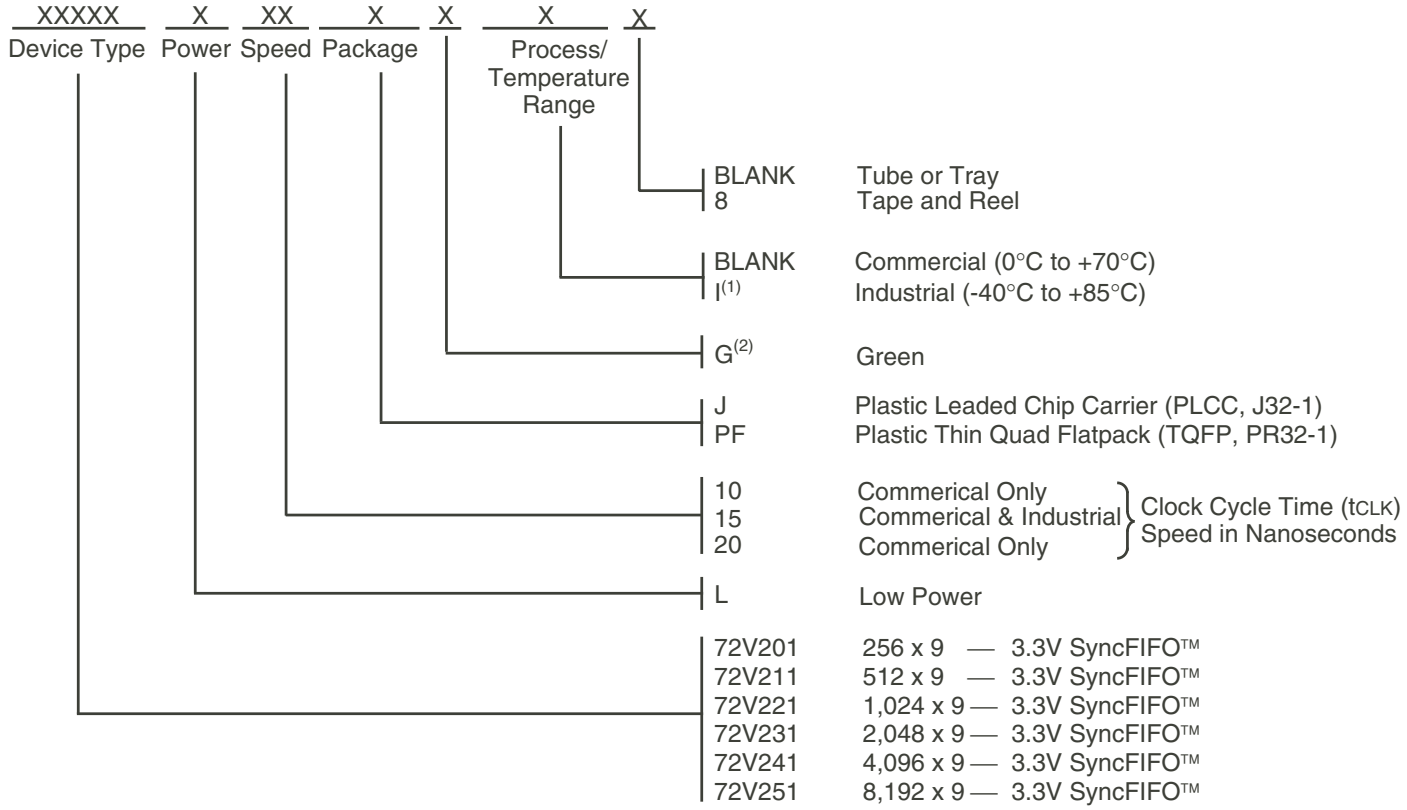


Figure 15. Block Diagram of 256 x 18, 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18 and 8,192 x 18 Synchronous FIFO Used in a Width Expansion Configuration

ORDERING INFORMATION



4092 drw 18

NOTES:

1. Industrial temperature range product for the 15ns is available as a standard device. All other speed grades are available by special order.
2. Green parts available. For specific speeds and packages contact your sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

DATASHEET DOCUMENT HISTORY

01/11/2002	pg. 3.
02/01/2002	pg. 3.
02/08/2006	pgs. 1 and 14.
10/22/2008	pg. 14.
08/08/2013	pgs. 1, 13 and 14.
03/19/2018	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-360-1753
email: FIFOhelp@idt.com