Quad, 12-Bit, 170 MSPS/210 MSPS Serial Output 1.8 V ADC

Data Sheet

AD9639

FEATURES

- 4 ADCs in one package
- JESD204 coded serial digital outputs
- On-chip temperature sensor
- −95 dB channel-to-channel crosstalk
- SNR: 65 dBFS with AIN = 85 MHz at 210 MSPS
- SFDR: 77 dBc with AIN = 85 MHz at 210 MSPS
- Excellent linearity
  - DNL: ±0.28 LSB (typical)
  - INL: ±0.7 LSB (typical)
- 780 MHz full power analog bandwidth
- Power dissipation: 325 mW per channel at 210 MSPS
- 1.25 V p-p input voltage range, adjustable up to 1.5 V p-p
- 1.8 V supply operation
- Clock duty cycle stabilizer
- Serial port interface features
  - Power-down modes
  - Digital test pattern enable
  - Programmable header
  - Programmable pin functions (PGMx, PDWN)

APPLICATIONS

- Communication receivers
- Cable head end equipment/M-CMTS
- Broadband radios
- Wireless infrastructure transceivers
- Radar/military-aerospace subsystems
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

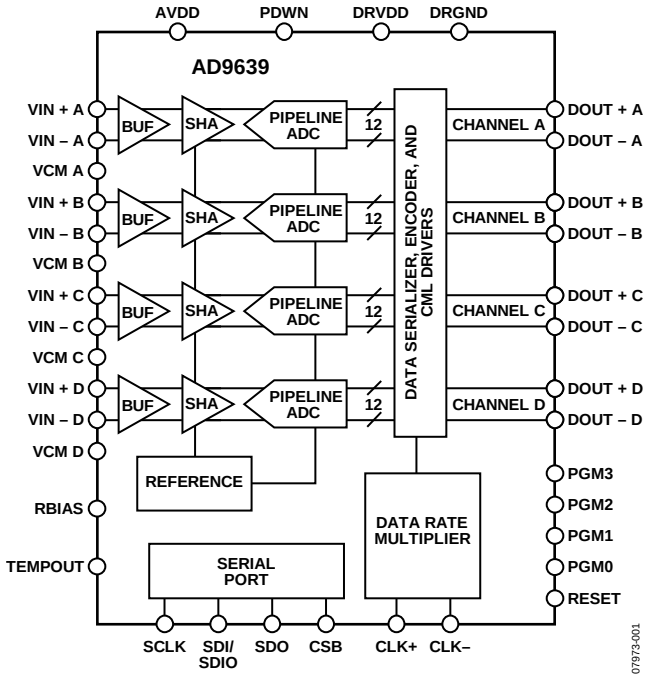

Figure 1.

GENERAL DESCRIPTION

The AD9639 is a quad, 12-bit, 210 MSPS analog-to-digital converter (ADC) with an on-chip temperature sensor and a high speed serial interface. It is designed to support the digitizing of high frequency, wide dynamic range signals with an input bandwidth of up to 780 MHz. The output data is serialized and presented in packet format, consisting of channel-specific information, coded samples, and error code correction.

The ADC requires a single 1.8 V power supply. The input clock can be driven differentially with a sine wave, LVPECL, CMOS, or LVDS. A clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles. The on-chip reference eliminates the need for external decoupling and can be adjusted by means of SPI control.

Various power-down and standby modes are supported. The ADC typically consumes 150 mW per channel with the digital link still in operation when standby operation is enabled.

Fabricated on an advanced CMOS process, the AD9639 is available in a Pb-free/RoHS-compliant, 72-lead LFCSP package. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Four ADCs are contained in a small, space-saving package.
2. An on-chip PLL allows users to provide a single ADC sampling clock; the PLL distributes and multiplies up to produce the corresponding data rate clock.
3. The JESD204 coded data rate supports up to 4.2 Gbps per channel.
4. The AD9639 operates from a single 1.8 V power supply.
5. Flexible synchronization schemes and programmable mode pins are available.
6. An on-chip temperature sensor is included.

Rev. C
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REVISION HISTORY

5/14—Rev. B to Rev. C

Changes to Digital Outputs and Timing Section ... 27
Changes to Table 15 ... 33

7/13—Rev. A to Rev. B

Change to Current Drive Parameter, Table 1 ... 3
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2/10—Rev. 0 to Rev. A

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5/09—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 1.

		AD9639BCPZ-170			AD9639BCPZ-210			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	25°C		−2	±12		−2	±12	mV
Offset Matching	25°C		4	12		4	12	mV
Gain Error	25°C	−2.8	+1	+4.7	−2.8	+1	+4.7	% FS
Gain Matching	25°C		0.9	2.7		0.9	2.7	% FS
Differential Nonlinearity (DNL)	Full		±0.28	±0.6		±0.28	±0.6	LSB
Integral Nonlinearity (INL)	Full		±0.45	±0.9		±0.7	±1.3	LSB
ANALOG INPUTS								
Differential Input Voltage Range[2]	Full	1.0	1.25	1.5	1.0	1.25	1.5	V p-p
Common-Mode Voltage	Full		1.4			1.4		V
Input Capacitance	25°C		2			2		pF
Input Resistance	Full		4.3			4.3		kΩ
Analog Bandwidth, Full Power	Full		780			780		MHz
Voltage Common Mode (VCM x Pins)								
Voltage Output	Full	1.4	1.44	1.5	1.4	1.44	1.5	V
Current Drive	Full		1			1		mA
TEMPERATURE SENSOR OUTPUT			−1.12			−1.12		mV/°C
Voltage Output	Full		739			737		mV
Current Drive	Full		50			50		µA
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD}	Full		535	570		610	650	mA
I_{DRVDD}	Full		98	105		111	120	mA
Total Power Dissipation (Including Output Drivers)	Full		1.139	1.215		1.298	1.386	W
Power-Down Dissipation	Full		3			3		mW
Standby Dissipation[2]	Full		152			173		mW
CROSSTALK	Full		−95			−95		dB
Overrange Condition[3]	Full		−90			−90		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] AVDD/DRVDD, with link established.
[3] Overrange condition is specified as 6 dB above the full-scale input range.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 2.

		AD9639BCPZ-170			AD9639BCPZ-210			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 84.3 MHz	Full	63.5	64.5		63.2	64.2		dB
f_{IN} = 240.3 MHz	25°C		64.1			63.2		dB
SIGNAL-TO-(NOISE + DISTORTION) (SINAD) RATIO								
f_{IN} = 84.3 MHz	Full	63.3	64.4		62.8	63.9		dB
f_{IN} = 240.3 MHz	25°C		63.9			63		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 84.3 MHz	Full	10.2	10.4		10.1	10.3		Bits
f_{IN} = 240.3 MHz	25°C		10.3			10.2		Bits
WORST HARMONIC (SECOND)								
f_{IN} = 84.3 MHz	Full		87.5	78.6		86	77	dBc
f_{IN} = 240.3 MHz	25°C		82			80		dBc
WORST HARMONIC (THIRD)								
f_{IN} = 84.3 MHz	Full		79	74		76	72.6	dBc
f_{IN} = 240.3 MHz	25°C		84			77		dBc
WORST OTHER (EXCLUDING SECOND OR THIRD)								
f_{IN} = 84.3 MHz	Full		96	86		90	83.7	dBc
f_{IN} = 240.3 MHz	25°C		88			88		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)								
f_{IN1} = 140.2 MHz, f_{IN2} = 141.3 MHz, AIN1 and AIN2 = −7.0 dBFS	25°C		78			77		dBc
f_{IN1} = 170.2 MHz, f_{IN2} = 171.3 MHz, AIN1 and AIN2 = −7.0 dBFS[2]	25°C					77		dBc

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Tested at 170 MSPS and 210 MSPS.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 3.

		AD9639BCPZ-170			AD9639BCPZ-210			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUTS (CLK+, CLK–)								
Logic Compliance	Full		LVPECL/LVDS/CMOS			LVPECL/LVDS/CMOS		
Differential Input Voltage	Full	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD − 0.3		AVDD + 1.6	AVDD − 0.3		AVDD + 1.6	
Internal Common-Mode Bias	Full		1.2			1.2		V
Input Common-Mode Voltage	Full	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V_{IH})	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V_{IL})	Full	0		0.8	0		0.8	V
High Level Input Current (I_{IH})	Full	−10		+10	−10		+10	µA
Low Level Input Current (I_{IL})	Full	−10		+10	−10		+10	µA
Differential Input Resistance	25°C	16	20	24	16	20	24	kΩ
Input Capacitance	25°C		4			4		pF
LOGIC INPUTS (PDWN, CSB, SDI/SDIO, SCLK, RESET, PGMx)[2]								
Logic 1 Voltage	Full	0.8 × AVDD			0.8 × AVDD			V
Logic 0 Voltage	Full			0.2 × AVDD			0.2 × AVDD	V
Logic 1 Input Current (CSB)	Full		0			0		µA
Logic 0 Input Current (CSB)	Full		−60			−60		µA
Logic 1 Input Current (PDWN, SDI/SDIO, SCLK, RESET, PGMx)	Full		55			55		µA
Logic 0 Input Current (PDWN, SDI/SDIO, SCLK, RESET, PGMx)	Full		0			0		µA
Input Resistance	25°C		30			30		kΩ
Input Capacitance	25°C		4			4		pF
LOGIC OUTPUT (SDO)								
Logic 1 Voltage	Full	1.2		AVDD + 0.3	1.2		AVDD + 0.3	V
Logic 0 Voltage	Full	0		0.3	0		0.3	V
DIGITAL OUTPUTS (DOUT + x, DOUT − x)								
Logic Compliance			CML			CML		
Differential Output Voltage	Full		0.8			0.8		V
Common-Mode Voltage	Full		DRVDD/2			DRVDD/2		V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Specified for 13 SDI/SDIO pins on the same SPI bus.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T_{MIN} = −40°C, T_{MAX} = +85°C, 1.25 V p-p differential input, AIN = −1.0 dBFS, DCS enabled, unless otherwise noted.

Table 4.

		AD9639BCPZ-170			AD9639BCPZ-210			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK								
Clock Rate	Full	100		170	100		210	MSPS
Clock Pulse Width High (t_{EH})	Full	2.65	2.9		2.15	2.4		ns
Clock Pulse Width Low (t_{EL})	Full	2.65	2.9		2.15	2.4		ns
DATA OUTPUT PARAMETERS								
Data Output Period or UI (DOUT + x, DOUT − x)	Full		1/(20 × f_{CLK})			1/(20 × f_{CLK})		Seconds
Data Output Duty Cycle	25°C		50			50		%
Data Valid Time	25°C		0.8			0.8		UI
PLL Lock Time (t_{LOCK})	25°C		4			4		µs
Wake-Up Time (Standby)	25°C		250			250		ns
Wake-Up Time (Power-Down)[2]	25°C		50			50		µs
Pipeline Latency	Full			40			40	CLK cycles
Data Rate per Channel (NRZ)	25°C		3.4			4.2		Gbps
Deterministic Jitter	25°C		10			10		ps
Random Jitter	25°C		6			6		ps rms
Channel-to-Channel Bit Skew	25°C		0			0		Seconds
Channel-to-Channel Packet Skew[3]	25°C		±1			±1		CLK cycles
Output Rise/Fall Time	25°C		50			50		ps
TERMINATION CHARACTERISTICS								
Differential Termination Resistance	25°C		100			100		Ω
APERTURE								
Aperture Delay (t_A)	25°C		1.2			1.2		ns
Aperture Uncertainty (Jitter)	25°C		0.2			0.2		ps rms
OUT-OF-RANGE RECOVERY TIME	25°C		1			1		CLK cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and details on how these tests were completed.
[2] Receiver dependent.
[3] See the Serial Data Frame section.

TIMING DIAGRAM

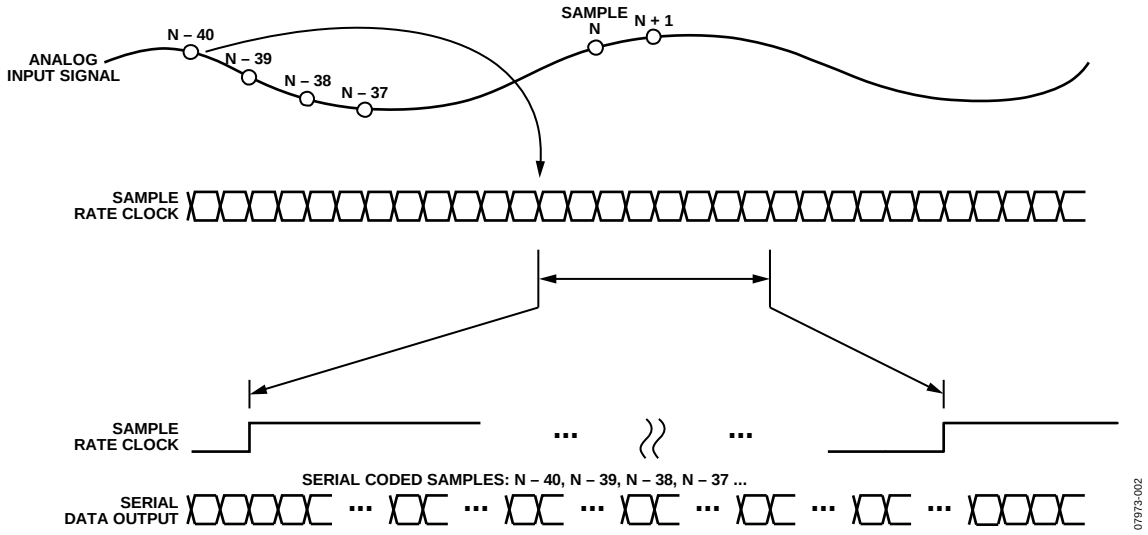


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
DOUT + x/DOUT − x to DRGND	−0.3 V to DRVDD + 0.3 V
SDO, SDI/SDIO, CLK±, VIN ± x, VCM x, TEMPOUT, RBIAS to AGND	−0.3 V to AVDD + 0.3 V
SCLK, CSB, PGMx, RESET, PDWN to AGND	−0.3 V to AVDD + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
72-Lead LFCSP (CP-72-3)	16.2	7.9	0.6	°C/W

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

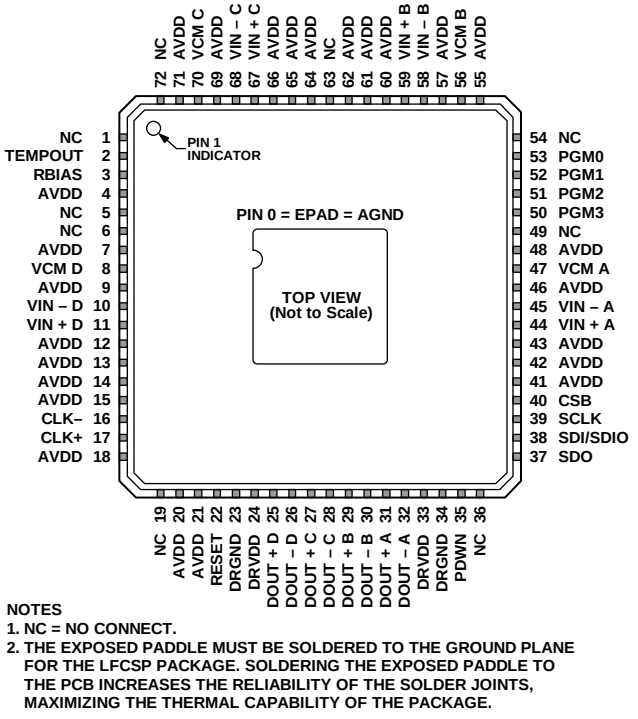


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND	Analog Ground (Exposed Paddle). The exposed paddle must be soldered to the ground plane. Soldering the exposed paddle to the PCB increases the reliability of the solder joints, maximizing the thermal capability of the package.
1, 5, 6, 19, 36, 49, 54, 63, 72	NC	No Connection.
2	TEMPOUT	Output Voltage to Monitor Temperature.
3	RBIAS	External Resistor to Set the Internal ADC Core Bias Current.
4, 7, 9, 12, 13, 14, 15, 18, 20, 21, 41, 42, 43, 46, 48, 55, 57, 60, 61, 62, 64, 65, 66, 69, 71	AVDD	1.8 V Analog Supply.
8	VCM D	Common-Mode Output Voltage Reference.
10	VIN – D	ADC D Analog Input Complement.
11	VIN + D	ADC D Analog Input True.
16	CLK–	Clock Input Complement.
17	CLK+	Clock Input True.
22	RESET	Reset Enable Pin. Resets the digital output timing.
23, 34	DRGND	Digital Output Driver Ground.
24, 33	DRVDD	1.8 V Digital Output Driver Supply.
25	DOUT + D	ADC D Digital Output True.
26	DOUT – D	ADC D Digital Output Complement.
27	DOUT + C	ADC C Digital Output True.
28	DOUT – C	ADC C Digital Output Complement.
29	DOUT + B	ADC B Digital Output True.
30	DOUT – B	ADC B Digital Output Complement.

Pin No.	Mnemonic	Description
31	DOUT + A	ADC A Digital Output True.
32	DOUT − A	ADC A Digital Output Complement.
35	PDWN	Power-Down.
37	SDO	Serial Data Output for 4-Wire SPI Interface.
38	SDI/SDIO	Serial Data Input/Serial Data Input/Output for 3-Wire SPI Interface.
39	SCLK	Serial Clock.
40	CSB	Chip Select Bar.
44	VIN + A	ADC A Analog Input True.
45	VIN − A	ADC A Analog Input Complement.
47	VCM A	Common-Mode Output Voltage Reference.
50, 51, 52, 53	PGM3, PGM2, PGM1, PGM0	Optional Pins to be Programmed by Customer.
56	VCM B	Common-Mode Output Voltage Reference.
58	VIN − B	ADC B Analog Input Complement.
59	VIN + B	ADC B Analog Input True.
67	VIN + C	ADC C Analog Input True.
68	VIN − C	ADC C Analog Input Complement.
70	VCM C	Common-Mode Output Voltage Reference.

TYPICAL PERFORMANCE CHARACTERISTICS

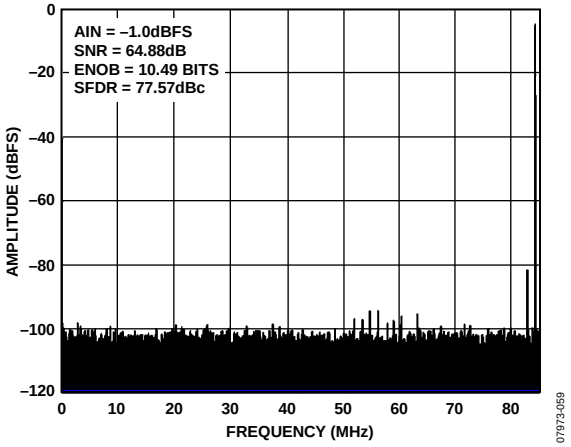


Figure 4. Single-Tone 32k FFT with f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

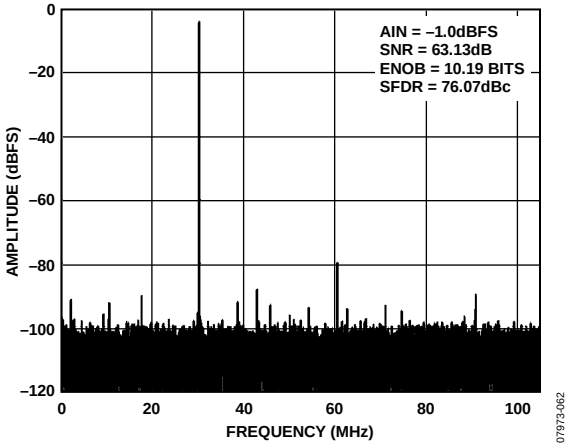


Figure 7. Single-Tone 32k FFT with f_{IN} = 240.3 MHz, f_{SAMPLE} = 210 MSPS

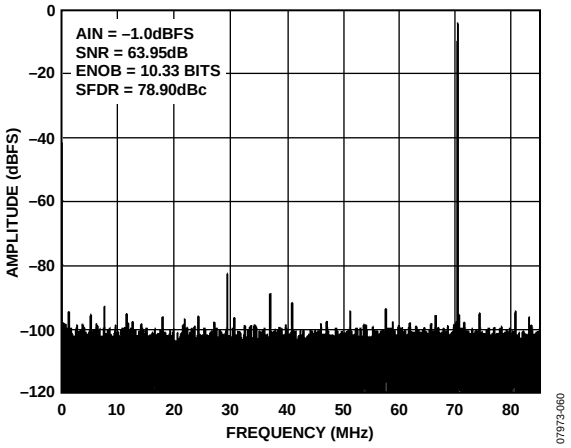


Figure 5. Single-Tone 32k FFT with f_{IN} = 240.3 MHz, f_{SAMPLE} = 170 MSPS

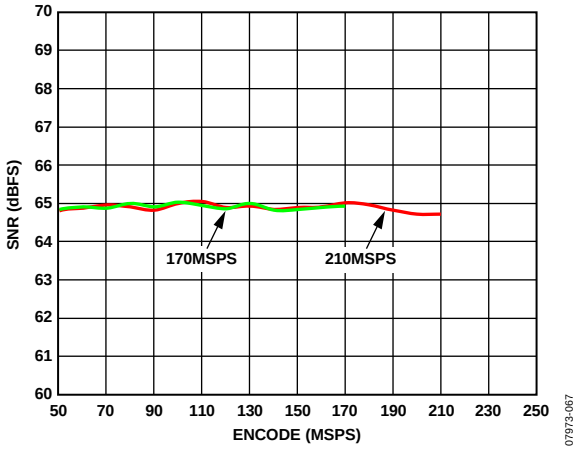


Figure 8. SNR vs. Encode, f_{IN} = 84.3 MHz

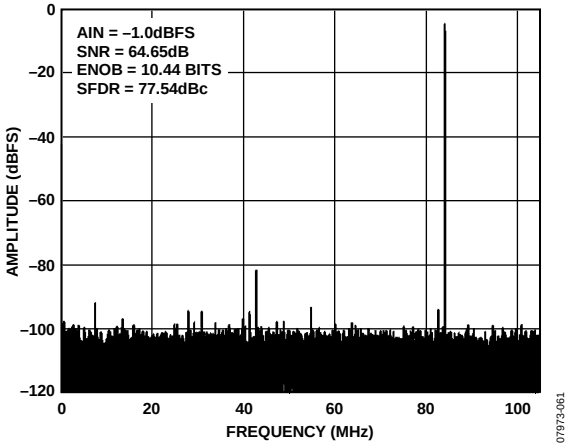


Figure 6. Single-Tone 32k FFT with f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

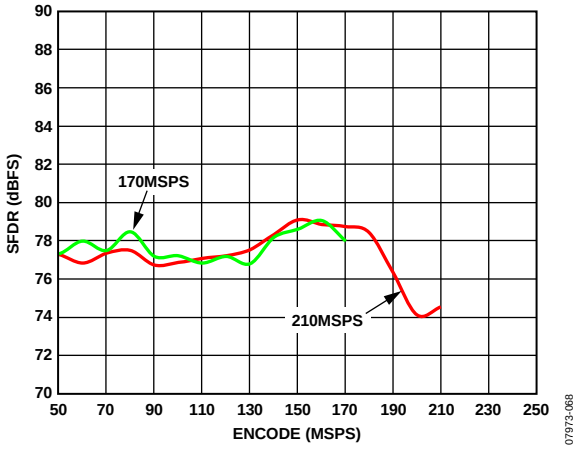


Figure 9. SFDR vs. Encode, f_{IN} = 84.3 MHz

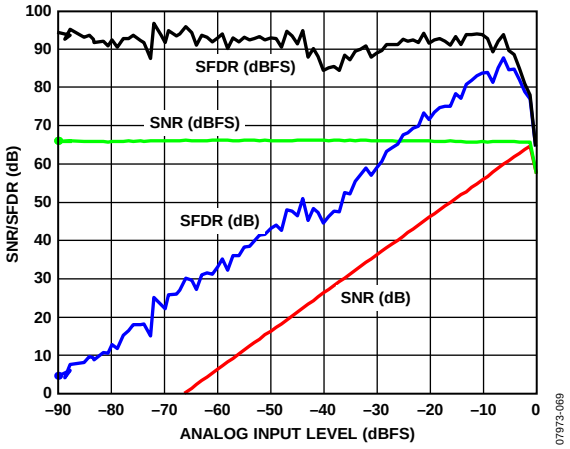


Figure 10. SNR/SFDR vs. Analog Input Level, f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

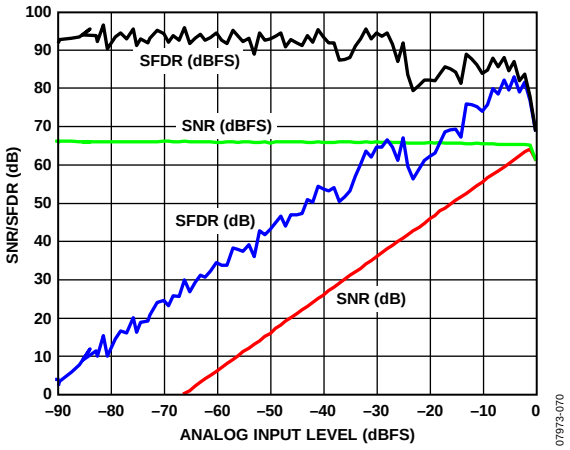


Figure 11. SNR/SFDR vs. Analog Input Level, f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

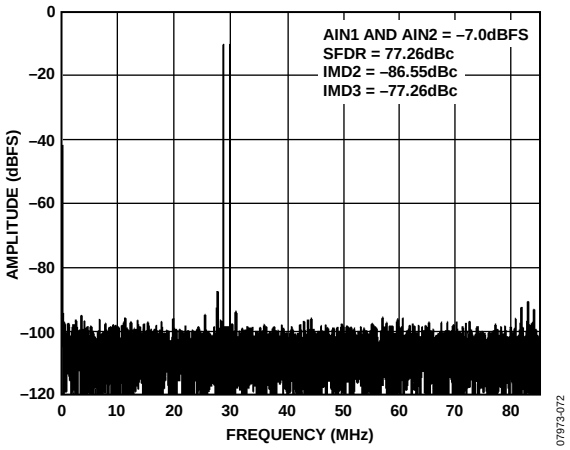


Figure 12. Two-Tone 32k FFT with f_{IN1} = 140.2 MHz and f_{IN2} = 141.3 MHz, f_{SAMPLE} = 170 MSPS

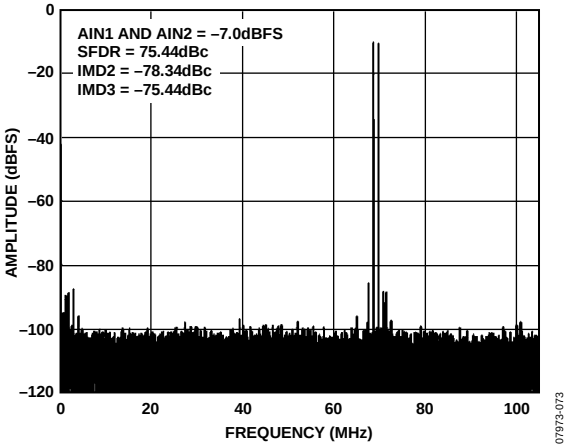


Figure 13. Two-Tone 32k FFT with f_{IN1} = 140.2 MHz and f_{IN2} = 141.3 MHz, f_{SAMPLE} = 210 MSPS

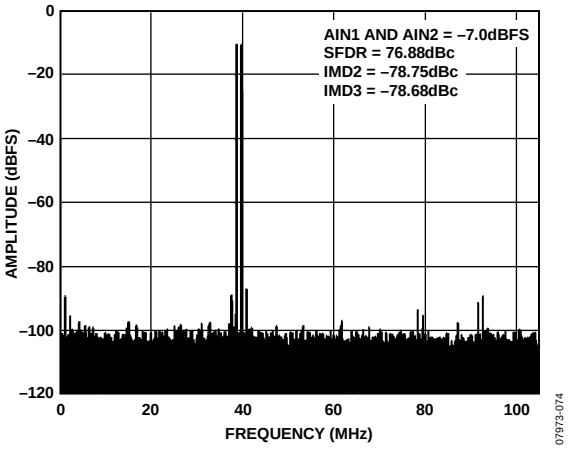


Figure 14. Two-Tone 32k FFT with f_{IN1} = 170.2 MHz and f_{IN2} = 171.3 MHz, f_{SAMPLE} = 210 MSPS

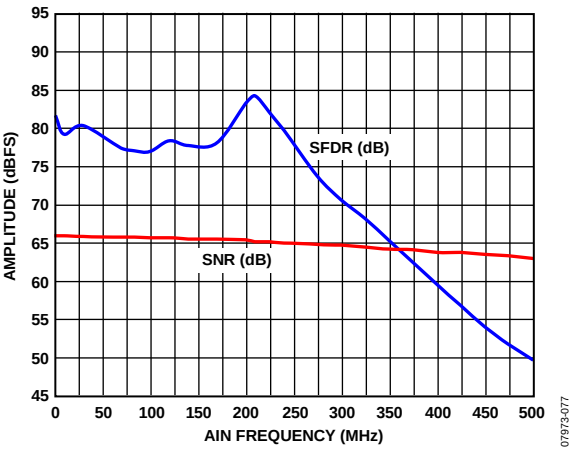


Figure 15. SNR/SFDR Amplitude vs. AIN Frequency, f_{SAMPLE} = 170 MSPS

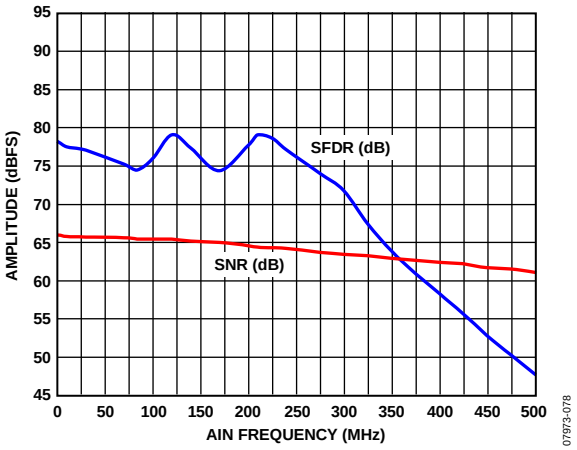


Figure 16. SNR/SFDR Amplitude vs. AIN Frequency, f_{SAMPLE} = 210 MSPS

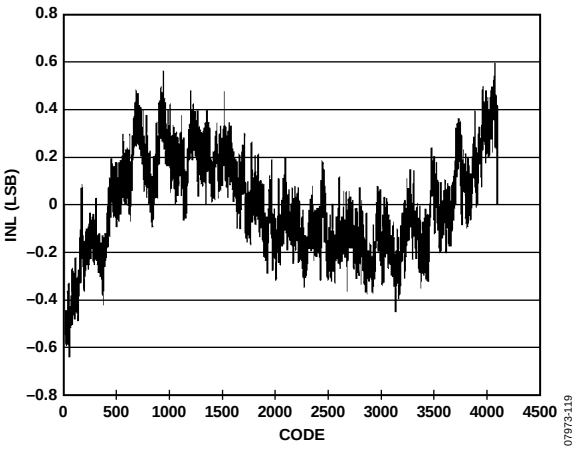


Figure 19. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 210 MSPS

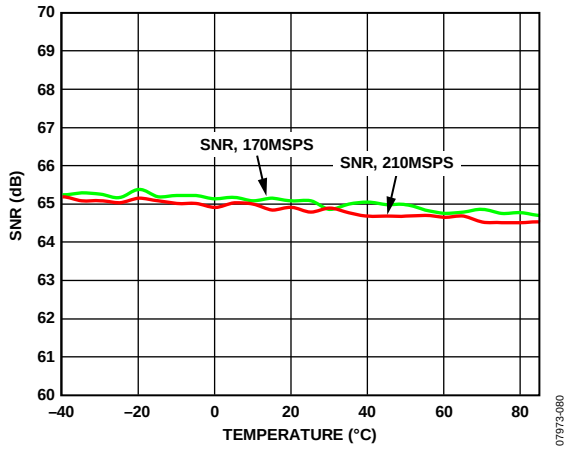


Figure 17. SNR vs. Temperature, f_{IN} = 84.3 MHz

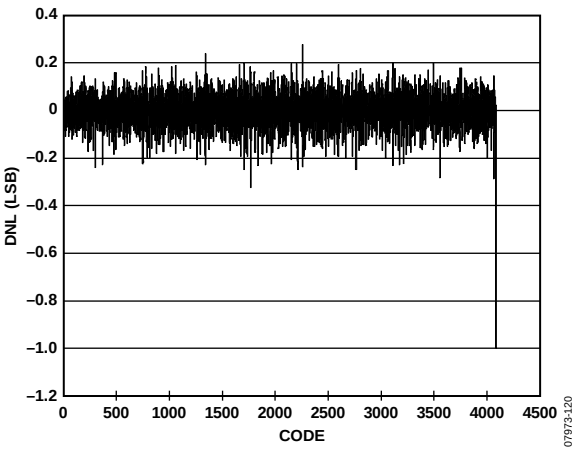


Figure 20. DNL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 210 MSPS

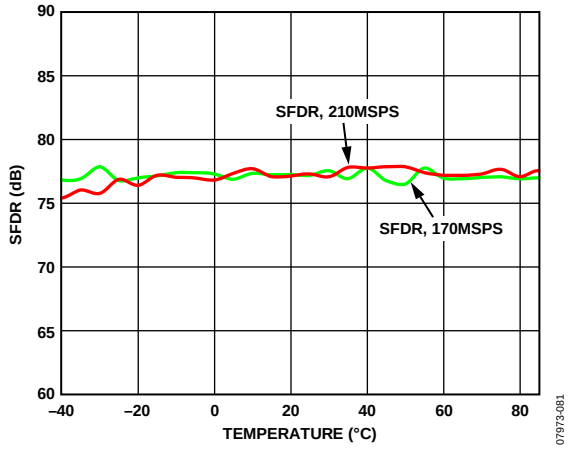


Figure 18. SFDR vs. Temperature, f_{IN} = 84.3 MHz

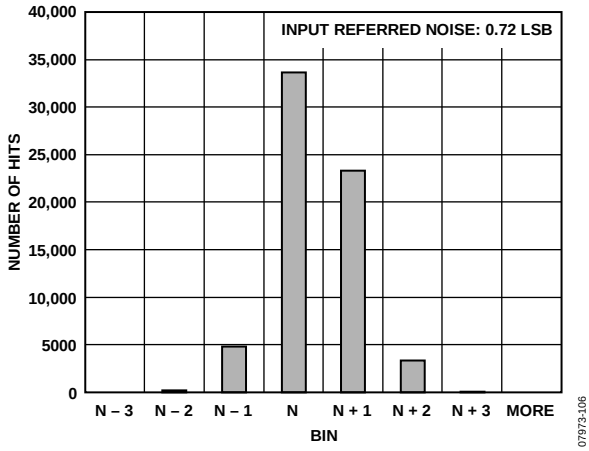


Figure 21. Input-Referred Noise Histogram, f_{SAMPLE} = 170 MSPS

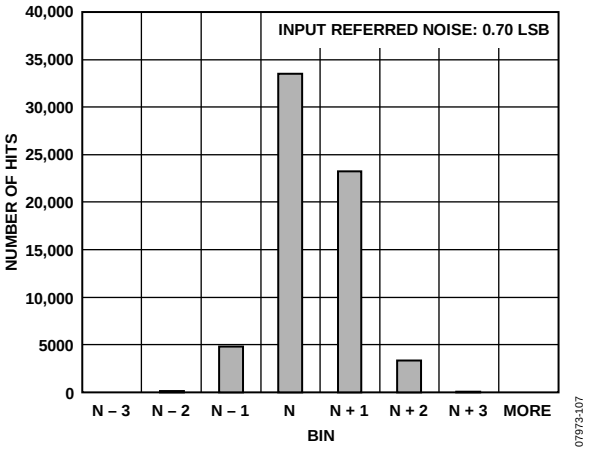


Figure 22. Input-Referred Noise Histogram, f_{SAMPLE} = 210 MSPS

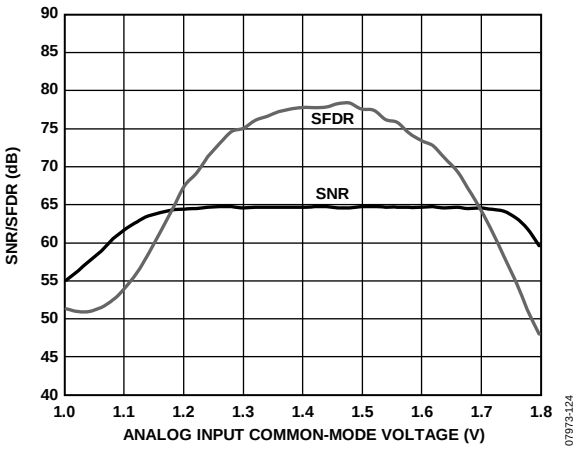


Figure 24. SNR/SFDR vs. Analog Input Common-Mode Voltage, f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

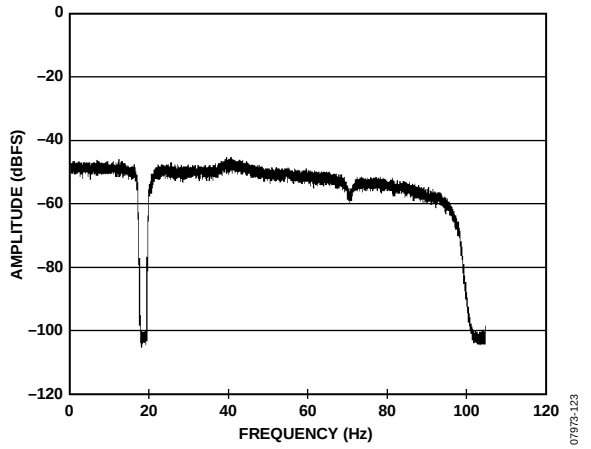


Figure 23. Noise Power Ratio (NPR), f_{SAMPLE} = 210 MSPS

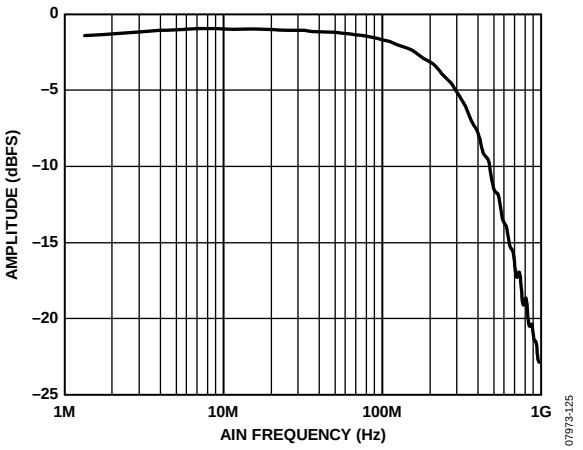


Figure 25. Full-Power Bandwidth Amplitude vs. AIN Frequency, f_{SAMPLE} = 210 MSPS

EQUIVALENT CIRCUITS

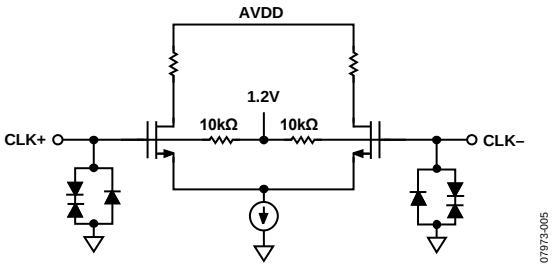


Figure 26. CLK± Inputs

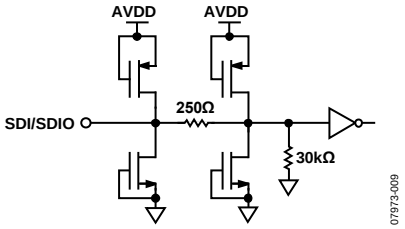


Figure 30. Equivalent SDI/SDIO Input Circuit

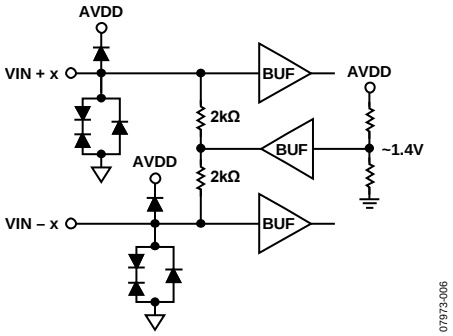


Figure 27. Analog Inputs

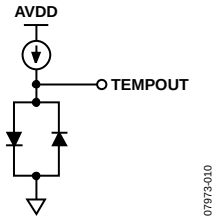


Figure 31. Equivalent TEMPOUT Output Circuit

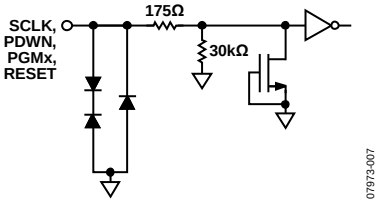


Figure 28. Equivalent SCLK, RESET, PDWN, PGMx Input Circuit

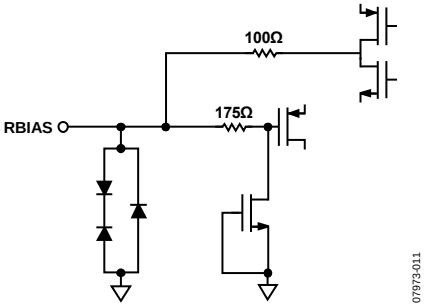


Figure 32. Equivalent RBIAS Input/Output Circuit

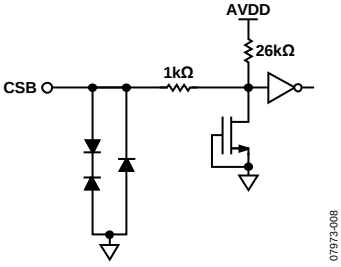


Figure 29. Equivalent CSB Input Circuit

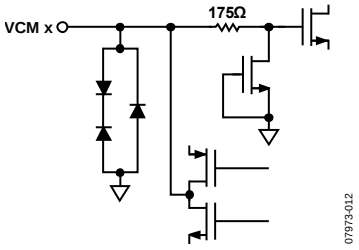


Figure 33. Equivalent VCM x Output Circuit

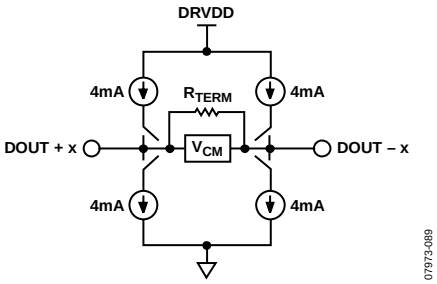


Figure 34. Equivalent Digital Output Circuit

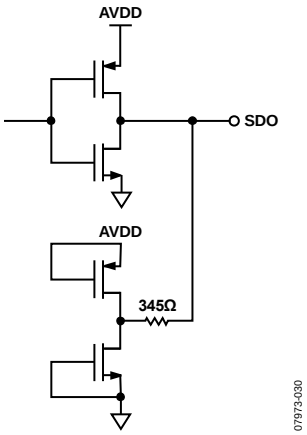


Figure 35. Equivalent SDO Output Circuit

THEORY OF OPERATION

The AD9639 architecture consists of a differential input buffer and a front-end sample-and-hold amplifier (SHA) followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended mode. The output of the pipeline ADC is put into its final serial format by the data serializer, encoder, and CML drivers block. The data rate multiplier creates the clock used to output the high speed serial data at the CML outputs.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9639 is a differential buffer. This input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. SNR and SINAD performance degrades if the analog input is driven with a single-ended signal.

For best dynamic performance, the source impedances driving VIN + x and VIN − x should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. A small resistor in series with each input can help to reduce the peak transient current injected from the output stage of the driving source.

In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. The use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-827 Application Note and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, Number 2, April 2005) for more information on this subject. In general, the precise values depend on the application.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9639, the default input span is 1.25 V p-p. To configure the ADC for a different input span, see the V_{REF} register (Address 0x18). For the best performance, an input span of 1.25 V p-p or greater should be used (see Table 15 for details).

Differential Input Configurations

The AD9639 can be driven actively or passively; in either case, optimum performance is achieved by driving the analog input differentially. For example, using the ADA4937 differential amplifier to drive the AD9639 provides excellent performance and a flexible interface to the ADC for baseband and second Nyquist (~100 MHz IF) applications (see Figure 36 and Figure 37). In either application, use 1% resistors for good gain matching. Note that the dc-coupled configuration shows some degradation in spurious performance. For more information, consult the ADA4937 data sheet.

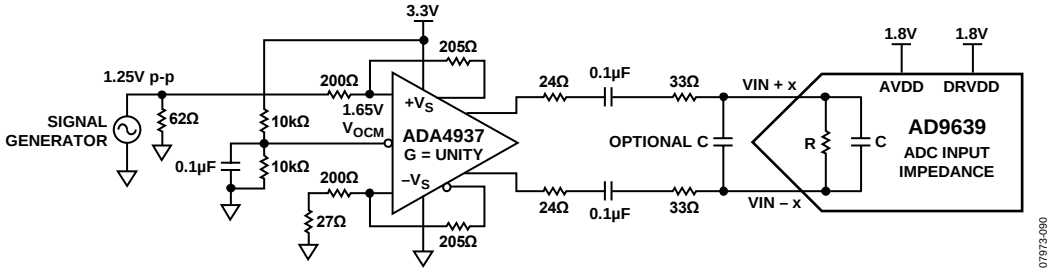


Figure 36. Differential Amplifier Configuration for AC-Coupled Baseband Applications

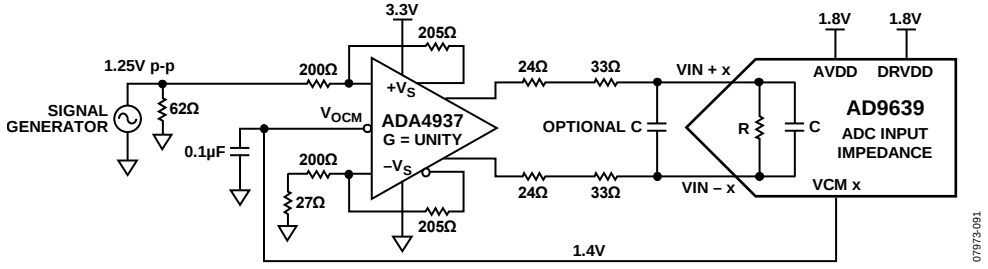


Figure 37. Differential Amplifier Configuration for DC-Coupled Baseband Applications

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration to achieve the true performance of the AD9639 (see Figure 38 to Figure 40).

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

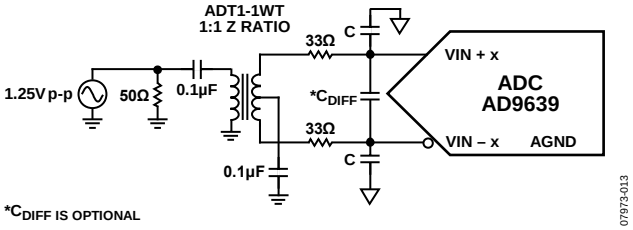


Figure 38. Differential Transformer-Coupled Configuration for Baseband Applications

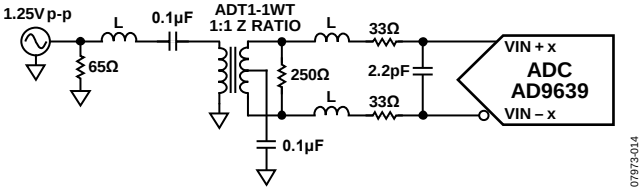


Figure 39. Differential Transformer-Coupled Configuration for Wideband IF Applications

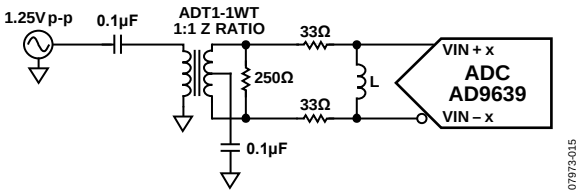


Figure 40. Differential Transformer-Coupled Configuration for Narrow-Band IF Applications

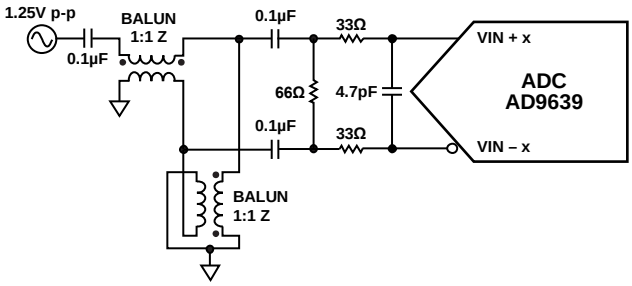


Figure 41. Differential Balun-Coupled Configuration for Wideband IF Applications

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance can degrade due to input common-mode swing mismatch. If the application requires a single-ended input configuration, ensure that the source impedances on each input are well matched to achieve the best possible performance. A full-scale input of 1.25 V p-p can be applied to the VIN + x pin of the AD9639 while the VIN – x pin is terminated. Figure 42 shows a typical single-ended input configuration.

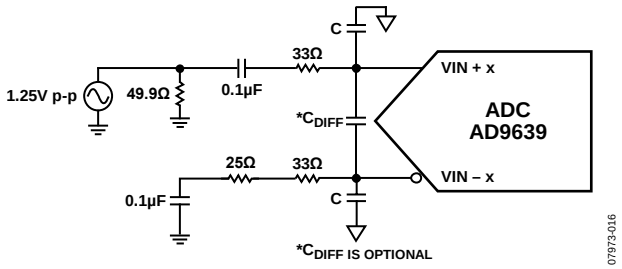


Figure 42. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9639 sample clock inputs (CLK+ and CLK–) should be clocked with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally to 1.2 V and require no additional biasing.

Figure 43 shows a preferred method for clocking the AD9639. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9639 to approximately 0.8 V p-p differential. This helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD9639, and it preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

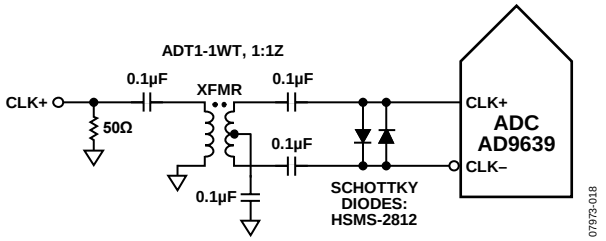


Figure 43. Transformer-Coupled Differential Clock

Another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 44. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9518 family of clock drivers offers excellent jitter performance.

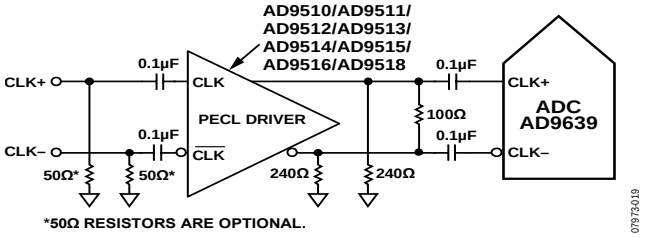


Figure 44. Differential PECL Sample Clock

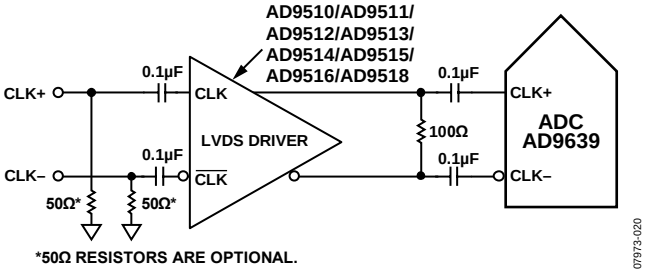


Figure 45. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 46). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages of up to 3.3 V and, therefore, offers several selections for the drive logic voltage.

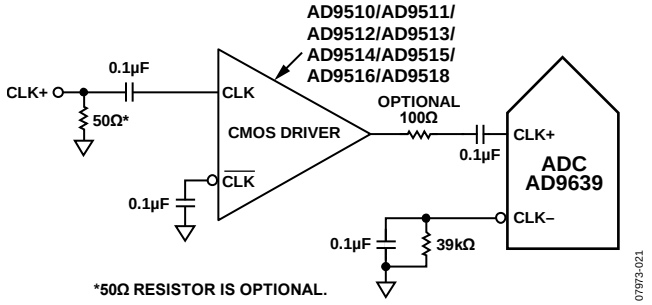


Figure 46. Single-Ended 1.8 V CMOS Sample Clock

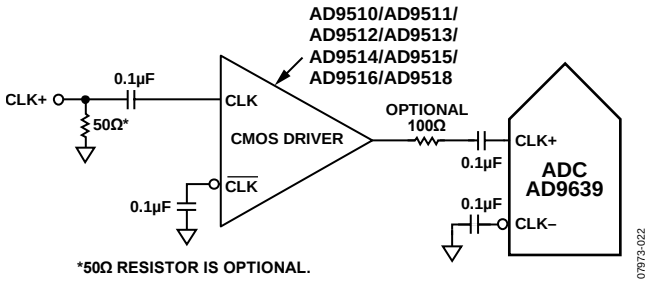


Figure 47. Single-Ended 3.3 V CMOS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9639 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9639. When the DCS is on (default), noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance may be affected when operated in this mode. See the Memory Map section for more details on using this feature.

Jitter in the rising edge of the input is an important concern, and it is not reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 50 MHz nominal. It is not recommended that this ADC clock be dynamic in nature. Moving the clock around dynamically requires long wait times for the back end serial capture to retime and resynchronize to the receiving logic. This long time constant far exceeds the time that it takes for the DCS and the PLL to lock and stabilize. Only in rare applications would it be necessary to disable the DCS circuitry in the clock register (see Address 0x09 in Table 15). Keeping the DCS circuit enabled is recommended to maximize ac performance.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated as follows:

$$SNR\ Degradation = 20 \times \log 10(1/2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 48).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9639. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock during the last step.

Refer to the AN-501 Application Note, the AN-756 Application Note, and the *Analog Dialogue* article, "Analog-to-Digital Converter Clock Optimization: A Test Engineering Perspective" (Volume 42, Number 2, February 2008) for in-depth information about jitter performance as it relates to ADCs (visit www.analog.com).

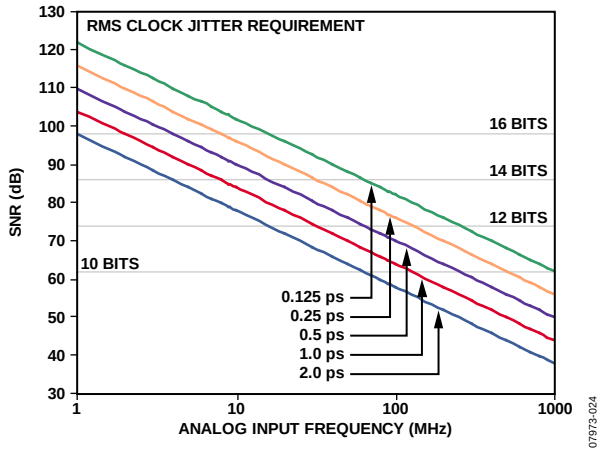


Figure 48. Ideal SNR vs. Input Frequency and Jitter

Power Dissipation

As shown in Figure 49 and Figure 50, the power dissipated by the AD9639 is proportional to its clock rate. The digital power dissipation does not vary significantly because it is determined primarily by the DRVDD supply and the bias current of the digital output drivers.

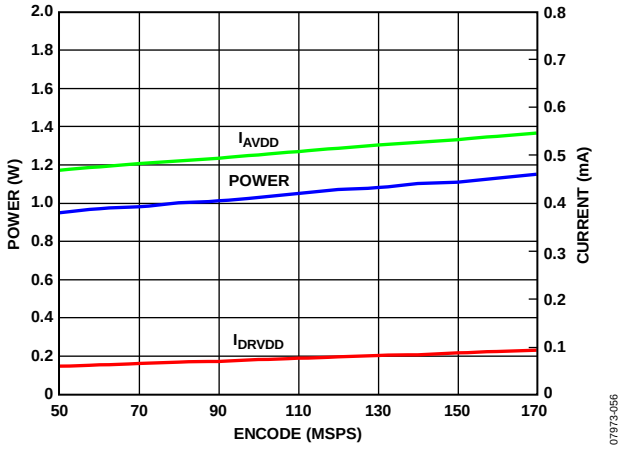


Figure 49. Supply Current vs. Encode for f_{IN} = 84.3 MHz, f_{SAMPLE} = 170 MSPS

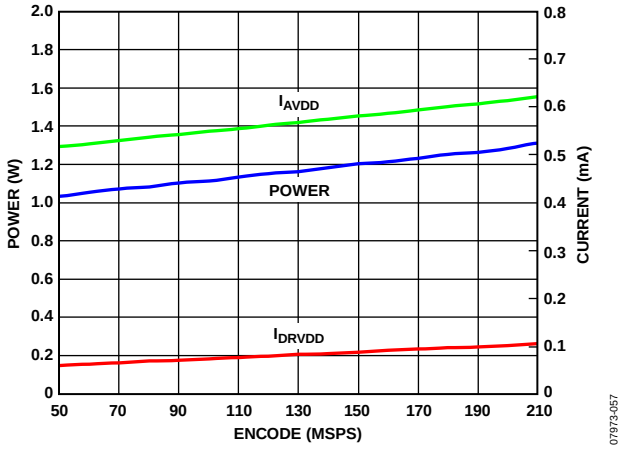


Figure 50. Supply Current vs. Encode for f_{IN} = 84.3 MHz, f_{SAMPLE} = 210 MSPS

DIGITAL OUTPUTS

Serial Data Frame

The AD9639 digital output complies with the JEDEC Standard No. 204 (JESD204), which describes a serial interface for data converters. JESD204 uses 8B/10B encoding as well as optional scrambling. K28.5 and K28.7 comma symbols are used for frame synchronization. The receiver is required to lock onto the serial data stream and recover the clock with the use of a PLL. (Refer to IEEE Std 802.3-2002, Section 3, for a complete 8B/10B and comma symbol description.)

The 8B/10B encoding works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. In the AD9639, the 12-bit converter word is broken into two octets. Bit 11 through Bit 4 are in the first octet. The second octet contains Bit 3 through Bit 0 and four tail bits. The MSB of the tail bits can also be used to indicate an out-of-range condition. The tail bits are configured using the JESD204 register, Address 0x033[3].

The two resulting octets are optionally scrambled and encoded into their corresponding 10-bit code. The scrambling function is controlled by the JESD204 register, Address 0x033[0]. Figure 51 shows how the 12-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and the octets are encoded into two 10-bit symbols. Figure 52 illustrates the data format.

The scrambler uses a self-synchronizing polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver should be a self-synchronizing version of the scrambler polynomial. A 16-bit parallel implementation is shown in Figure 54.

Refer to JEDEC Standard No. 204-April 2006, Section 5.1, for complete transport layer and data format details and Section 5.2 for a complete explanation of scrambling and descrambling.

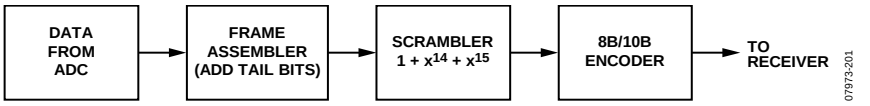


Figure 51. ADC Data Output Path

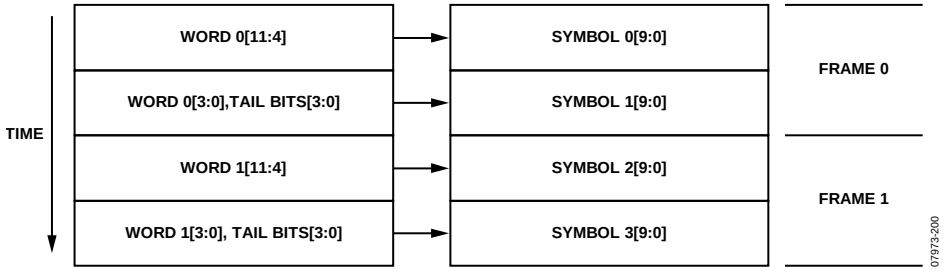


Figure 52. 12-Bit Data Transmission with Tail Bits

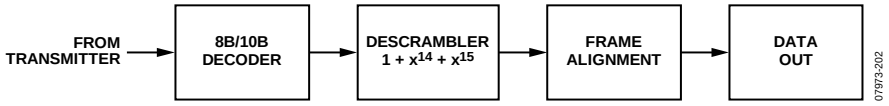


Figure 53. Required Receiver Data Path

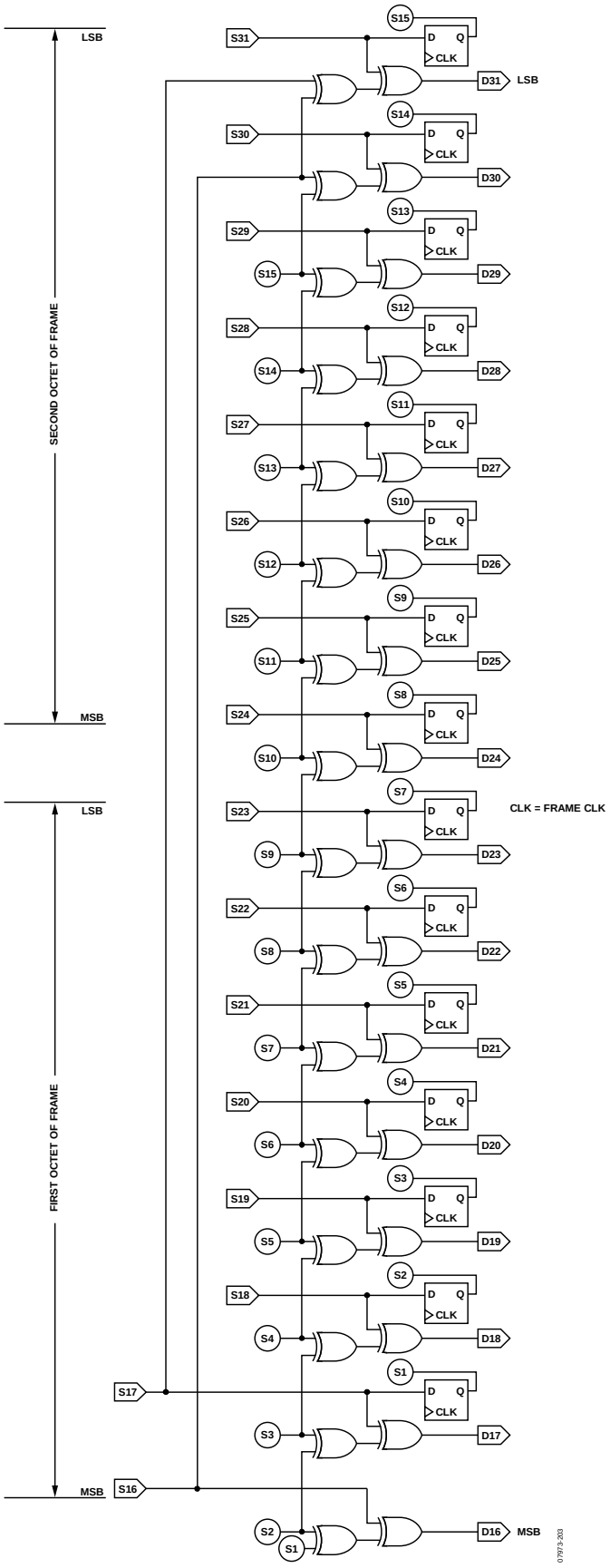


Figure 54. Parallel Descrambler Required in Receiver

Initial Synchronization

The serial interface must synchronize to the frame boundaries before data can be properly decoded. The JESD204 standard has a synchronization routine to identify the frame boundary. The PGMx pins are used as $\overline{\text{SYNC}}$ pins by default. When the $\overline{\text{SYNC}}$ pin is taken low for at least two clock cycles, the AD9639 enters the synchronization mode. The AD9639 transmits the K28.5 comma symbol until the receiver can identify the frame boundary. The receiver should then deassert the sync signal (take $\overline{\text{SYNC}}$ high) and the ADC begins transmitting real data. The first non-K28.5 symbol is the MSB symbol of the 12-bit data.

To minimize skew and time misalignment between each channel of the digital outputs, the following actions should be taken to ensure that each channel data frame is within ±1 clock cycle of the sample clock. For some receiver logic, this is not required.

1. Full power-down through external PDWN pin.
2. Chip reset via external RESET pin.
3. Power-up by releasing external PDWN pin.

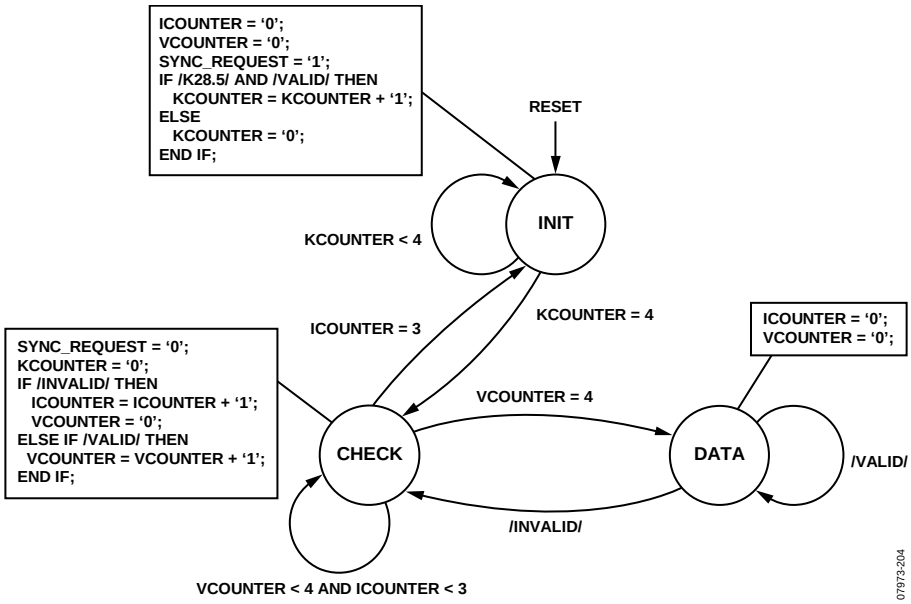


Figure 55. Receiver State Machine

Table 8. Variables Used in Receiver State Machine

Variable	Description
ICOUNTER	Counter used in the CHECK phase to count the number of invalid symbols.
/INVALID/	Asserted by receiver to indicate that the current symbol is an invalid symbol given the current running disparity.
/K28.5/	Asserted when the current symbol corresponds to the K28.5 control character.
KCOUNTER	Counter used in the INIT phase to count the number of valid K28.5 symbols.
SYNC_REQUEST	Asserted by receiver when loss of code group synchronization is detected.
/VALID/	Asserted by receiver to indicate that the current symbol is a valid symbol given the current running disparity.
VCOUNTER	Counter used in the CHECK phase to count the number of successive valid symbols.

Continuous Synchronization

Continuous synchronization is part of the JESD204 specification. The 12-bit word requires two octets to transmit all the data. The two octets (MSB and LSB) are called a frame. When scrambling is disabled and the LSB octets of two consecutive frames are the same, the second LSB octet is replaced by a K28.7 comma symbol. The receiver is responsible for replacing the K28.7 comma symbol with the LSB octet of the previous frame.

When scrambling is enabled, any D28.7 symbols found in the LSB octet of a frame are replaced with K28.7 comma symbols. The receiver is responsible for replacing the K28.7 comma symbols with D28.7 symbols when in this mode.

By looking for K28.7 symbols, the receiver can ensure that it is still synchronized to the frame boundary.

```
IF /K28.7/
   /REPLACE_K28.7/
   IF (OCOUNTER == PREVIOUS_POSITION) AND /VALID/
      /RESET_OCTET_COUNTER/
   END IF;
   IF /VALID/ | (OCOUNTER == N-1)
      PREVIOUS_POSITION = OCOUNTER
   END IF;
END IF;
```

07973-205

Figure 56. Pseudocode for Data Dependent Frame Synchronization in Receiver

Table 9. Variables and Functions in Data Dependent Frame Synchronization

Variable	Description
N	Number of octets in frame (octet indexing starts from 0).
/K28.7/	Asserted when the current symbol corresponds to the K28.7 control character.
OCOUNTER	Counter used to mark the position of the current octet in the frame.
PREVIOUS_POSITION	Variable that stores the position in the frame of a K28.7 symbol.
/REPLACE_K28.7/	Replace K28.7 at the decoder output as follows. When scrambling is disabled, replace K28.7 with the LSB octet that was decoded at the same position in the previous frame; when scrambling is enabled, replace K28.7 at the decoder output with D28.7.
/RESET_OCTET_COUNTER/	Reset octet counter to 0 at reception of next octet.
/VALID/	Asserted by receiver to indicate that the current symbol is a valid symbol given the current running disparity.

Digital Outputs and Timing

The AD9639 has differential digital outputs that power up by default. The driver current is derived on chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

A 100 Ω differential termination resistor should be placed at each receiver input to result in a nominal 400 mV peak-to-peak swing at the receiver. Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

The AD9639 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of DRVDD if dc-coupled connecting is used. For receiver logic that is not within the bounds of the DRVDD supply, an ac-coupled connection should be used. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

If there is no far-end receiver termination or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 6 inches and that the differential output traces be close together and at equal lengths.

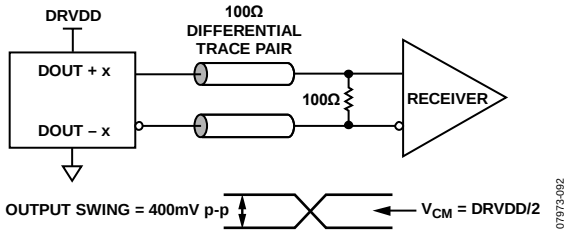


Figure 57. DC-Coupled Digital Output Termination Example

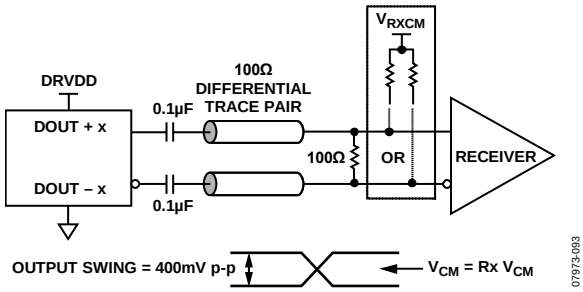


Figure 58. AC-Coupled Digital Output Termination Example

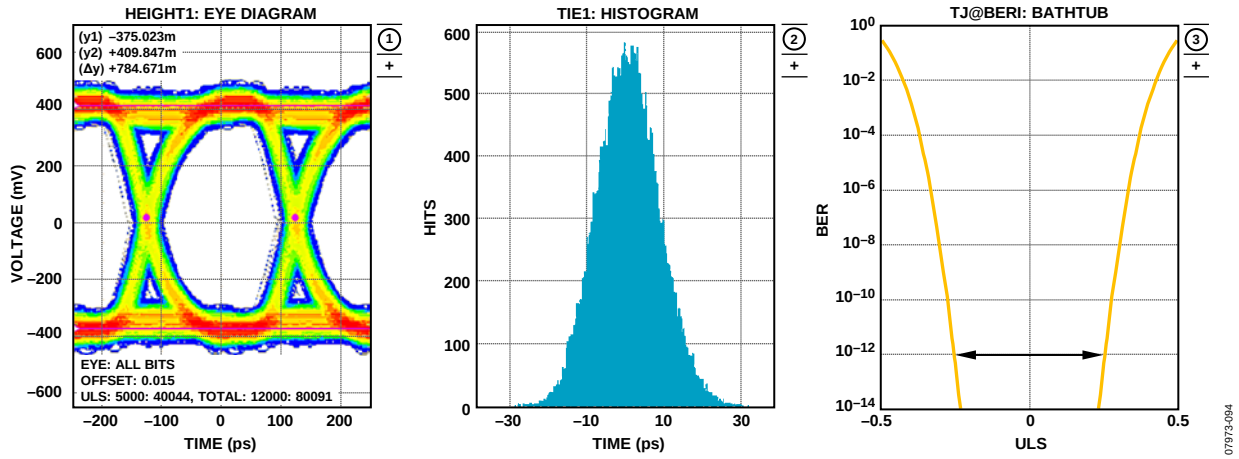


Figure 59. Digital Outputs Data Eye with Trace Lengths Less Than 6 Inches on Standard FR-4, External 100 Ω Terminations at Receiver

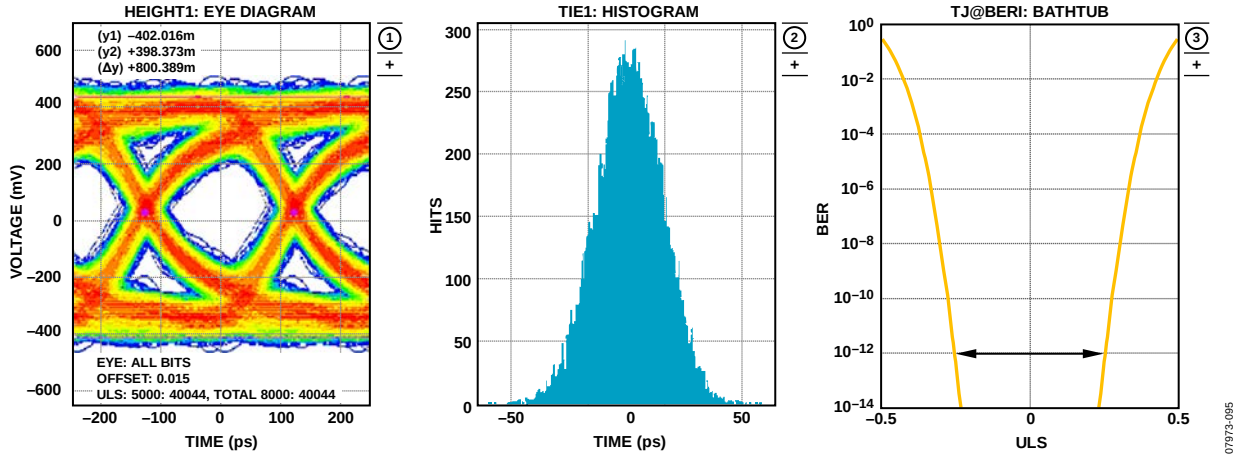


Figure 60. Digital Outputs Data Eye with Trace Lengths Greater Than 12 Inches on Standard FR-4, External 100 Ω Terminations at Receiver

Figure 59 shows an example of the digital output (default) data eye and a time interval error (TIE) jitter histogram with trace lengths less than 6 inches on standard FR-4 material. Figure 60 shows an example of trace lengths exceeding 12 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position. It is the user's responsibility to determine whether the waveforms meet the timing budget of the design when the trace lengths exceed 6 inches.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer trace lengths (see Address 0x15 in Table 15). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is offset binary by default. Table 10 provides an example of this output coding format. To change the output data format to twos complement or gray code, see the Memory Map section (Address 0x14 in Table 15).

Table 10. Digital Output Coding

Code	(VIN + x) – (VIN – x), Input Span = 1.25 V p-p (V)	Digital Output Offset Binary ([D11:D0])
4095	+0.625	1111 1111 1111
2048	0.00	1000 0000 0000
2047	–0.000305	0111 1111 1111
0	–0.625	0000 0000 0000

The lowest typical clock rate is 100 MSPS. For clock rates slower than 100 MSPS, the user can set Bit 3 to 0 in the serial control register (Address 0x21 in Table 15). This option allows the user to adjust the PLL loop bandwidth to use clock rates as low as 50 MSPS.

Setting Bit 2 in the output mode register (Address 0x14) allows the user to invert the digital outputs from their nominal state. This is not to be confused with inverting the serial stream to an LSB first mode. In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. However, this order can be inverted so that the LSB is first in the data output serial stream.

There are eight digital output test pattern options available that can be initiated through the SPI (see Table 12 for the output bit sequencing options). This feature is useful when validating receiver capture and timing. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern selected. Note that some patterns do not adhere to the data format select option.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ (511) bits. A description of the PN sequence short and how it is generated can be found in Section 5.1 of the ITU-T O.150 (05/96) recommendation. The only difference is that the starting value must be a specific value instead of all 1s (see Table 11 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ (8,388,607) bits. A description of the PN sequence long and how it is generated can be found in Section 5.6 of the ITU-T O.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 11 for the initial values) and that the AD9639 inverts the bit stream with relation to the ITU-T standard.

Table 11. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0DF	0xDF9, 0x353, 0x301
PN Sequence Long	0x29B80A	0x591, 0xFD7, 0x0A3

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

Table 12. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	Yes
0001	Midscale short	1000 0000 0000	Same	Yes
0010	+Full-scale short	1111 1111 1111	Same	Yes
0011	−Full-scale short	0000 0000 0000	Same	Yes
0100	Checkerboard	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long[1]	N/A	N/A	Yes
0110	PN sequence short[1]	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No

[1] All test mode options except PN sequence long and PN sequence short can support 8- to 14-bit word lengths to verify data capture to the receiver.

TEMPOUT Pin

The TEMPOUT pin can be used as a coarse temperature sensor to monitor the internal die temperature of the device. This pin typically has a 737 mV output with a clock rate of 210 MSPS and a negative going temperature coefficient of −1.12 mV/°C. The voltage response of this pin is characterized in Figure 61.

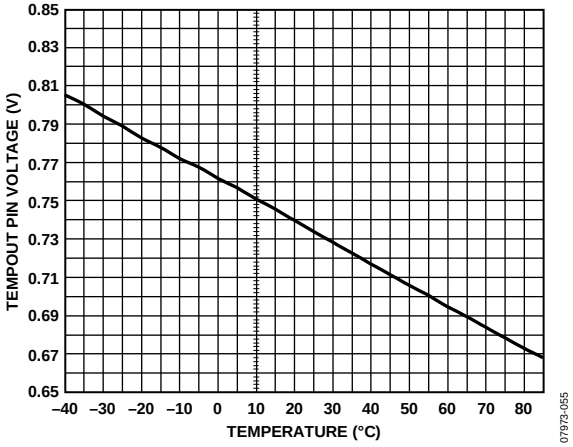


Figure 61. TEMPOUT Pin Voltage vs. Temperature

RBIAS Pin

To set the internal core bias current of the ADC, place a resistor (nominally equal to 10.0 kΩ) between ground and the RBIAS pin. The resistor current is derived on chip and sets the AVDD current of the ADC to a nominal 610 mA at 210 MSPS. Therefore, it is imperative that a 1% or less tolerance on this resistor be used to achieve consistent performance.

VCM x Pins

The common-mode output pins can be enabled through the SPI to provide an external reference bias voltage of 1.4 V for driving the VIN + x/VIN − x analog inputs. The VCM x pins may be required when connecting external devices, such as an amplifier or transformer, to interface to the analog inputs.

RESET Pin

The RESET pin resets the datapath and sets all SPI registers to their default values. To use this pin, the user must resynchronize the digital outputs. This pin is only 1.8 V tolerant.

PDWN Pin

When asserted high, the PDWN pin turns off all ADC channels, including the output drivers. This function can be changed to a standby function (see Address 0x08 in Table 15). This feature allows the user to place all channels into standby mode. The output drivers transmit pseudorandom data until the outputs are disabled using the output mode register (Address 0x14).

When the PDWN pin is asserted high, the AD9639 is placed into power-down mode, shutting down the reference, reference buffer, PLL, and biasing networks. In this state, the ADC typically dissipates 3 mW. If any of the SPI features are changed before the power-down feature is enabled, the chip continues to function after PDWN is pulled low without requiring a reset. The AD9639 returns to normal operating mode when the PDWN pin is pulled low. This pin is only 1.8 V tolerant.

SDO Pin

The SDO pin is for use in applications that require a 4-wire SPI mode operation. For normal operation, it should be tied low to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 345 Ω internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant.

SDI/SDIO Pin

The SDI/SDIO pin is for use in applications that require either a 4- or 3-wire SPI mode operation. For normal operation, it should be tied low to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant.

SCLK Pin

For normal operation, the SCLK pin should be tied to AGND through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 30 kΩ internal pull-down resistor pulls this pin low. This pin is only 1.8 V tolerant.

CSB Pin

For normal operation, the CSB pin should be tied high to AVDD through a 10 kΩ resistor. Alternatively, the device pin can be left open, and the 26 kΩ internal pull-up resistor pulls this pin high. Tying the CSB pin to AVDD causes all information on the SCLK and SDI/SDIO pins to be ignored. Tying the CSB pin low causes all information on the SDO and SDI/SDIO pins to be written to the device. This feature allows the user to reduce the number of traces to the device if necessary. This pin is only 1.8 V tolerant.

PGMx Pins

All PGMx pins are automatically initialized as synchronization pins by default. These pins are used to lock the FPGA timing and data capture during initial startup. These pins are respective to each channel (PGM3 = Channel A, PGM2 = Channel B, and so on). The sync (PGMx) pin should be pulled high until this pin receives a low signal input from the receiver, during which time the ADC outputs K28.5 comma symbols to indicate the frame boundary. When the receiver finds the frame boundary, the sync identification is deasserted low and the ADC outputs the valid data on the next packet boundary.

When steady state operation for the device is achieved, these pins can be assigned as a standby option using the PGM mode register (Address 0x53 in Table 15). All other PGMx pins become global synchronization pins. This pin is only 1.8 V tolerant.

SERIAL PORT INTERFACE (SPI)

The AD9639 serial port interface allows the user to configure the converter for specific functions or operations through a structured register space provided in the ADC. The SPI can provide the user with additional flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the Analog Devices, Inc., AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Four pins define the SPI: SCLK, SDI/SDIO, SDO, and CSB (see Table 13). The SCLK pin is used to synchronize the read and write data presented to the ADC. The SDI/SDIO pin is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The SDO pin is used in 4-wire mode to read back data from the part. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 13. Serial Port Pins

Pin	Function
SCLK	Serial clock. Serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDI/SDIO	Serial data input/output. Dual-purpose pin that typically serves as an input or an output, depending on the SPI wire mode, the instruction sent, and the relative position in the timing frame.
SDO	Serial data output. Used only in 4-wire SPI mode. When set, the SDO pin becomes active. When cleared, the SDO pin remains in three-state and all read data is routed to the SDI/SDIO pin.
CSB	Chip select bar (active low). This control gates the read and write cycles.

The falling edge of CSB in conjunction with the rising edge of SCLK determines the start of the framing sequence. During the instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. An example of the serial timing and its definitions can be found in Figure 63 and Table 14.

During normal operation, CSB is used to signal to the device that SPI commands are to be received and processed. When CSB is brought low, the device processes SCLK and SDI/SDIO to execute instructions. Normally, CSB remains low until the communication cycle is complete. However, if connected to a slow device, CSB can be brought high between bytes, allowing older microcontrollers enough time to transfer data into shift registers. CSB can be stalled when transferring one, two, or three bytes of data. When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until CSB is taken high to end the communication cycle. This allows complete memory transfers without requiring additional instructions. Regardless of the mode, if CSB is taken high in the middle of a byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port configuration influences how the AD9639 operates. For applications that do not require a control port, the CSB line can be tied high. This places the SDI/SDIO pin into its secondary mode, as defined in the SDI/SDIO Pin section. CSB can also be tied low to enable 2-wire mode. When CSB is tied low, SCLK and SDI/SDIO are the only pins required for communication. Although the device is synchronized during power-up, the user should ensure that the serial port remains synchronized with the CSB line when using this mode. When operating in 2-wire mode, it is recommended that a 1-, 2-, or 3-byte transfer be used exclusively. Without an active CSB line, streaming mode can be entered but not exited.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used to both program the chip and read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDI/SDIO pin to change from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first or LSB first mode. MSB first mode is the default at power-up and can be changed by adjusting the configuration register (Address 0x00). For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 13 constitute the physical interface between the user's programming device and the serial port of the AD9639. The SCLK and CSB pins function as inputs when using the SPI. The SDI/SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

If multiple SDI/SDIO pins share a common connection, ensure that proper V_{OH} levels are met. Assuming the same load for each AD9639, Figure 62 shows the number of SDI/SDIO pins that can be connected together and the resulting V_{OH} level. This interface is flexible enough to be controlled by either serial PROMs or PIC microcontrollers, providing the user with an alternative method, other than a full SPI controller, to program the ADC (see the AN-812 Application Note).

For users who wish to operate the ADC without using the SPI, remove any connections from the CSB, SCLK, SDO, and SDI/SDIO pins. By disconnecting these pins from the control bus, the ADC can function in its most basic operation. Each of these pins has an internal termination that floats to its respective level.

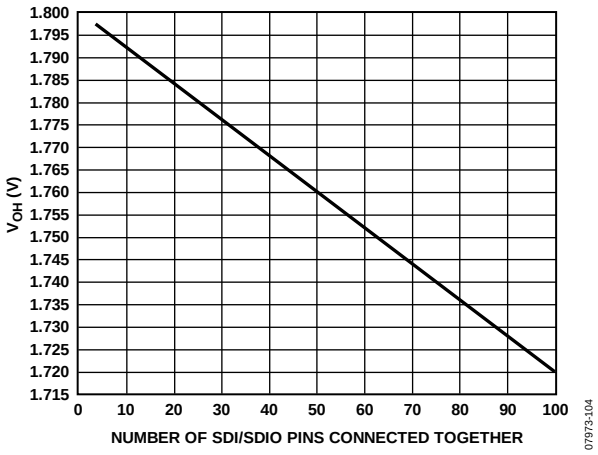


Figure 62. SDI/SDIO Pin Loading

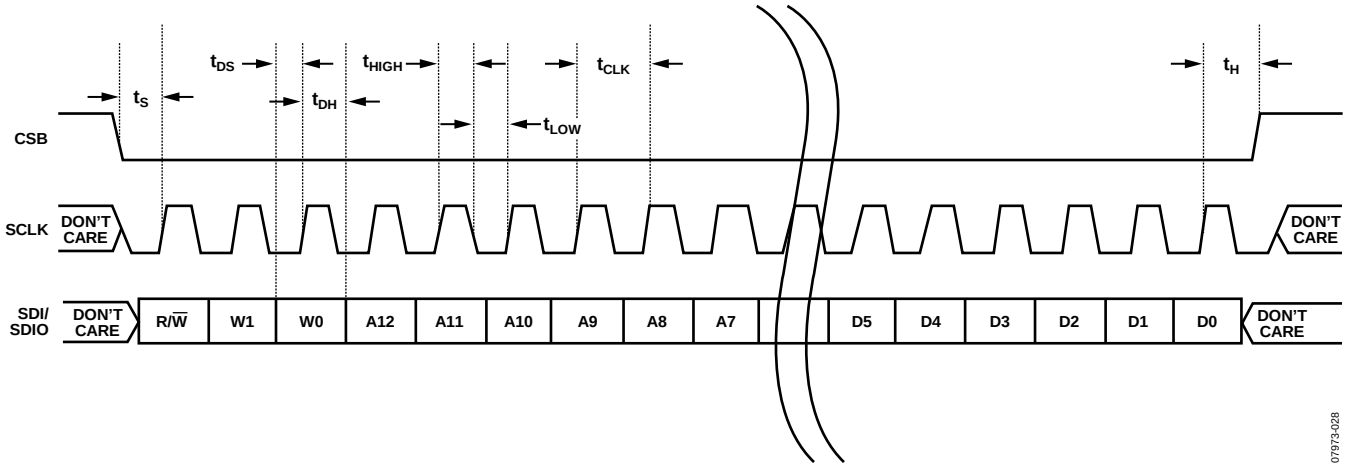


Figure 63. Serial Timing Details

Table 14. Serial Timing Definitions

Parameter	Timing (ns min)	Description
t_{DS}	5	Setup time between the data and the rising edge of SCLK
t_{DH}	2	Hold time between the data and the rising edge of SCLK
t_{CLK}	40	Period of the clock
t_S	5	Setup time between CSB and SCLK
t_H	2	Hold time between CSB and SCLK
t_{HIGH}	16	Minimum period that SCLK should be in a logic high state
t_{LOW}	16	Minimum period that SCLK should be in a logic low state
$t_{EN_SDI/SDIO}$	10	Minimum time for the SDI/SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 63)
$t_{DIS_SDI/SDIO}$	10	Minimum time for the SDI/SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 63)

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map register table (Table 15) has eight bit locations. The memory map is divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02), the device index and transfer registers (Address 0x05 and Address 0xFF), and the ADC function registers (Address 0x08 to Address 0x53).

The leftmost column of the memory map indicates the register address; the default value is shown in the second rightmost column. The Bit 7 column is the start of the default hexadecimal value given. For example, Address 0x09, the clock register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address, followed by 0x01 in the device update register (Address 0xFF[0], the transfer bit), the duty cycle stabilizer is turned off. It is important to follow each write sequence with a transfer bit to update the SPI registers. For more information about this and other functions, consult the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

RESERVED LOCATIONS

Undefined memory locations should not be written to except when writing the default values suggested in this data sheet. Blank cells in Table 15 should be considered reserved bits and have a 0 written into their registers during power-up.

DEFAULT VALUES

When the AD9639 comes out of a reset, critical registers are preloaded with default values. These values are indicated in Table 15.

LOGIC LEVELS

In Table 15, "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "bit is cleared" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Table 15. Memory Map Register

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	chip_port_ config (local, master)	SDO active (not required, ignored if not used)	LSB first	Soft reset	16-bit address (default mode for ADCs)					0x18	
0x01	chip_id (global)	8-bit chip ID, Bits[2:0] 0x29: AD9639, 12-bit quad									Read only.
0x02	chip_grade (global)		Speed grade 010 = 170 MSPS 100 = 210 MSPS								Read only.
Device Index and Transfer Registers											
0x05	device_ index_A (global)					ADC A	ADC B	ADC C	ADC D	0x0F	Bits are set to determine which device on chip receives the next write command. The default is all devices on chip.
0xFF	device_ update (local, master)								SW transfer 1 = on 0 = off (default)	0x00	Synchro-nously transfers data from the master shift register to the slave.
ADC Function Registers											
0x08	Modes (local)		External PDWN pin function 00 = full power-down (default) 01 = standby					Power-down mode 00 = chip run (default) 01 = full power-down 10 = standby 11 = reset		0x00	Determines generic modes of chip operation.
0x09	Clock (global)								Duty cycle stabilize 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off.
0x0D	test_io (local)			Reset PN sequence long gen 1 = on 0 = off (default)	Reset PN sequence short gen 1 = on 0 = off (default)	Flexible output test mode 0000 = off (normal operation) 0001 = midscale short 0010 = +FS short 0011 = –FS short 0100 = checkerboard output 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = 1/0 word toggle				0x00	When set, the test data is placed on the output pins in place of normal data.
0x0E	test_bist (local)						BIST init 1 = on 0 = off (default)		BIST enable 1 = on 0 = off (default)	0x00	When Bit 0 is set, the built-in self-test function is initiated.
0x0F	adc_input (local)						Analog disconnect enable 1 = on 0 = off (default)	VCM enable 1 = on 0 = off (default)		0x00	

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Comments
0x10	Offset (local)	6-bit device offset adjustment[5:0] 011111 = +31 LSB 011110 = +30 LSB 011101 = +29 LSB … 000010 = +2 LSB 000001 = +1 LSB 000000 = 0 LSB 111111 = −1 LSB 111110 = −2 LSB 111101 = −3 LSB … 100001 = −31 LSB 100000 = −32 LSB								0x00	Device offset trim.
0x14	output_mode (local/global)				Output enable bar (local) 1 = off 0 = on (default)		Output invert enable (global) 1 = on 0 = off (default)	Data format select (global) 00 = offset binary (default) 01 = twos complement 10 = gray code		0x00	Configures the outputs and the format of the data.
0x15	output_adjust (global)							Output driver current[1:0] 00 = 400 mV (default) 01 = 500 mV 10 = 440 mV 11 = 320 mV		0x00	VCM output adjustments.
0x18	V_{REF} (global)	Ref_Vfs[4:0] Reference full-scale adjust 10000 = 0.98 V p-p 10001 = 1.00 V p-p 10010 = 1.02 V p-p 10011 = 1.04 V p-p … 11111 = 1.23 V p-p 00000 = 1.25 V p-p 00001 = 1.27 V p-p … 01110 = 1.48 V p-p 01111 = 1.5 V p-p								0x00	Select adjustments for V_{REF}.
0x21	serial_control (global)					PLL high encode rate mode (global) 0 = low rate 1 = high rate (default)				0x08	Serial stream control.
0x24	misr_lsb (local)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	Least significant byte of MISR. Read only.
0x25	misr_msb (local)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	Most significant byte of MISR. Read only.

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)	Comments
0x33	JESD204 (global)					Over-range in LSB of tail bits 0 = over-range disabled (default) 1 = over-range enabled			Scram-bling enable 0 = scram-bling disabled (default) 1 = scram-bling enabled	0x00	
0x53	Dynamic pgm pins (global)	pgm_3 00 = sync 01 = Standby A 10 = Standby A and Standby D 11 = Standby A and Standby B		pgm_2 00 = sync 01 = Standby B 10 = Standby B and Standby C 11 = Standby B and Standby A		pgm_1 00 = sync 01 = Standby C 10 = Standby C and Standby B 11 = Standby C and Standby D		pgm_0 00 = sync 01 = Standby D 10 = Standby D and Standby A 11 = Standby D and Standby C		0x00	Standby = ADC core off, PN23 enabled, serial channel enabled.

APPLICATIONS INFORMATION

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9639, it is recommended that two separate 1.8 V supplies be used: one for analog (AVDD) and one for digital (DRVDD). If only one supply is available, it should be routed to the AVDD pin first and then tapped off and isolated with a ferrite bead or a filter choke preceded by decoupling capacitors for the DRVDD pin. Several different decoupling capacitors can be used to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the parts, with minimal trace lengths.

A single PCB ground plane should be sufficient when using the AD9639. With proper decoupling and smart partitioning of the analog, digital, and clock sections of the PCB, optimum performance can easily be achieved.

EXPOSED PADDLE THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9639. An exposed continuous copper plane on the PCB should mate to the AD9639 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane into several uniform sections by overlaying a silkscreen on the PCB. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions guarantees only one tie point. See Figure 64 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

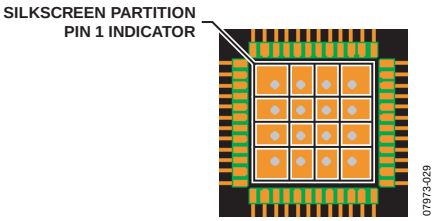
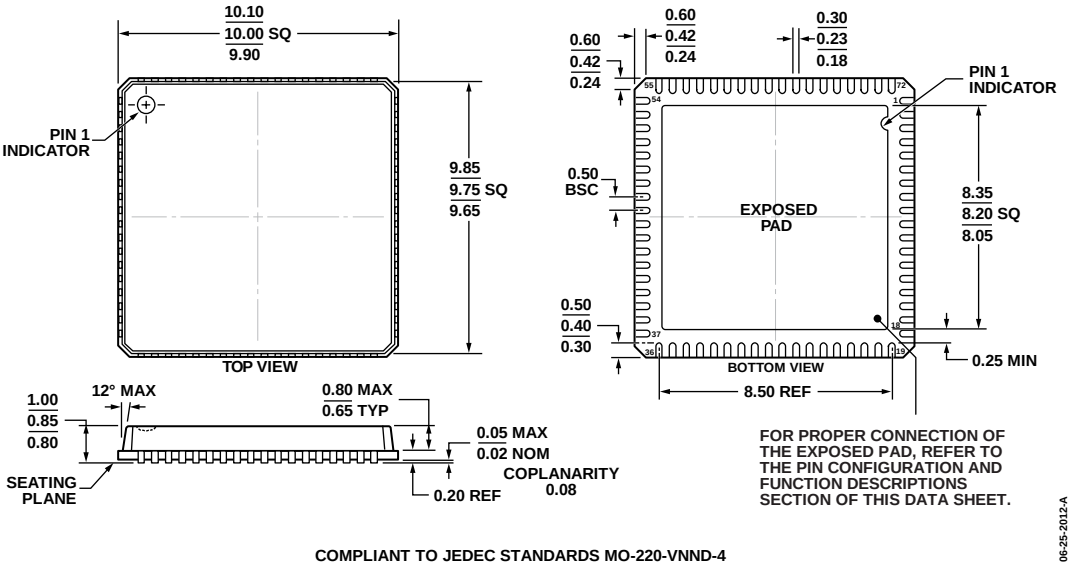


Figure 64. Typical PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 65. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9639BCPZ-170	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9639BCPZRL-170	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9639BCPZ-210	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9639BCPZRL-210	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-3
AD9639-210KITZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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