BridgeSwitch Family

High-Voltage, Self-Powered, Half-bridge Motor Driver with Integrated Device Protection and System Monitoring

Product Highlights

Highest Performance and Design Flexibility

- Fully integrated half-bridge stage with up to 98% efficiency
  - Eliminates external heat sink at rated continuous RMS current
- 600 V N-channel power FREDFETs
  - Ultra-soft, fast recovery diode
- Accurate instantaneous phase current information output (BRD126X)
  - Eliminates external sensing and amplification circuitry
- Self-biased low-side and high-side drivers
  - Eliminates need for auxiliary power supply
- Small footprint surface mount inSOP-24C package
  - Exposed pads enable heat sinking through PCB
- Controlled FREDFET switching speed reduces EMI

Enhanced Safety and Reliability Features

- Adustable cycle-by-cycle current limit for both FREDFETs
  - Fail-safe operation
- Internal dual level thermal overload protection
- Self-configuring system level monitoring input
  - Four level DC bus undervoltage
  - DC bus overvoltage
  - System temperature
- Adaptive dead time
- Simultaneous conduction lockout protection

Status Interface

- Bi-directional bussed open Drain single wire interface
- Reports status updates to system MCU
  - Successful power-up
  - Internal over-current or temperature faults
  - System level faults
  - Includes device identification
- Status query through system MCU
- Device fault reset through system MCU

Applications

- 2- or 3-phase high-voltage PM and BLDC motor drives
  - Up to 300 W typical inverter output power
- Appliances including dish washers and refrigerators
- Condenser fans in high efficiency air conditioners

Description

The BridgeSwitch™ family of integrated half-bridges dramatically simplifies the development and production of high-voltage inverter driven 2- or 3-phase PM or BLDC motor drives. It incorporates two high-voltage N-channel power FREDFETs with low and high-side drivers in a single small-outline package. The internal power FREDFETs offer ultra-soft and ultrafast diodes ideally suited for hard switched inverter drives. Both drivers are self-supplied eliminating the need for an external auxiliary power supply. BridgeSwitch provides a unique instantaneous phase current output signal simplifying implementation of sensor-less control schemes. The low-profile, compact footprint surface mount package offers extended creepage distances and allows heat sinking of both power FREDFETs through the printed circuit board.

BridgeSwitch offers internal fault protection functions and external system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two level thermal overload protection. External system level monitoring includes DC bus sensing with four undervoltage levels and one overvoltage level as well as driving external sensors such as an NTC. The bi-directional bussed single wire status interface reports observed status changes.

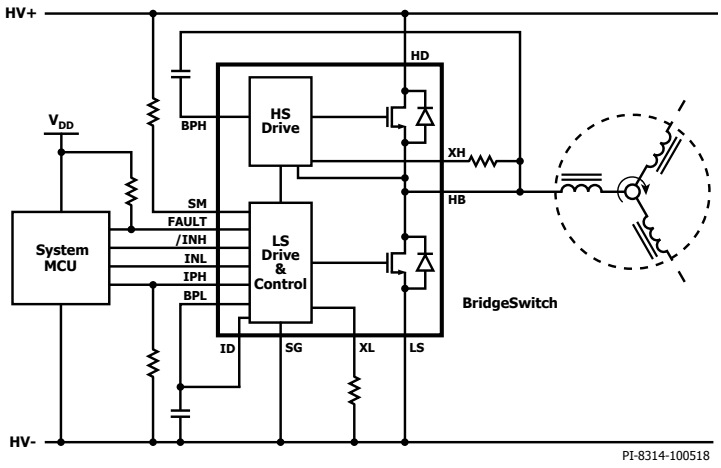


Figure 1. Typical 3-Phase Inverter Schematic (BRD126X).

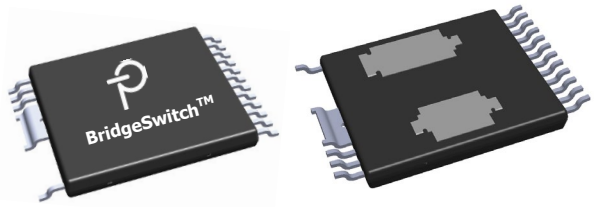


Figure 2. InSOP-24C Package (Top and Bottom Sides).

Product Family

Product[3]	DC Output Current[1]	Continuous RMS Current[2]
BRD1160C / BRD1260C	1.0 A	0.22 A
BRD1161C / BRD1261C	1.7 A	0.50 A
BRD1163C / BRD1263C	3.0 A	0.75 A
BRD1165C / BRD1265C	5.5 A	1.00 A

Table 1. Product Family.

Notes:
1. Continuous DC output current per FREDFET, calculated at 25 °C case and 125 °C junction temperature. Normally limited by internal circuitry
2. Continuous phase RMS current, internal self-supply, 340 V bus, trapezoidal commutation with 12 kHz high-side PWM, PCB heat sinking with 50 °C case temperature rise.
3. Package: InSOP-24C.

This Product is Covered by Patents and/or Pending Patent Applications.

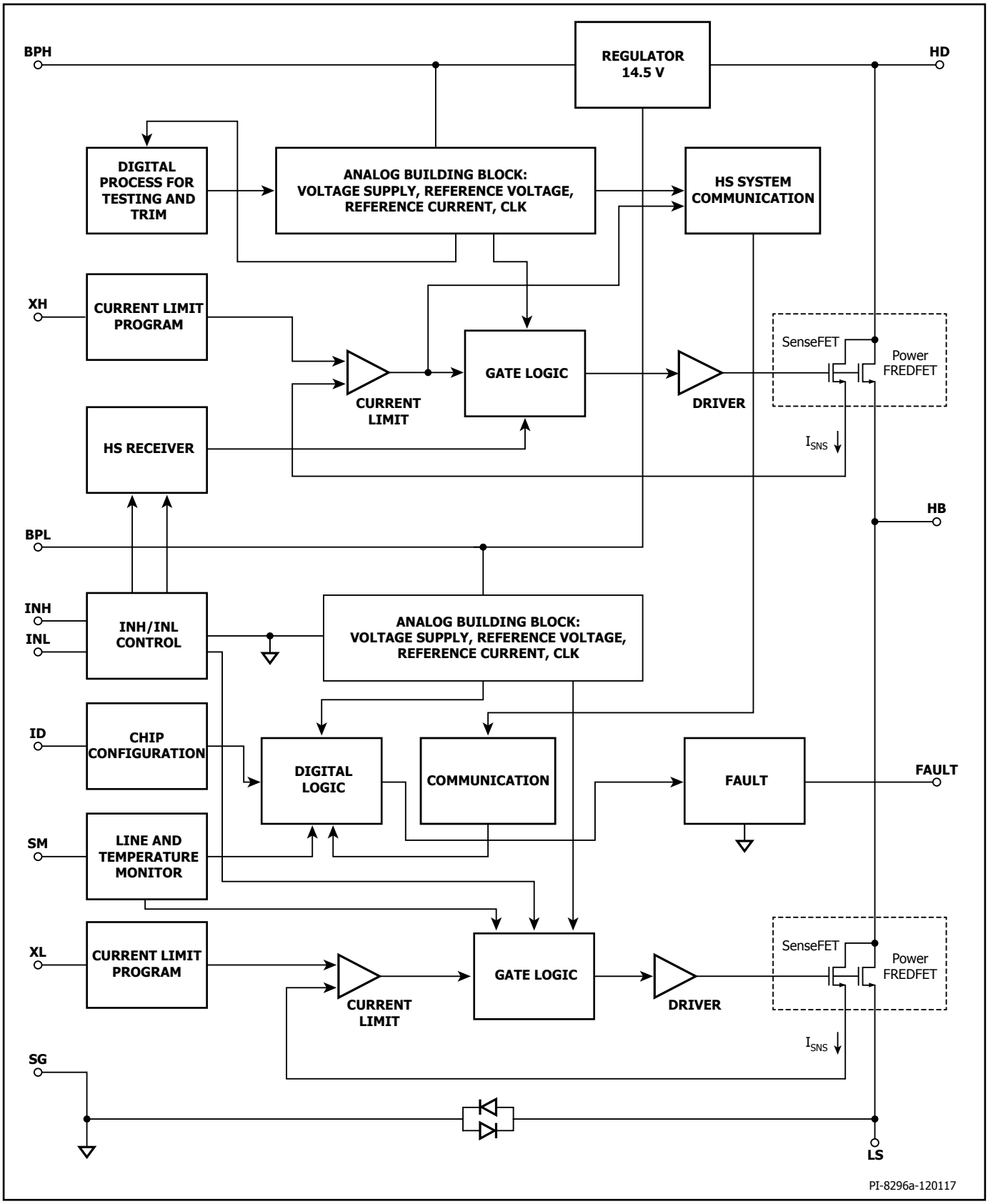


Figure 3. Functional Block Diagram BRD116X.

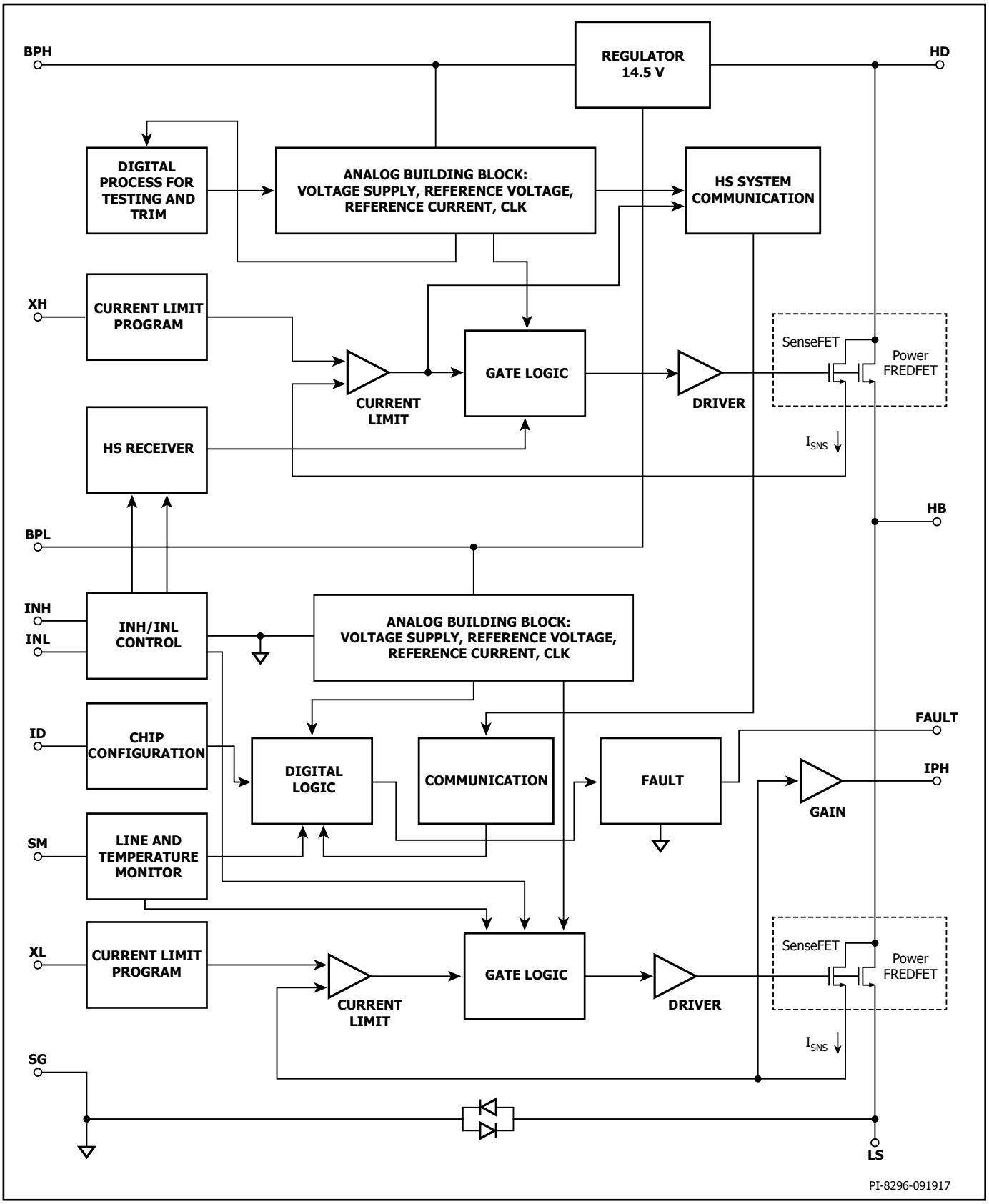


Figure 4. Functional Block Diagram BRD126X.

Pin Functional Description

HIGH-SIDE DRAIN (HD) Exposed Pad
The HD exposed pad is the electrical connection to the high-side power FREDFET Drain connection. It is also the input for the internal low-side and high-side self-supply circuitry.

EXTERNAL CURRENT LIMIT LOW-SIDE (XL) Pin (Pin 1)
This pin connects to a resistor to set the cycle-by-cycle current limit for the low-side power FREDFET.

PHASE CURRENT OUTPUT (IPH) Pin (Pin 2, BRD126X)
This pin connects to a small signal resistor and provides low-side FREDFET Drain current information. The pin should be left floating if the function is not used. Function is not available with BRD116X.

SIGNAL GROUND (SG) Pin (Pins 3 and 10)
These pins are the ground reference connection for low-side controller small signal pins and the system micro-controller.

BYPASS LOW-SIDE (BPL) Pin (Pin 4)
This pin connects to the external bypass capacitor for the low-side controller and FREDFET Gate driver.

CONTROL INPUT LOW-SIDE (INL) Pin (Pin 5)
Active high logic level control input for the low-side power FREDFET.

CONTROL INPUT HIGH-SIDE (/INH) Pin (Pin 6)
Active low logic level control input for the high-side power FREDFET.

STATUS COMMUNICATION (FAULT) Pin (Pin 7)
This open Drain pin connects to an I/O port of the system micro-controller to provide a status update. The pin should be connected to SIGNAL GROUND if the function is not used.

SYSTEM MONITOR (SM) Pin (Pin 8)
This pin is a self-configuring system monitor input. It configures itself into a high-voltage bus sense input if a resistor is connected to the high-voltage bus at power-up. It configures itself into an external temperature sense input if a resistance is connected to SYSTEM GROUND at power-up. The pin should be connected to SIGNAL GROUND if the function is not used.

DEVICE ID (ID) Pin (11)
This pin programs the device ID at power-up.

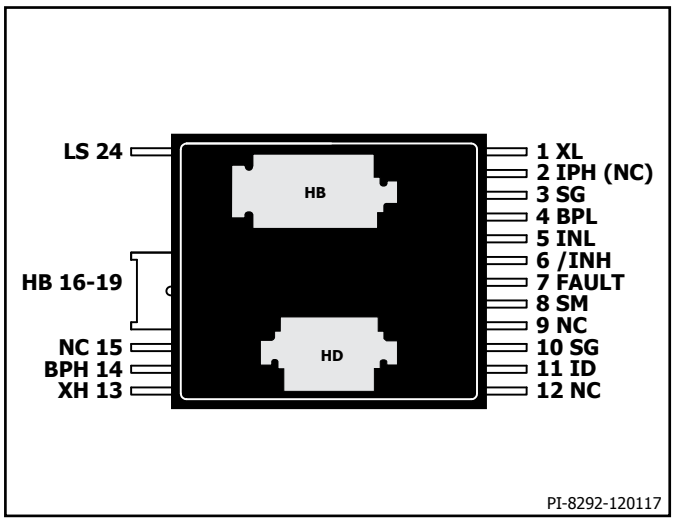


Figure 5. Pin Configuration (Bottom View).

EXTERNAL CURRENT LIMIT HIGH-SIDE (XH) Pin (Pin 13)
This pin connects to a resistor to set the cycle-by-cycle current limit for the high-side power FREDFET. The resistor is referenced to HALF BRIDGE CONNECTION.

BYPASS HIGH-SIDE (BPH) Pin (Pin 14)
This pin connects to the external bypass capacitor for the high-side FREDFET Gate driver. The capacitor is referenced to HALF BRIDGE CONNECTION.

HALF-BRIDGE CONNECTION (HB) (Pin 16-19)
This pin connects to the Source of the high-side power FREDFET and to the Drain of the low-side power FREDFET. It is also the reference for the BYPASS HIGH-SIDE and the EXTERNAL CURRENT LIMIT HIGH-SIDE pins.

LOW-SIDE SOURCE (LS) (Pin 24)
This pin is the low-side power FREDFET Source connection. It connects to the SIGNAL GROUND through a Kelvin connection.

NOT CONNECTED (NC) Pins (Pins 2 (BRD116X only) 9, 12, 15)
This pin is not connected and should be left floating. Pin 2 only applies to BRD116X.

BridgeSwitch Functional Description

BridgeSwitch combines two high-voltage power FREDFETs, gate drivers and controllers into a single package. The FREDFETs are connected in a half-bridge configuration where their diode structure (ultra-soft and ultra-fast recovery) makes them ideal for hard-switched inverter-based motor drivers.

To reduce external components, the drive controllers feature integrated high-voltage current sources, allowing them to draw current directly from the high-voltage DC Bus. The high-side controller provides high-side status updates to the low-side controller which generates an instantaneous phase-current output signal (BRD126X). This unique capability allows the implementation of a sensor-less motor-control scheme. The controllers also ensure that the FREDFET turn-off is faster than turn-on resulting in an optimal balance between thermal performance and EMI.

BridgeSwitch offers integrated fault protection and system level monitoring via a bi-directional bussed single-wire status interface. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs as well as two-level thermal overload protection. BridgeSwitch offers sophisticated DC-bus sensing, providing four undervoltage levels and one overvoltage level, and can also support external sensors such as an NTC. Figure 3 shows the functional block diagram of the device along with key features.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pin Regulator

The BYPASS LOW-SIDE pin and the BYPASS HIGH-SIDE pin have internal regulators that charge the BYPASS LOW-SIDE pin capacitor and the BYPASS HIGH-SIDE pin capacitor to V_{BPL} and V_{BPH}, respectively. A current source connected to HIGH-SIDE DRAIN charges the BYPASS LOW-SIDE capacitor. Another current source connected to HIGH-SIDE DRAIN charges the BYPASS HIGH-SIDE capacitor whenever the low-side power FREDFET turns on. Both current sources start charging once the HD pin voltage reaches $V_{HD(START)}$ (min. 50 V). The BYPASS LOW-SIDE and the BYPASS HIGH-SIDE pins are the internal supply voltage nodes for the low-side and the high-side controllers and Gate drivers. When the low-side or the high-side power FREDFETs are on, the device operates from the energy stored in the BYPASS LOW-SIDE pin capacitor or the BYPASS HIGH-SIDE pin capacitor, respectively.

In addition, there are shunt regulators clamping the BYPASS LOW-SIDE pin to $V_{BPL(SHUNT)}$ and the BYPASS HIGH-SIDE pin to $V_{BPH(SHUNT)}$ when current is provided to the BYPASS LOW-SIDE pin and the BYPASS HIGH-SIDE pin from an external DC source through resistors (see R_{SL} and R_{SH} in Figure 6). External supply voltage V_{SUP} is greater than bypass shunt regulator voltage $V_{BPX(SHUNT)}$ plus the voltage drop of bootstrap diode D_{SH}. A typical value is V_{SUP} = 17 V. Resistors R_{SL} and R_{SH} limit the external supply current to less than 12 mA (2-5 mA recommended). Shorting BPL pins or BPH pins from separate devices directly together is not recommended.

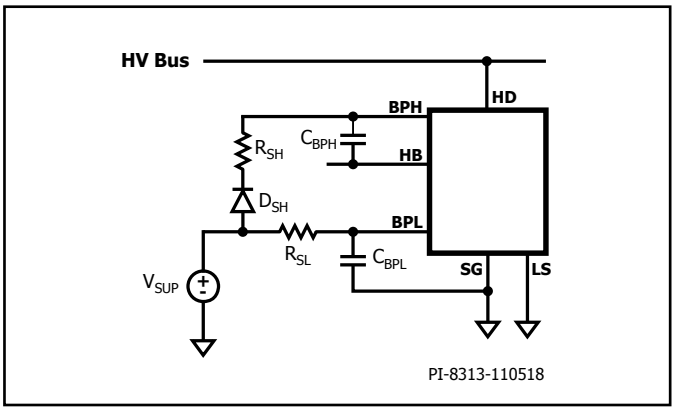


Figure 6. External BPL Pin and BPH Pin Power Supply Example.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pin Undervoltage Threshold

The BYPASS LOW-SIDE pin and BYPASS HIGH-SIDE pin undervoltage circuitries disable the respective power FREDFET when either the BYPASS LOW-SIDE pin voltage or the BYPASS HIGH-SIDE pin voltage drops below V_{BPL}-$V_{BPL(HYST)}$ or V_{BPH}-$V_{BPH(HYST)}$, respectively, in steady-state operation. Once either the BYPASS LOW-SIDE pin voltage or the BYPASS HIGH-SIDE pin voltage fall below this threshold, it must rise back up to V_{BPL} or V_{BPH}, respectively to enable power FREDFET switching.

BYPASS LOW-SIDE Pin and HIGH-SIDE Pins Capacitor Selection

Capacitors connected to the BYPASS LOW-SIDE pin and BYPASS HIGH-SIDE pin supply bias current for the low-side and the high-side controller and deliver the required Gate charge for turning on the low-side or the high-side power FREDFET. The BYPASS HIGH-SIDE pin capacitor supplies the high-side controller bias current over a time interval which is a function of the high-side commutation duty ratio and PWM frequency. The recommended maximum voltage ripple at the BYPASS HIGH-SIDE pin capacitor over this time interval is 250 mV. The minimum required capacitance value for both bypass low-side and bypass high-side is 0.33 µF. The recommended bypass low-side capacitance is 1 µF.

Given application operating conditions determine the required bypass high-side capacitance to keep ripple voltage below 250 mV. Figure 7 depicts the minimum recommended BYPASS HIGH-SIDE pin capacitance as function of high-side commutation duty ratio D_{HS} and PWM frequency.

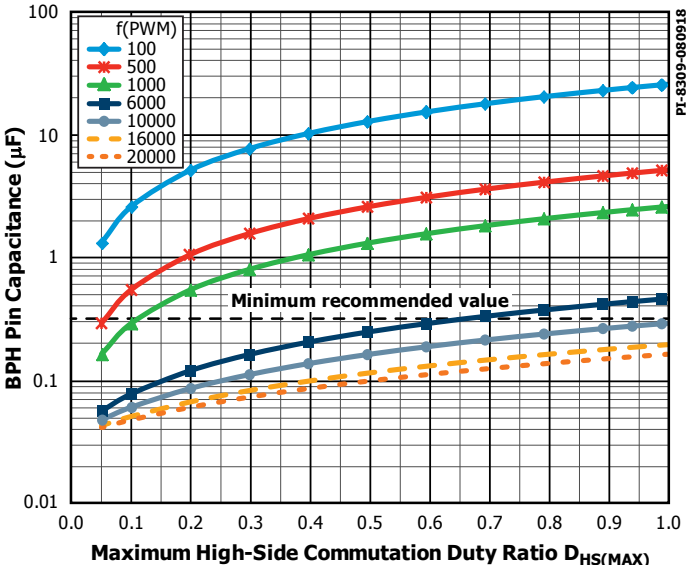


Figure 7. BYPASS HIGH-SIDE Pin Capacitance vs. High-Side Commutation Duty Ratio and PWM Frequency.

Note that multilayer chip capacitors (MLCC) can exhibit a significant DC bias characteristic. Selecting a BYPASS HIGH-SIDE pin capacitor (according to Figure 7) needs to take the possible capacitance reduction into account when biasing at V_{BPH}. Refer to the respective capacitor data sheet for details.

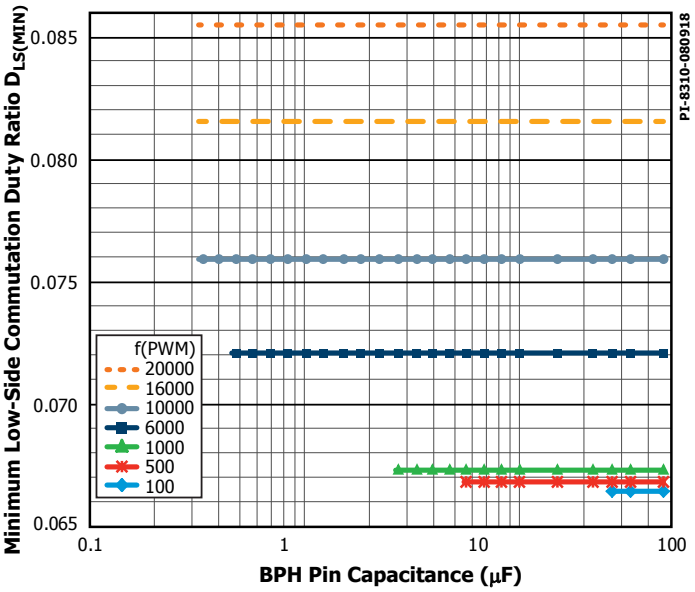


Figure 8. Minimum Low-Side Commutation Duty Ratio vs. BYPASS HIGH-SIDE Pin Capacitance and Low-Side PWM Frequency to Ensure Sufficient High-Side Self-Supply Current (High-Side Commutation Duty Ratio ≤ 0.95).

The BYPASS HIGH-SIDE pin capacitor recharges every time the low-side power FREDFET turns on. To ensure sufficient high-side self-supply current, the low-side power FREDFET on-time, as a function of chosen BYPASS HIGH-SIDE capacitance, low-side commutation duty ratio D_{LS} and PWM frequency, should meet the minimum low-side commutation duty ratio requirement $D_{LS(MIN)}$ shown in Figure 8. Note the maximum recommended voltage ripple of 250 mV across the bypass high-side capacitor restricts the choice of possible capacitance values at lower PWM frequencies.

Minimum low-side commutation duty ratio $D_{LS(MIN)}$ depicted in Figure 8 scales with the applicable maximum high-side commutation duty ratio in a given application. For example, the minimum low-side commutation duty ratio $D_{LS(MIN)}$ in an application operating at f_{PWM} = 6 kHz and a maximum high-side commutation duty ratio of $D_{HS(MAX)}$ = 0.95 is $D_{LS(MIN)}$ = 0.0435. $D_{LS(MIN)}$ increases by a factor of 0.99/0.95 to $D^*_{LS(MIN)}$ = 0.0453 if the same application operates for instance at a maximum high-side duty ratio of $D^*_{HS(MAX)}$ = 0.99.

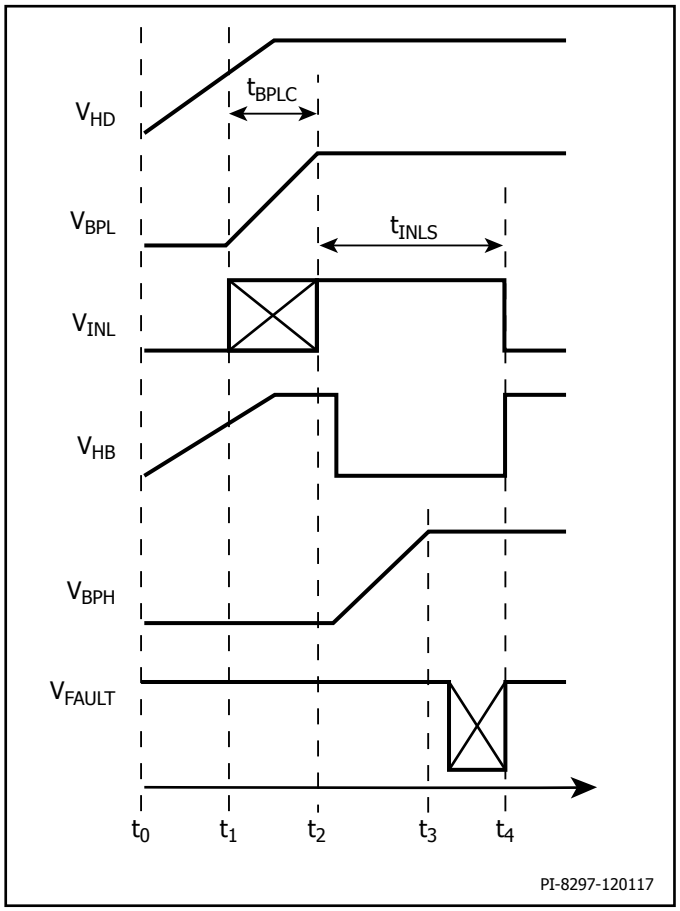


Figure 9. Recommended Power-Up Sequence with Self-supplied Operation.

Time Point	Activity
t_0	• High-voltage DC bus is applied
t_1	• Internal current source starts charging BPL pin capacitor once HD pin voltage reaches $V_{HD(START)}$ • System MCU may start setting low-side power FREDFET control signal INL to high
t_2	• BPL pin voltage reaches V_{BPL} (typically 14.5 V) • Device determines external device settings • Internal Gate drive logic turns on low-side power FREDFET after device setup completes and once INL becomes high or if it is high already • Internal current source starts charging BPH pin capacitor
t_3	• BPH pin voltage reaches V_{BPH} with respect to HB pin (typically 14.5 V). • Device starts communicating successful power-up through FAULT pin. Note: The device does not send a status update if the internal power-up sequence did not complete successfully.
t_4	• BridgeSwitch is ready for state operation (indicated by communicated status update starting at time point t_3) • System MCU turns off low-side power FREDFET

Table 2. Power-Up Sequence with Self-Supplied Operation.

Power-Up Sequence with Self-Supply

BridgeSwitch devices have internal self-supply supporting commutation PWM frequencies up to 20 kHz. To ensure a sufficient supply voltage levels across the BYPASS LOW-SIDE pin capacitor and the BYPASS HIGH-SIDE pin capacitor at inverter start-up, the system micro-controller (MCU) should follow the recommended power-up sequence depicted in Figure 9.

Table 2 lists activities occurring during the recommended power-up sequence.

The BYPASS LOW-SIDE pin capacitor C_{BPL}, the BPL pin charge current $I_{CH1(LS)}$, and the BYPASS LOW-SIDE pin voltage V_{BPL} determine the charging time t_{BPLC} starting at time point t1:

$$t_{BPLC} = t_2 - t_1 = \frac{C_{BPL} \times V_{BPL}}{I_{CH1(LS)}}$$

The system MCU manages the power-up sequence by controlling the time point t2 and duration t_{INLS} for turning on and off the low-side power FREDFET. The MCU may pull the CONTROL INPUT LOW-SIDE pin high any time after the full DC bus voltage is available (time point t_1). However, the device enables power MOSEFT switching only after the BYPASS LOW-SIDE pin voltages reaches V_{BPL} (typically 14.5 V) and the device setup completes. The device also reports a first status update through the FAULT pin once V_{BPL} reached typically 14.5 V

The high-side controller reports internally its status to the low-side controller at time point t3 after the BYPASS HIGH-SIDE pin voltage reaches V_{BPH} (typically 14.5 V) with respect to the HALF-BRIDGE CONNECTION pin. This is followed by a device status update to the system MCU through the STATUS COMMUNICATION pin.

A minimum low-side FREDFET on-time t_{INLS} is required for charging the BYPASS HIGH-SIDE pin capacitor, device setup, and status update communication through the FAULT pin. It is controlled by the system MCU and depends on the selected capacitance CBPH:

$$t_{INLS} = t_4 - t_2 \geq \frac{C_{BPH} \times V_{BPH}}{I_{CH1(HS)}} + 1\,ms$$

The system MCU should proceed with the power-up sequence described above, if a latching thermal shutdown had occurred and it decides to restart the inverter by first sending a FAULT latch reset command (see Table 7 for details).

Gate Drive Control Inputs

The low-side and high-side power FREDFETs are controlled through INL and /INH logic inputs. Both inputs are compatible with 3.3 V and 5 V CMOS logic levels. The low-side power FREDFET latches on or off with the edge of the active high INL signal during steady-state operation. The high-side power FREDFET latches on or off with the edge of the active low /INH signal. The INL input has an internal weak pull-down and the /INH input has an internal weak pull-up. This prevents accidental power FREDFET turn-on in case one or both control inputs are floating.

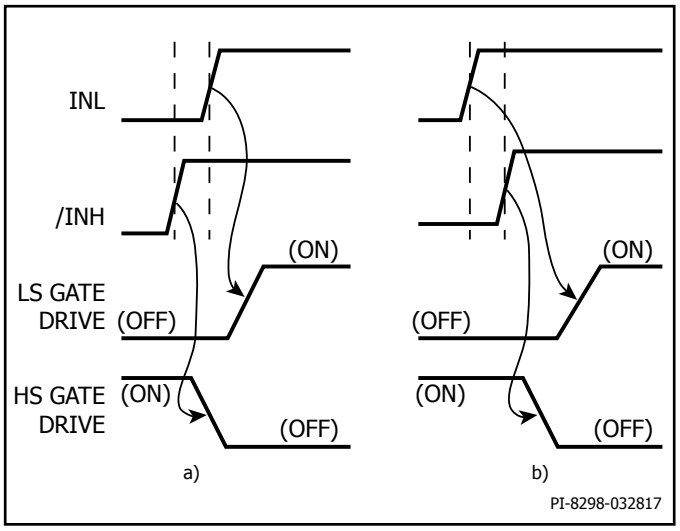


Figure 10. Simultaneous Conduction Lockout a) Not Active b) Active.

BridgeSwitch integrates simultaneous conduction lockout protection. A latch inhibits turning on the low-side power FREDFET Gate drive circuitry until the rising edge of the high-side control signal /INH has occurred (see Figure 10). The latch also inhibits turning on the high-side power FREDFET Gate drive circuitry until the falling edge of the low-side control signal INL has occurred.

The inverse logic polarity of INL and /INH control inputs allows optionally tying both together for controlling both power FREDFETs with a single PWM signal. To prevent possible FREDFET cross conduction, the integrated Gate drive logic applies adaptive dead times as shown in Figure 11. The falling edge of the low-side power FREDFET control input INL triggers the t_{DLH} timer (Dead Time low-side power FREDFET off to high-side power FREDFET on). The integrated Gate control logic enables turning on the high-side FREDFET Gate drive only after t_{DLH} expires. The rising edge of the high-side power FREDFET control input /INH triggers the t_{DHL} timer (Dead Time high-side power FREDFET off to low-side power FREDFET on). The integrated Gate control logic enables turning on the low-side FREDFET Gate drive only after t_{DHL} expires.

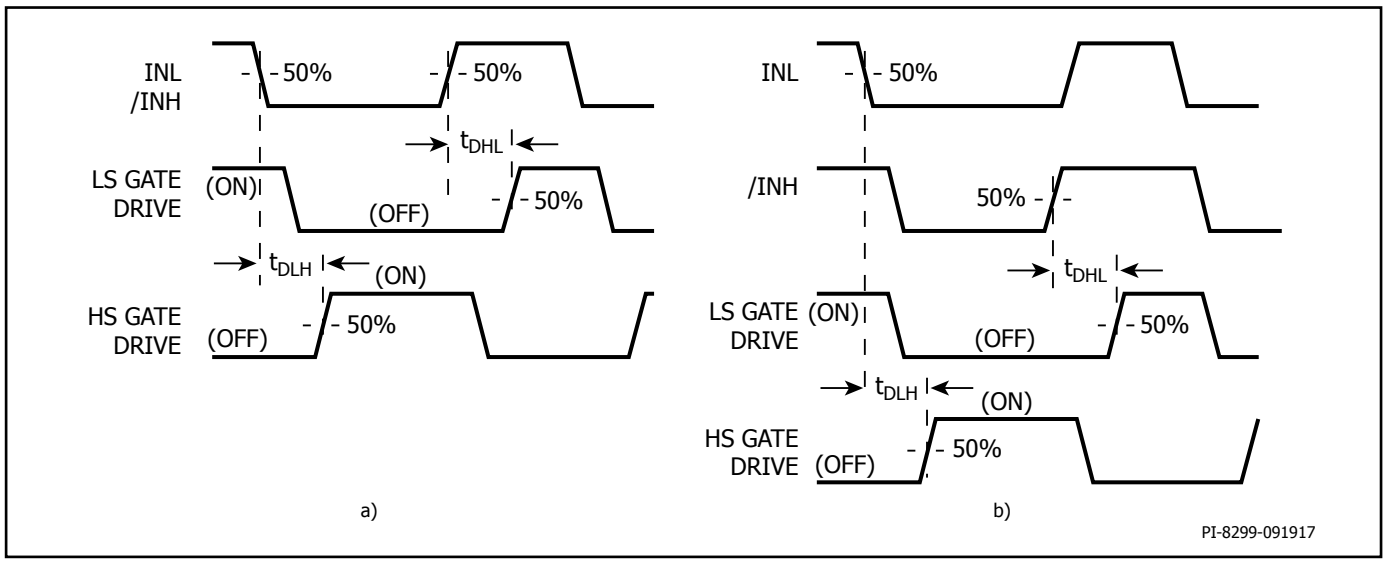


Figure 11. Adaptive Dead Time a) INL and /INH Inputs Tied Together b) INL and /INH Inputs Separate.

Device Internal High-Side Status Update

The BridgeSwitch high-side controller provides status updates to the low-side controller. The status update communicates triggered device level protection such as high-side power FREDFET over current or low-side power FREDFET over-temperature warning or shutdown. It also includes detected device faults such as XH pin short or open circuit and loss of high-side power supply. The high-side controller provides the internal status update every time the low-side power FREDFET turns on. For correct internal status updates, the system micro-controller has to set the INL control input high for at least $t_{INLH(COM)}$ (see Figure 24 for details). INL input turn-on control signals shorter than $t_{INHL(COM)}$ may cause incomplete internal status updates followed by the device reporting a "HS Driver not ready" status update (see Table 4).

Adjustable Cycle-by-Cycle Current Limit

BridgeSwitch devices feature cycle-by-cycle current limit protection for both, the low-side and the high-side power FREDFET. As soon as the power FREDFET current exceeds the respective current limit level threshold after the leading edge blanking timer t_{LEB} expires, the device turns off the power FREDFET. The FREDFET stays off until a turn-off edge followed by a turn-on edge is received at the respective INL or /INH control input. The device will also report the respective over-current fault through the STATUS COMMUNICATION pin (see Table 4 for details).

The actual current limit level is programmed through the external small signal resistor R_{XL} or R_{XH} (see Figure 1) connected to either the EXTERNAL CURRENT LIMIT LOW-SIDE pin or to the EXTERNAL CURRENT LIMIT HIGH-SIDE pin. Figure 12 shows the relationship between the resistor connected to XL pin or XH pin and the programmed normalized current limit level normalized to the default current limit level $I_{LIM(DEF)}$.

The recommended operating range for the actual set current limit level is 42% to 100% of $I_{LIM(DEF)}$ and a resistance range for R_{XL} or R_{XH} of 44.2 kΩ to 133 kΩ.

FREDFET switching is disabled for R_{XL} or R_{XH} values smaller than 35 kΩ and the device reports either a LS driver not ready or a HS driver not ready status update through the FAULT pin (refer to Table 4). This prevents inverter malfunction in case the programming resistor is accidentally short-circuited. The device continues to accept LS FREDFET turn-on signals in case it detects a short-circuit at the XH pin.

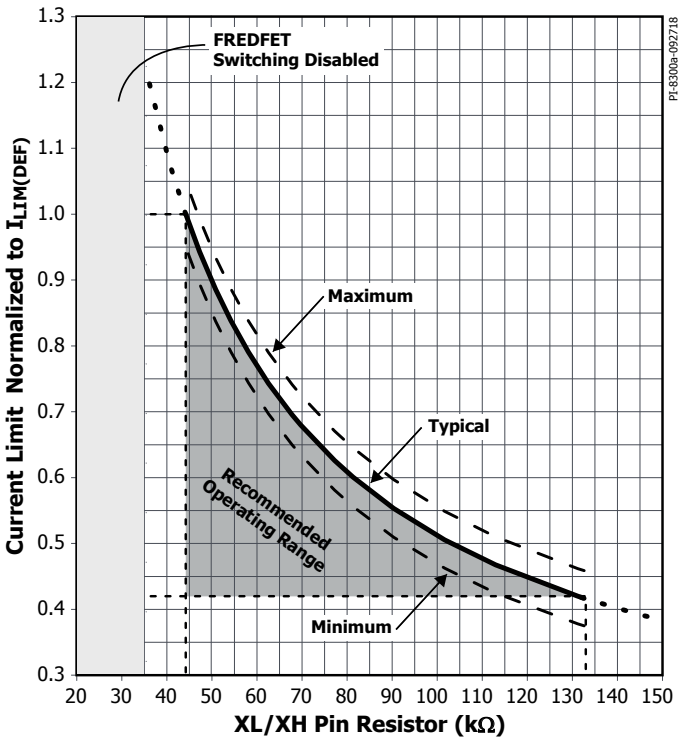


Figure 12. Cycle-by-Cycle Current Limit Level Programming Through EXTERNAL CURRENT LIMIT Pin.

A detected short-circuit at the XL pin will eventually cause the HS FREDFET switching to cease as well because the BPH pin capacitor is only re-charged when the LS FREDFET turns on. The normalized current limit level continues to fall below 42% down to 0% of $I_{LIM(DEF)}$ for R_{XL} or R_{XH} values greater than 133 kΩ. This provides protection against possible XL pin or XH pin open circuit faults where the effective current limit threshold is 0. However, below 42% the specified current limit level tolerance is not guaranteed.

Adding capacitors to the XL pin or XH pin is not recommended.

Device Over-Temperature Protection

BridgeSwitch devices feature an integrated dual level thermal overload protection. The device continuously monitors the temperature of the low-side power FREDFET. It will send a status update through the STATUS COMMUNICATION pin as soon as it reaches the lower Device Warning Temperature level T_{WA} (see Table 4 for details). The device disables FREDFET switching permanently once the FREDFET temperature exceeds the Device Shutdown Temperature threshold T_{SD} to prevent device damage. Additionally it will report the over-temperature fault through the FAULT pin. System level monitoring through the SYSTEM MONITOR pin continues and the device will report any additionally occurring status changes through the STATUS COMMUNICATION pin. The system MCU can re-enable FREDFET switching by sending the fault latch reset command through the FAULT bus (see Table 7 for details). Alternatively operation may resume after a full power-up sequence initiated by the system MCU.

Phase Current Information Output

BridgeSwitch BRD126X devices feature instantaneous motor winding phase current information through a resistor connected to the PHASE CURRENT OUTPUT pin. The voltage across the small signal resistor is a direct representation of the low-side power FREDFET Drain to Source channel current. The system MCU can digitize this voltage and use it for instance as an input for a chosen motor control algorithm. The device supports either independent phase current information through individual IPH pin resistors or a composite phase current signal through interconnected IPH pins with a single resistor as shown in Figure 13.

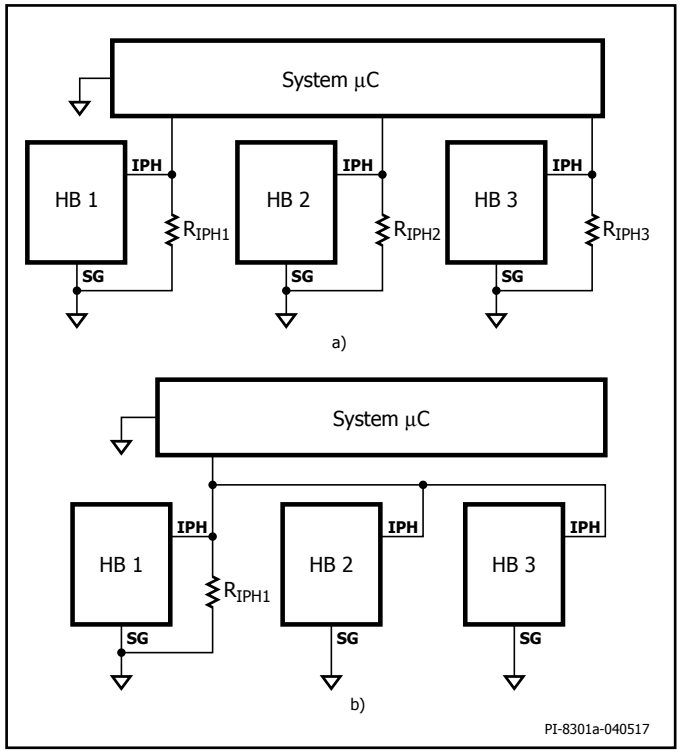


Figure 13. Phase Current Information through IPH Pin with BRD126X a) Individual Phase Currents b) Composite Phase Current.

The Phase Current Output Gain g_{IPH} and the resistor R_{IPH} connected to the PHASE CURRENT OUTPUT determine the voltage amplitude V_{IPH} at a given phase current I_{PHASE}:

$$V_{IPH} = R_{IPH} \times I_{PHASE} \times g_{IPH}$$

Maximum permissible voltage amplitude of V_{IPH} is 3.0 V.

External Current Sensing

BRD116X devices support discrete low-side FREDFET current sensing through an external current sense resistor in series with the LS pin. Figure 14 depicts one possible implementation example.

Voltage V_{SHUNT} is a direct representation of the motor winding current I_{MOTOR}. Resistor R1 and R2 set the gain of external amplifier U1. Resistor R3, C1, C2, and C3 provide noise filtering. Resistor R4 adds a DC offset V_{OFFSET} to the amplifier U1 output signal V_{OP}.

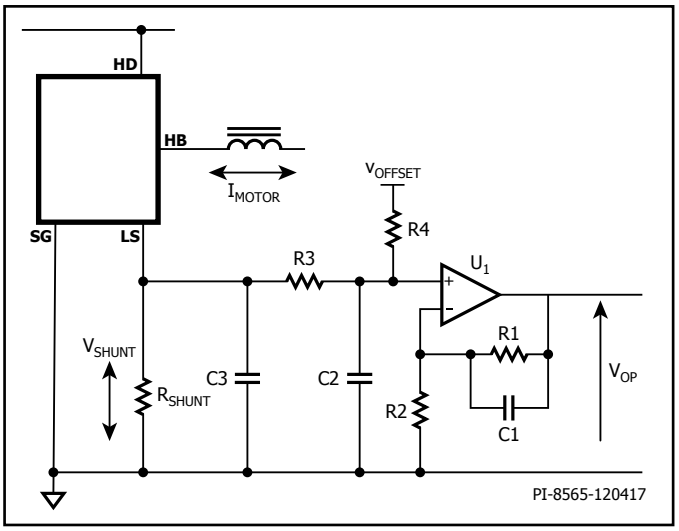


Figure 14. External Current Sense Example Circuit (BRD116X).

$$V_{OP} = \left(1 + \frac{R1}{R2}\right)\frac{V_{OFFSET} \times R3 + I_{MOTOR} \times R_{SHUNT} \times R4}{R3 + R4}$$

The voltage differential V_{SHUNT} between SG and LS pins should not exceed ±0.33 V. Current sense resistor R_{SHUNT} in series with the LS pin has to be sized accordingly.

System Monitor Input

BridgeSwitch features system level monitoring through the SYSTEM MONITOR input. The SM pin supports monitoring either the high-voltage (HV) DC bus (see Figure 14) or the temperature of an external component through an NTC thermistor (see Figure 16). The SM pin is self-configuring. It automatically detects the type of external connection and locks in the respective circuitry configuration at power-up.

High-Voltage DC Bus Monitoring

The SYSTEM MONITOR pin continuously monitors the high-voltage DC bus voltage level by sensing the current into this pin. The current I_{SM} into the SM pin is a direct representation of the high-voltage bus voltage level V_{BUS}:

$$I_{SM} = \frac{V_{BUS} - V_{SM}}{R_{HV1}}$$

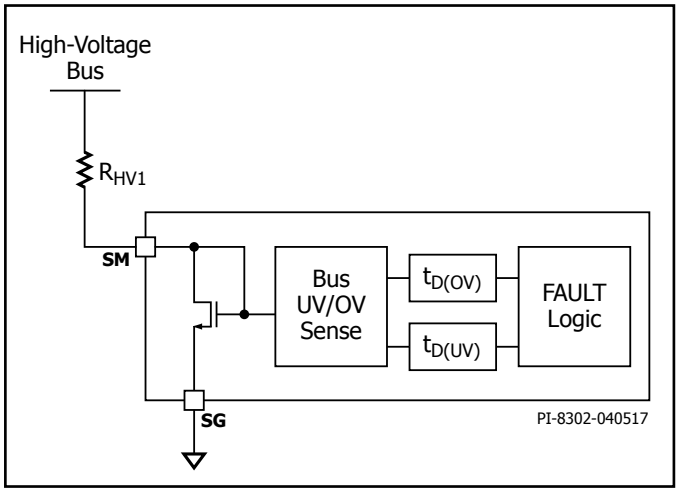


Figure 15. High-Voltage Bus Monitoring with SYSTEM MONITOR Pin.

The bus voltage sensing circuitry has five distinct current thresholds as shown in Figure 16. Thresholds I_{UV55}, I_{UV70}, I_{UV85}, and I_{UV100} are used to detect high-voltage bus undervoltage conditions. Threshold I_{OV} is used to detect a high-voltage bus overvoltage condition. The device reports a high-voltage bus fault through the STATUS COMMUNICATION pin anytime the current into the SM pin either drops below one of the four undervoltage thresholds or if it exceeds the overvoltage threshold (see Table 4 for details).

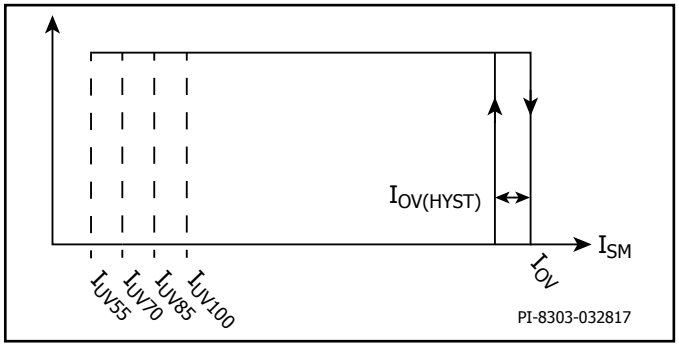


Figure 16. System Monitor Input Current Thresholds.

An undervoltage condition has to be present for at least $t_{D(UV)}$ (typically 40 ms) before it is reported to the system MCU. The device also communicates if a given undervoltage condition clears for at least $t_{D(UV)}$.

Note, during a bus brown-out condition, the device will report for instance a UV 70% status update if the bus voltage falls below 177 V for at least $t_{D(UV)}$ with a 7 MΩ sensing resistance (refer to Tables 3 and 4). If in this example the bus voltage recovers and rises above 177 V for at least $t_{D(UV)}$, the UV 70% condition clears and the device will report a UV 85% status update.

In case the SM pin current exceeds I_{OV} for at least $t_{D(OV)}$ (typically 80 μs), BridgeSwitch terminates the current low-side or high-side power FREDFET on-time and reports the fault to the system MCU through the FAULT pin. It ignores any subsequent FREDFET turn-on signals received at either INL or /INH until the SM pin current has dropped by at least $I_{OV(HYST)}$ for the duration of $t_{D(OV)}$. The FAULT pin reports a status update once the high-voltage bus overvoltage condition has cleared.

The system MCU may decide to stop sending turn-on signals to other BridgeSwitch devices in the inverter until the bus OV fault condition has cleared and the bus sensing device provided a status update accordingly. A full power-up sequence is recommended after the bus OV fault clears. High-side BYPASS capacitors may have discharged due to the disabled low-side FREDFET switching during the bus OV fault. Table 3 lists exemplary high-voltage bus monitoring thresholds with three different sensing resistor R_{HV1} values.

Sensing Resistor R_{HV1}	**6 MΩ**	**7 MΩ**	**8 MΩ**
	Bus Voltage UV or OV Threshold		
I_{OV} (typically 60 μA)	362 V	422 V	482 V
I_{UV100} (typically 35 μA)	212 V	247 V	282 V
I_{UV85} (typically 30 μA)	182 V	212 V	242 V
I_{UV70} (typically 25 μA)	152 V	177 V	202 V
I_{UV55} (typically 20 μA)	122 V	142 V	162 V

Table 3. Effective High-Voltage Bus Monitoring Thresholds.

Using multiple sense resistors with different values on more than one device increases the bus voltage sensing granularity further. Overvoltage protection can be disabled by limiting the current into the SM pin to less than the I_{OV} threshold through Zener diode V_{R1} and resistor R_{HV2} as shown in Figure 18. Bus undervoltage sensing remains active in this configuration.

Adding a small capacitor (maximum 100 pF) to the SM pin can improve bus monitoring accuracy in noisy environments.

System Level Temperature Monitoring

The SYSTEM MONITOR pin enables monitoring the temperature of an external component through an NTC thermistor as shown in Figure 17. Resistor R_2 allows fine-tuning the actual over-temperature threshold to the desired level with a given NTC resistor.

Current source I_{TM} (typically 96 μA) periodically injects a current into the NTC thermistor R_{NTC}. Its resistance falls with the temperature rising. Once the voltage level at the SM pin drops below $V_{TH(TM)}$ (typically 1.2 V), the detected system level over-temperature fault is communicated through the FAULT-pin after delay timer $t_{D(TM)}$ expires (see Table 4 for details). The resistance of thermistor $R_{NTC(TSYS)}$ at the desired system over-temperature threshold T_{SYS} determines R_2:

$$R_2 = 12.5\ k\Omega - R_{NTC(TSYS)}$$

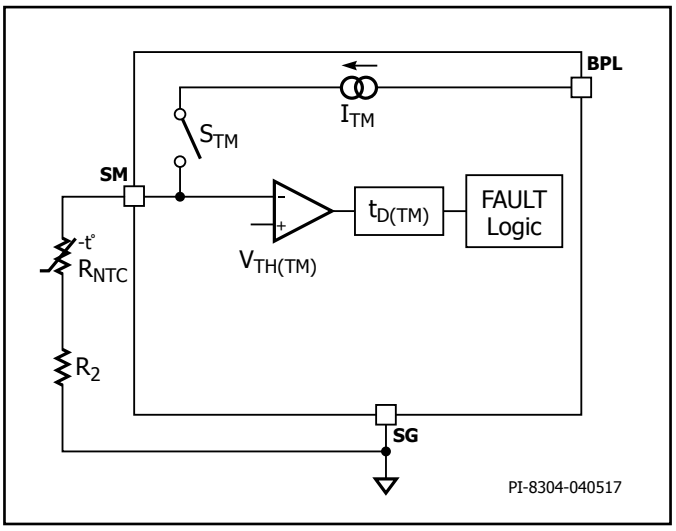


Figure 17. External Component Thermal Monitoring with SYSTEM MONITOR Pin.

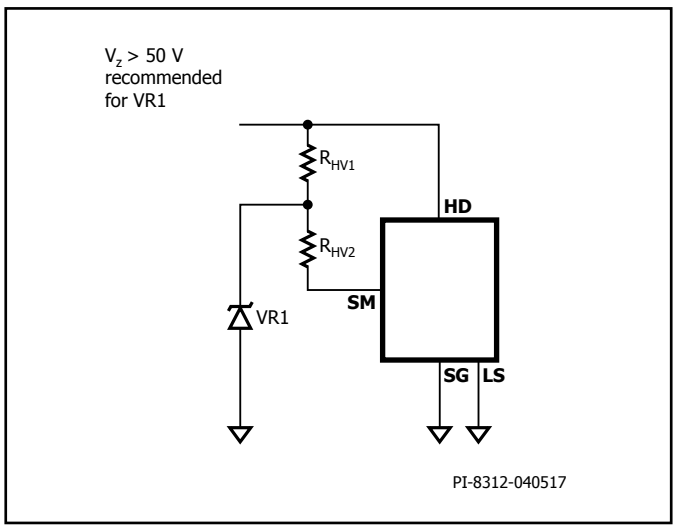


Figure 18. High-Voltage Bus Monitoring with Overvoltage Protection Disabled.

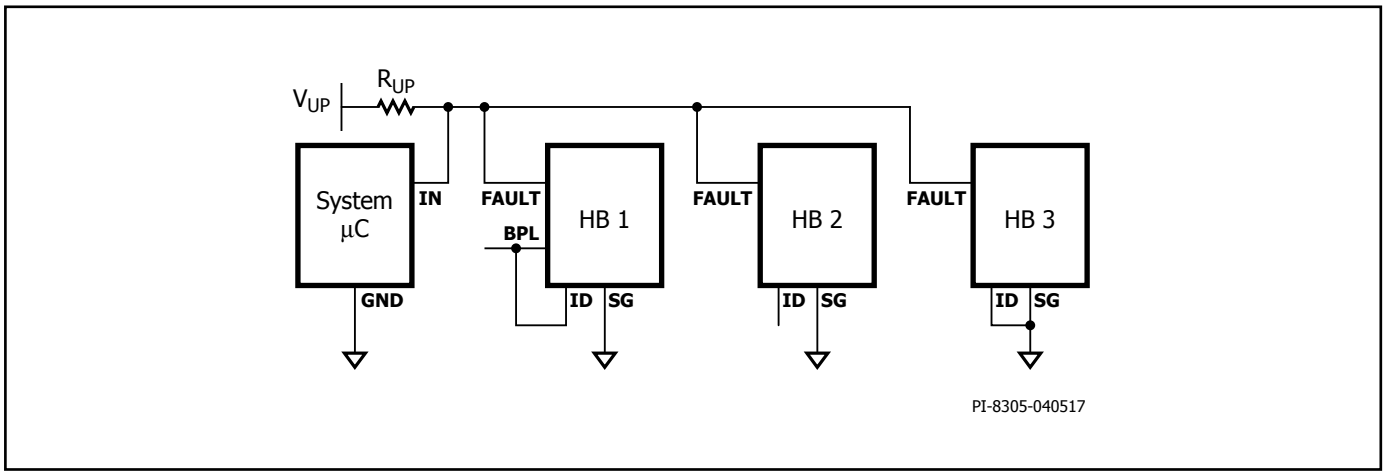


Figure 19. Single Wire Status Communication Bus with Device ID Programming.

Status Communication Bus

BridgeSwitch communicates status updates, including device or system level faults, to the system MCU through its open Drain FAULT pin. All FAULT pins connect to a single bus minimizing the number of pins occupied at the system MCU as shown Figure 19. The bus is pulled up to the system supply voltage through pull-up resistance R_{UP}. The minimum pull-up resistance R_{UP} the STATUS COMMUNICATION pin can drive is 2 kΩ for V_{UP} = 3.3 V or V_{UP} = 5 V. Pull-up resistance R_{UP} should not exceed 100 kΩ.

Status Word

BridgeSwitch uses a 7-bit word followed by a parity bit to report a status update (refer to Figure 21 for the timing diagram). Table 4 summarizes how various conditions are encoded. The 7-bit word consists of five blocks with status changes grouped together that cannot occur at the same time. This enables simultaneous reporting of multiple fault conditions to the system MCU. Grouping status conditions also allows reporting if a given fault condition has cleared. Cleared fault reporting applies to system level faults (bits 0, 1, and 2) and to low-side FREDFET thermal warning and loss if internal communication (bits 3 and 4). The status register entry in the bottom row (7-bit word "000 00 0 0") encodes Device Ready status and is used to communicate a successful power-up sequence. The device also sends it to acknowledge a status request sent by the system MCU in case no fault condition is present at the time (see Table 7 for details). The parity bit is generated using odd parity.

Table 5 lists examples of possible status update codes the device may communicate to the system MCU and the resulting transmit time for the respective status update. Transmission times range from 290 µs to 470 µs.

Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I_{OV}	0	0	1	X	X	X	X
High-voltage bus UV 100%	I_{UV100}	0	1	0	X	X	X	X
High-voltage bus UV 85%	I_{UV85}	0	1	1	X	X	X	X
High-voltage bus UV 70%	I_{UV70}	1	0	0	X	X	X	X
High-voltage bus UV 55%	I_{UV55}	1	0	1	X	X	X	X
System thermal fault	$V_{TH(TM)}$	1	1	0	X	X	X	X
LS Driver not ready[1]	n/a	1	1	1	X	X	X	X
LS FET thermal warning	T_{WA}	X	X	X	0	1	X	X
LS FET thermal shutdown	T_{SD}	X	X	X	1	0	X	X
HS Driver not ready[2]	I_{COM}	X	X	X	1	1	X	X
LS FET over-current	$V_{X(TH)}$	X	X	X	X	X	1	X
HS FET over-current	$V_{X(TH)}$	X	X	X	X	X	X	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

Table 4. Status Word Encoding.
Notes:
1. Includes XL pin open/short-circuit fault and IPH pin to XL pin short-circuit.
2. Includes internal communication loss, supply out of range, and XH pin open/short-circuit fault.

Fault	7-Bit Word	Parity Bit	Transmit Time $t_{TRANSMIT}$[1]
Device Ready (no faults)	000 00 0 0	1	290 µs
High-voltage bus UV 100%	010 00 0 0	0	290 µs
LS FREDFET thermal warning and over-current	000 01 1 0	1	350 µs
System thermal fault, LS FET thermal warning, HS & LS FET over-current	110 01 1 1	0	410 µs
Maximum transmission duration	111 01 1 1	1	470 µs

Table 5. Example Status Update Codes and Resulting Transmit Times.
Notes:
1. Assumes t_{ID} = 80 µs (device ID #3).

Device ID Selection

At power-up, each device assigns itself a unique device ID depending on the DEVICE ID pin connection. This device ID allows communicating the physical location of a detected fault condition to the system MCU. The device ID is also used for bus arbitration purposes. Table 6 lists the device ID, resulting Device ID Time Period t_{ID}, and how to program the respective ID through the ID pin (refer to Figure 19). Note that the system MCU is assigned automatically a default t_{ID} = 160 µs, thereby ensuring that it always wins bus arbitration.

Device ID	t_{ID}	ID Pin Connection
1	40 µs	Connected to BPL pin
2	60 µs	Floating
3	80 µs	Connected to SG pin
System MCU	160 µs	n/a

Table 6. Device ID Selection Through the ID Pin at Power-Up.

Status Communication

Communication on the FAULT bus initiates for one of the following three reasons:

1. Ready for mission mode communication after a successful power-up.
2. A FAULT status register update communication initiated by one of the devices.
3. A current status communication following a query by the system micro-controller.

Figure 20 summarizes the status communication flowchart for all three cases listed above.

Besides a status query, the system micro-controller can also send a command to reset the status register (see Table 7 and steps 16 and 17 in Figure 20). A power-up sequence is recommended after sending the reset command (refer to Figure 9).

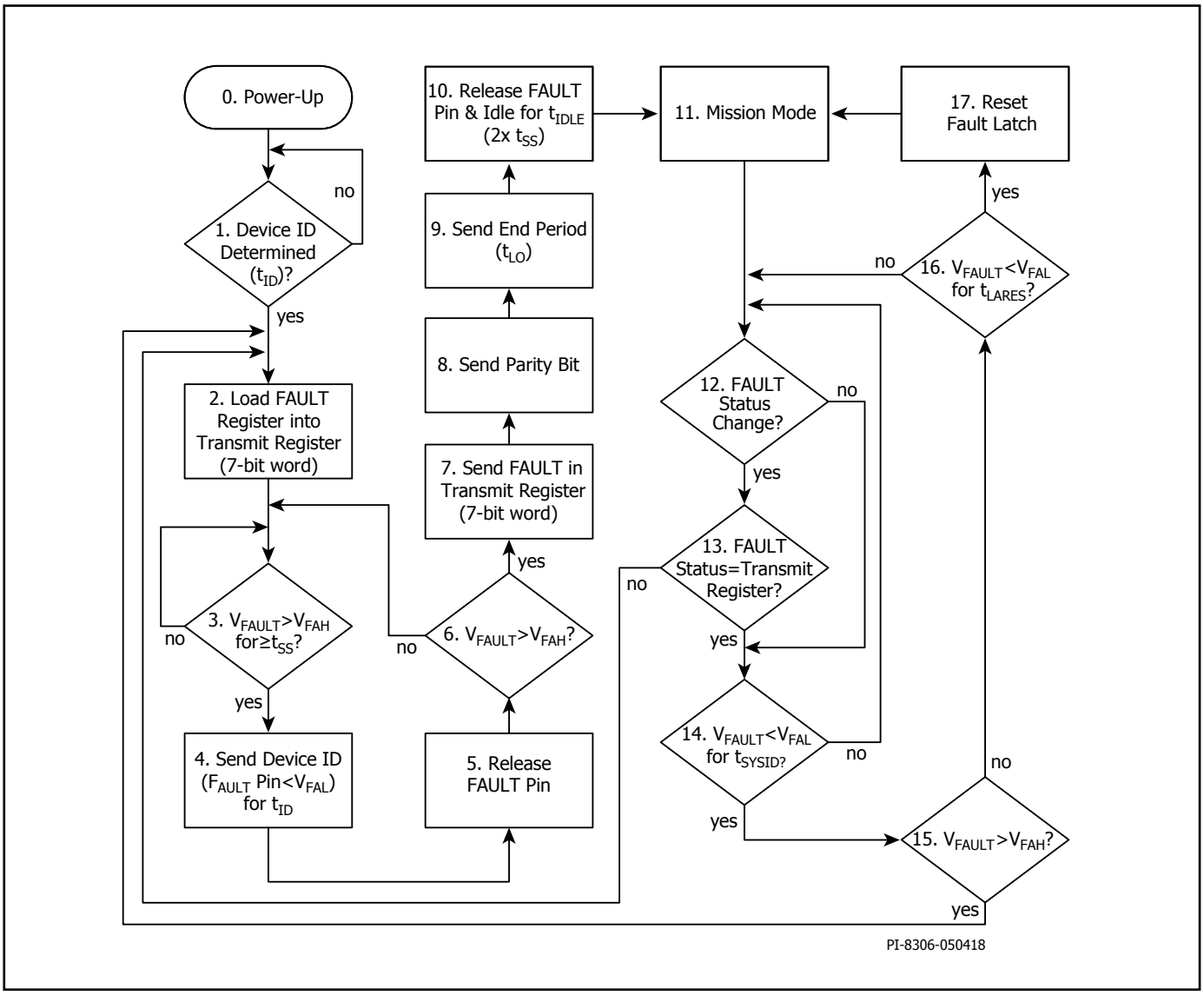


Figure 20. Status Communication Flowchart.

Figure 21 depicts the bit stream timing diagram BridgeSwitch uses for a status update communication. The two logic states are encoded with two different voltage signal high-time periods at the STATUS COMMUNICATION pin followed by a low-time period t_{LO} (typically 10 µs). A logic "1" is encoded with a period t_{BIT1} (typically 40 µs) and a logic "0" is encoded with a period t_{BIT0} (typically 10 µs).

Each time BridgeSwitch detects a status change, it loads the actual FAULT register into the Transmit register (see step 2 in Figure 20) and proceeds with a status update transmission.

The device starts a status update transmission only if the bus has been idle for at least the Steady State Time Period t_{SS} (typically 80 µs) to ensure that no other device uses the bus already (see step 3 in Figure 20).

A status update transmission starts always with bus arbitration initiated by the communicating device. It pulls the FAULT pin low for its assigned Device ID Time Period t_{ID} (refer to Table 6), releases the pin and then verifies that the communication bus stays high (see steps 4 to 6 in Figure 20). If this is the case, the device has won bus arbitration and can proceed with transmitting its status update (see steps 7 to 10 in Figure 20). If the bus stays low after sending its ID, another device started a transmission attempt (or bus arbitration) at the same time. In this case the device will make another communication attempt by proceeding back to step 3 in Figure 20. After each completed transmission the device will idle for t_{IDLE} (typically $2 \times t_{SS}$ = 160 µs) before starting a new communication. This enables other devices on the bus to communicate a possible occurred status change or to respond to a status inquiry sent by the system MCU.

The device communicates each detected status update only once. It also reports a status change for all system level faults to the system MCU. This includes DC bus undervoltage and overvoltage conditions and external temperature monitor faults. It also reports all status level changes for device internal faults with the exception of the LS power FREDFET thermal shutdown fault (a cleared LS power FREDFET thermal warning is reported).

Status Query and Fault Latch Reset

The device monitors the STATUS COMMUNICATION pin for possible commands sent by the system MCU once it is mission mode. This could be a status update inquiry (see step 15 in Figure 20) by the MCU through it pulling the bus low for a period of t_{SYSID} (typically 160 µs). Or it could be a command to reset the device status register including over-temperature shutdown latch and to enter the power-up sequence mode (see step 17 in Figure 20) by pulling the FAULT bus low for a period of t_{LARES} (2x t_{SYSID} = typically 320 µs). Note, a power-up sequence (refer to Figure 9) is recommended after the MCU has sent a latch reset command. This ensures that the bypass high-side voltage is at the nominal level before switching resumes. Table 7 summarizes available system MCU commands.

Bus Pulldown Period	Command
t_{SYSID}	Status query
t_{LARES} (2x t_{SYSID})	Status register including over-temperature latch reset and power-up sequence mode

Table 7. System MCU Commands.

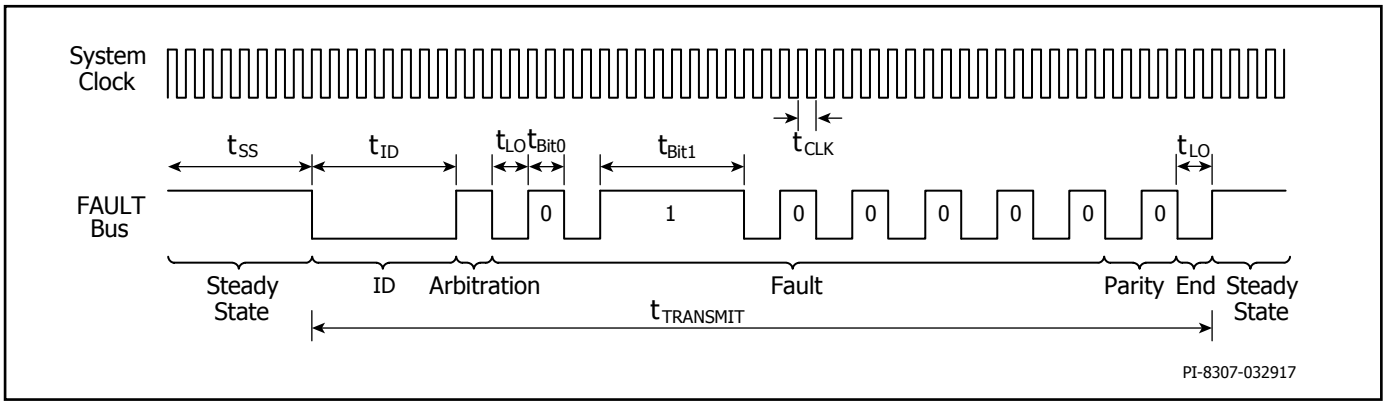


Figure 21. Status Communication Bit Stream.

Application Example

A High Efficiency, 300 W, Three-Phase Inverter

The schematic shown in Figure 22 is a 3-phase inverter using three BRD1265C devices. The design is capable of driving a high-voltage, 3-phase brushless DC (BLDC) motor from a rectified AC input voltage. The design is rated for a continuous input power of 300 W and 1 A_{RMS} phase current at a DC input voltage of 340 V and 12 kHz PWM switching frequency without requiring a heat sink thanks to its full load efficiency of greater than 98%. The inverter design supports various motor control schemes through proper interface between a system microcontroller board and this inverter. This design demonstrates high efficiency across a wide load range and does not require a low voltage supply thanks to the self-biased operation of the BRD1265C devices. The inverter offers a variety of device fault protections and system level telemetry. Fault protection on a device level includes low-side and high-side FREDFET cycle-by-cycle current limit protection and a two level thermal overload warning and protection. System level telemetry includes high-voltage DC bus monitoring and system level thermal monitoring. A simple, single wire interface communicates all observed status updates to the system microcontroller.

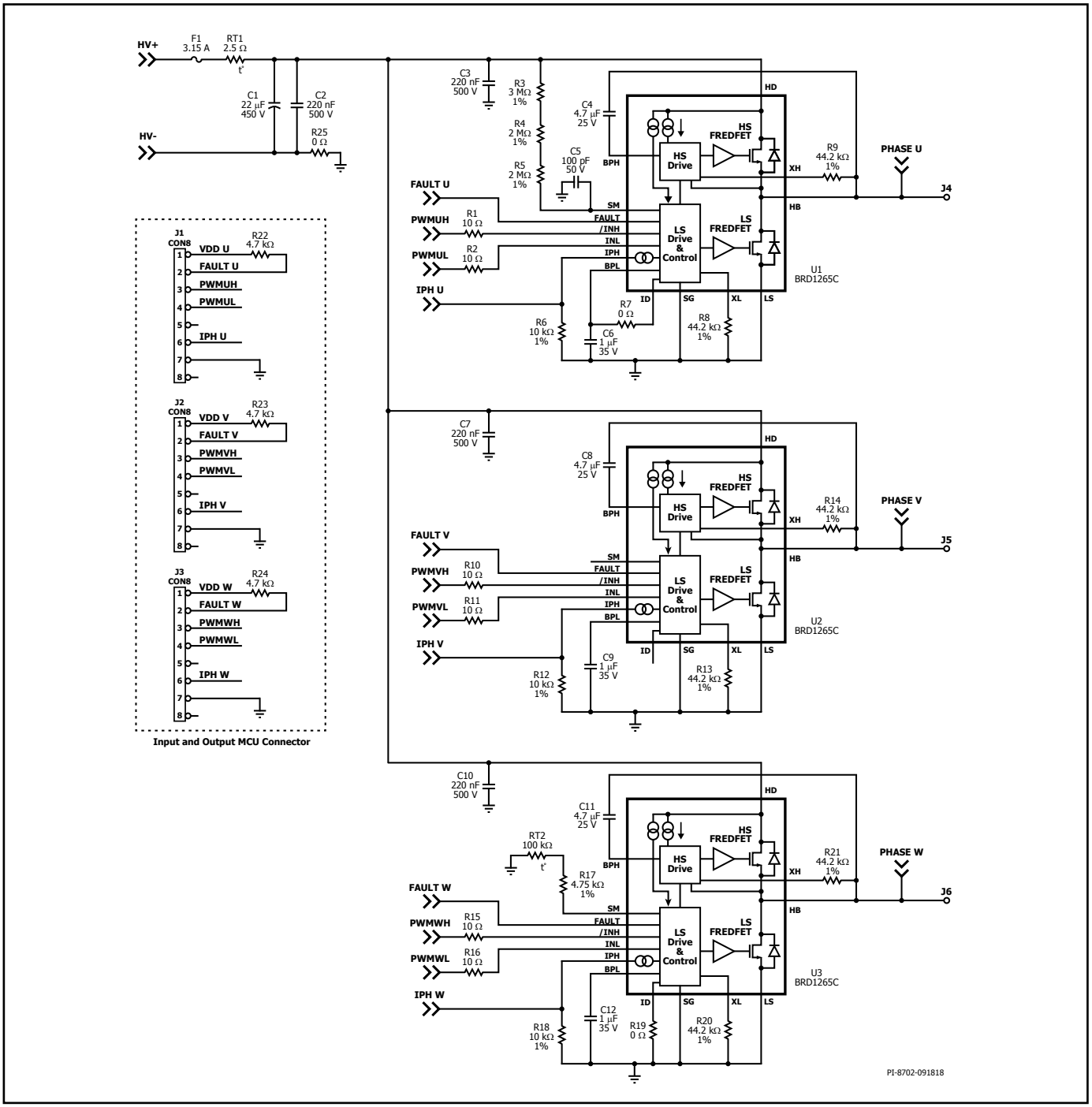


Figure 22. Schematic DER-654. Three-Phase Inverter Example using BRD1265C.

Input Stage
Fuse F1 provides over-current protection and thermistor RT1 limits the inrush current. C1 and C2 provide local decoupling of rectified AC input voltage. Resistor R25 is placed on the main input return path to allow sensing of the input DC current if desired. A zero ohm resistor is used as a place holder.

Three-Phase BridgeSwitch Inverter
The three BridgeSwitch devices U1, U2, and U3 form the 3-phase inverter. The outputs of the inverter connect to the 3-phase BLDC motor through connectors J4, J5, and J6. Capacitors C3, C7, and C10 provide local high frequency decoupling of the DC bus voltage to BridgeSwitch.

BridgeSwitch Bias Supply
Capacitors C6, C9, and C12 provide decoupling for the BridgeSwitch integrated low-side controller and gate driver. Capacitors C4, C8, and C11 provide decoupling for the integrated high-side controller and gate driver.

PWM Inputs
Input signals PWMUH, PWMUL, PWMVH, PWMVL, PWMWH, and PWMWL control the switching state of the integrated high-side and low-side power FREDFETs. The system microcontroller connects through J1, J2, and J3 to drive the BridgeSwitch low- and high-side FREDFET control inputs INL and /INH. Resistors R1, R2, R10, R11, R15, and R16 situated between system microcontroller outputs and BridgeSwitch PWM control inputs improve integrity of control signals from the system microcontroller.

Cycle-by-Cycle Current Limit
Resistors R8, R13, and R20 set the cycle-by-cycle current limit level for the integrated low-side FREDFETs while R9, R14, and R21 set the cycle-by-cycle current limit level for the integrated high-side power FREDFETs. The selected value of 44.2 kΩ sets the current limit at 100% of the default value or 3 A for BRD1265C (refer to Figure 12 for current limit program details).

Phase Current Information
Each BRD1265C provides instantaneous phase current information through the IPH pin. Resistors R6, R12, and R18 determine the small signal voltage amplitude. The IPH pin output gain is 100 μA/A which translates into a 1 V signal for a 1 A Drain current with the selected value of R6, R12 and R18 (10 kΩ). The voltage signal is available through pin 6 of connectors J1, J2, and J3 for interfacing to the system microcontroller.

DC Bus Undervoltage (UV) and Overvoltage (OV) Monitoring
BridgeSwitch U1 monitors the DC bus voltage through resistors R3, R4, and R5. The combined resistance of R3, R4 and R5 sets the undervoltage thresholds and overvoltage threshold as shown in Table 3. Optional capacitor C5 provides high frequency noise decoupling at the SM pin in noisy environments. The recommended maximum value is 100 pF. The FAULT interface of U1 reports any detected DC bus voltage change to the system microcontroller via connector J1.

System Level Temperature Monitoring
BridgeSwitch U3 monitors the system temperature through thermistor RT2 connected to the SM pin. Resistor R17 tunes the threshold of the system level fault temperature to the desired level. In this example, it is 90 °C.

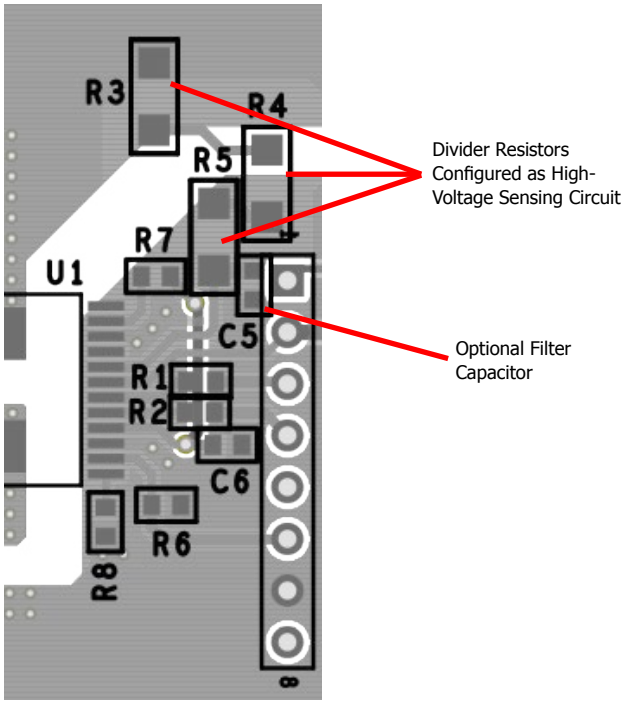
Status Update Communication
The FAULT pins of U1, U2, and U3 report any detected status updates to the system microcontroller via J1, J2, and J3 respectively. Open Drain FAULT pins are pulled high to VDD_U, VDD_V, and VDD_W through resistors R22, R23, and R24.

Device ID
Each BRD1265C assigns itself a unique device ID by determining its ID pin connection at power-up. The device ID enables communication of the physical location of a detected status update to the system microcontroller (refer to Figure 19 for Single Wire Status Communication Bus with Device ID Programming). In the design shown in Figure 22, U1 has its ID pin shorted to BPL pin via R7. The ID pin on U2 is left open, while U3 has its ID pin shorted to SG pin via R19 (refer to Table 6 for ID assignment details).

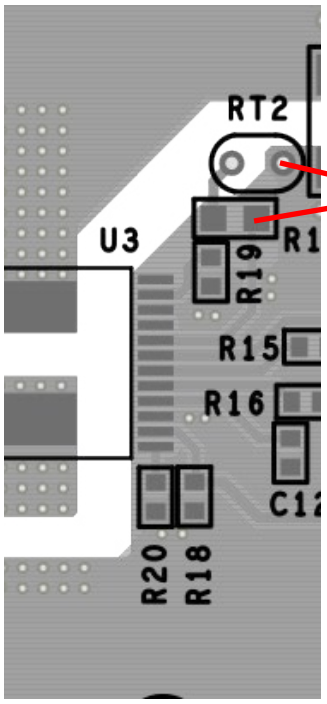
Signal Connectors to System Microcontroller
Connectors J1, J2, and J3 interface the three-phase inverter stage to the system microcontroller for PWM inputs, IPH outputs, and status update signals. External pull-up voltage levels VDD_U, VDD_V, and VDD_W for the FAULT interface are 3.3 V or 5 V.

PCB Design Guidelines

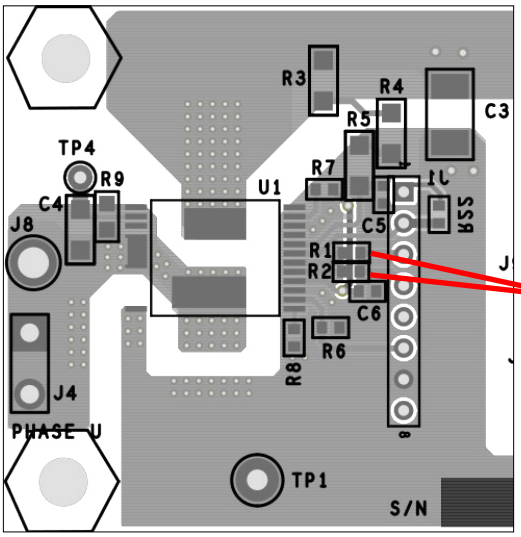
System Monitor Pin Circuit
When configured as a high-voltage sensing circuit, the divider resistors from the DC bus voltage to the SM pin are placed close to the IC with minimum trace lengths. An optional filter capacitor can be placed near the SM pin and returns to the SG pin.



When the SM pin is configured as a system level temperature monitor pin, the thermistor and series resistor are placed close to the SM pin.



Thermistor and Series Resistor Configured as System Temperature Monitor



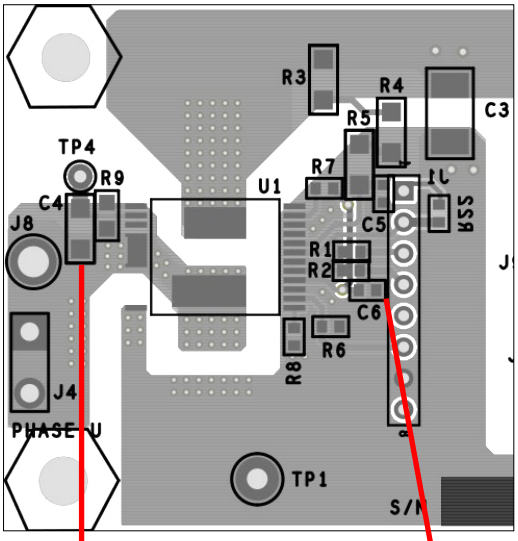
INL and INH Series Resistors

XL and XH Resistors

The XL resistor is placed near the XL pin and returns to the SG pin. The XH resistor is placed near the XH pin with a minimized loop area to the high-side return reference, the HB pin.

BPL and BPH Capacitor

The BPH/BPL decoupling capacitors are placed as close as possible to the BridgeSwitch BPH and BPL pins in order to maximize noise immunity and enable a stable supply to the IC. The BPL decoupling capacitor returns directly to the SG pin and the BPH decoupling capacitor returns directly to the HB pin.

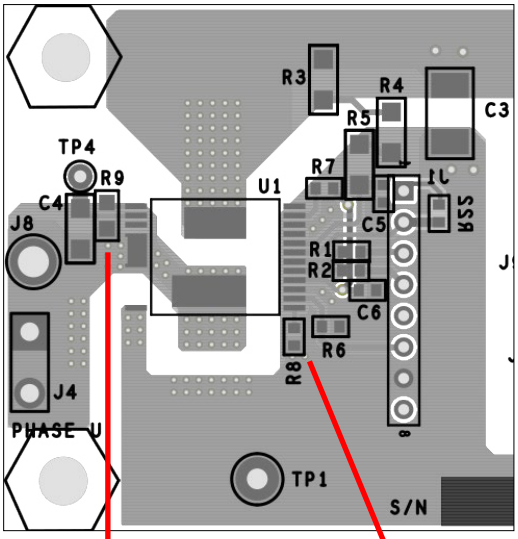


BPH Capacitor

BPL Capacitor

INL and /INH Input Resistors

The INL/INH resistors are placed as close as possible to the INL/INH pins. It is a good practice to minimize the lengths of PCB trace carrying the PWM signal from the microcontroller to the BridgeSwitch for good signal integrity.

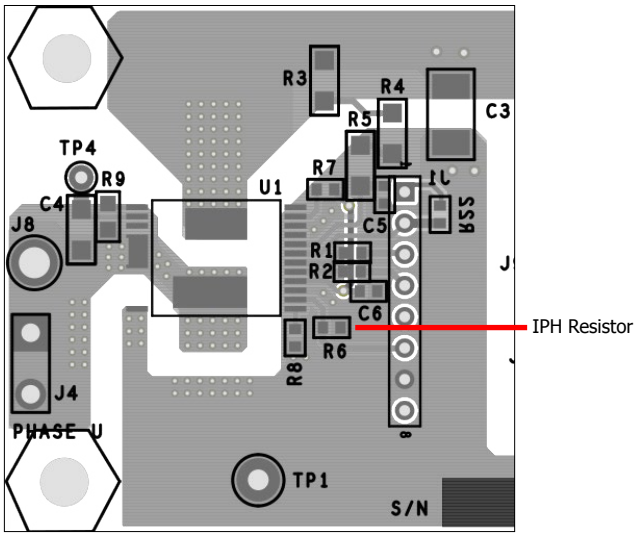


XH Resistor

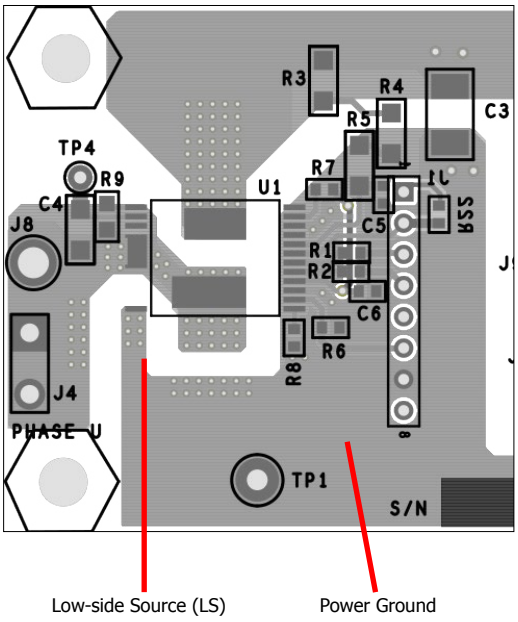
XL Resistor

IPH Resistors

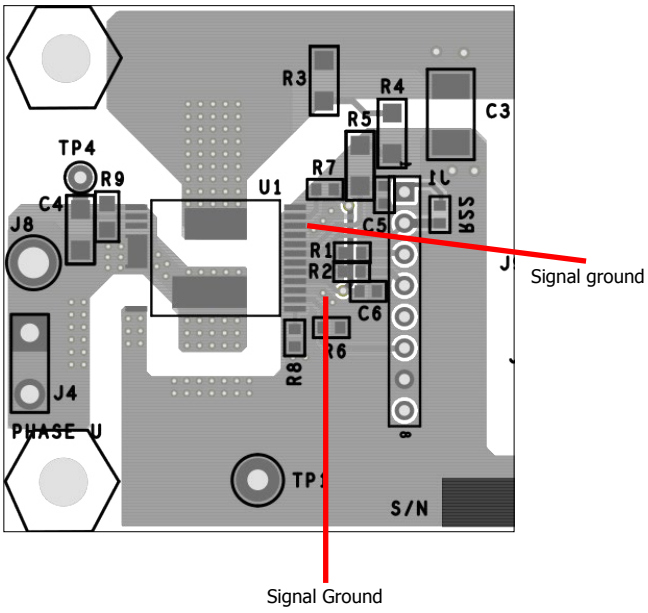
The IPH resistor is closely placed to the IPH pin. The length of PCB traces carrying the IPH signal to the system microcontroller should be kept as short as possible to avoid noise pick up and maintain signal integrity. The IPH resistor references to the SG pin.



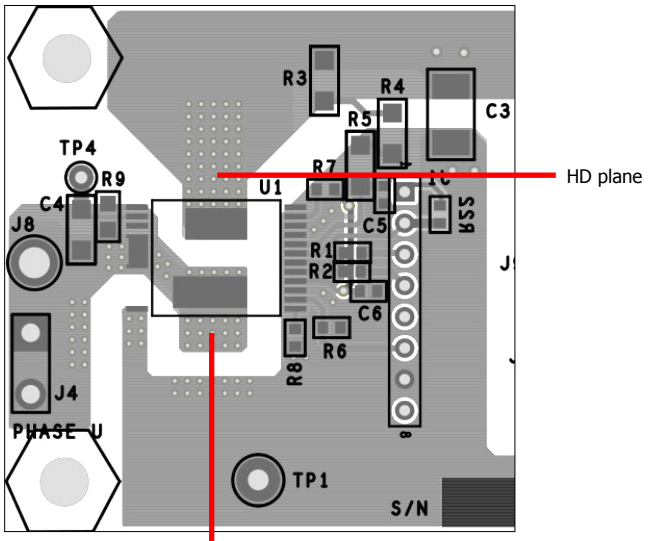
Signal Ground (SG)
Signal ground is connected directly to LS pin via a solid copper connect. This copper connect is separated from all logic and small signal circuit returning traces. All low-side control circuits and system microcontroller signals reference to the SG pin.

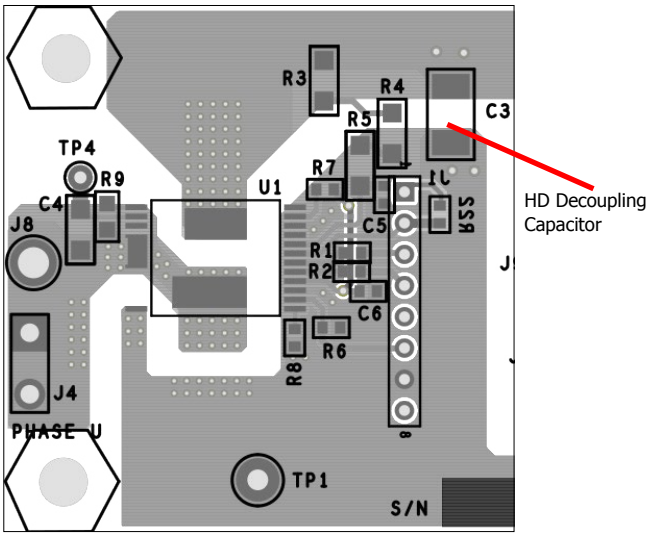


HD and HB Plane
The BridgeSwitch HD and HB exposed pad layout is configured to provide sufficient copper area for heat sinking.



Power Ground
The LS pin serves as the power ground. It is good practice to connect the LS pin to a ground plane, which connects to the bulk capacitor negative terminal and acts as ground shield.





DC Bus Decoupling Capacitor

The HD pin decoupling capacitor provides local high frequency decoupling of the DC bus voltage to BridgeSwitch. The capacitor is placed between DC input bus positive and negative planes and close to BridgeSwitch with required creepage and clearance distances taken into account.

Absolute Maximum Ratings[1,2]

HD Pin Voltage[2]: ..... -1.3 V to 600 V
HB Pin Voltage:..... -5 V to 600 V
DC Output Current[6,7]: BRD1X60C ..... 1.0 A
BRD1X61C..... 1.7 A
BRD1X63C ..... 3.0 A
BRD1X65C ..... 5.5 A
BPH Pin Voltage[3] ..... -0.3 V to 16.5 V
BPL/ID Pin Voltage..... -0.3 V to 16.5 V
BYPASS Pin Current..... 15 mA
XH PIN[3] Voltage ..... -0.3 V to 5.3 V
XL PIN Voltage..... -0.3 V to 5.3 V
FAULT/INL/INH Pin Voltage..... -0.3 V to 5.3 V
SM Pin Voltage..... -0.3 V to 5.3 V
SM Pin Current ..... 2 mA
IPH Pin Voltage..... -0.3 V to 5.3 V
IPH Pin Current..... 2 mA
LS Pin to SG Pin Voltage[5]..... ±0.33 V
Junction Temperature[7] ..... -40 °C to 150 °C
Storage Temperature ..... -65 °C to 150 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
2. All voltages referenced to low-side Source LS and signal ground SG except noted otherwise, T_A = 25 °C.
3. Referenced to Half-Bridge Connection HB, T_A = 25 °C.
4. 1/16" from case for 5 seconds.
5. With external current sense resistor in series with LS pin. T_J = -20 °C to 125 °C.
6. Continuous DC output current per FREDFET calculated at 25 °C case and 125 °C junction temperature.
7. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance (θ_{JA})[3]: inSOP-24C Package
BRD1X60C ..... 80 °C/W[1], 65 °C/W[2]
BRD1X61C..... 78 °C/W[1], 63 °C/W[2]
BRD1x63C..... 74 °C/W[1], 59 °C/W[2]
BRD1x65C..... 68 °C/W[1], 53 °C/W[2]

Notes:
1. Exposed pads soldered to 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
2. Exposed pads soldered to 1.0 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.
3. Both power switches each dissipating half the total power.

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Bypass Supply Function							
BYPASS Voltages	V_{BPL} V_{BPH}	T_J = 25 °C See Note D		13.8	14.5	15.2	V
BYPASS Shunt Regulator Voltages	$V_{BPL(SHUNT)}$ $V_{BPH(SHUNT)}$	I_{BPL} = I_{BPH} = 6 mA T_J = 25 °C See Note D		14.5	15.3	16.1	V
BYPASS Voltage Hysteresis	$V_{BPL(HYST)}$ $V_{BPH(HYST)}$	T_J = 25 °C		1.9	2.4	2.9	V
BYPASS Low-Side Supply Current	$I_{BPL(S1)}$	V_{BPL} = 14.5 V See Note A	$V_{INL} < V_{IL}$, $V_{/INH} > V_{IH}$			0.45	mA
	$I_{BPL(S2)}$		$V_{INL} > V_{IL}$, $V_{/INH} < V_{IH}$			0.80	
BYPASS High-Side Supply Current	$I_{BPH(S1)}$	V_{BPL} = 14.5 V See Note A	$V_{INL} < V_{IL}$, $V_{/INH} > V_{IH}$			0.42	mA
	$I_{BPH(S2)}$		$V_{INL} > V_{IL}$, $V_{/INH} < V_{IH}$			0.67	
BYPASS Low-Side Charge Current	$I_{CH1(LS)}$	T_J = 25 °C	V_{BPL} = 0 $V_{HD-to-LS}$ = 50 V	3.0			mA
	$I_{CH2(LS)}$		V_{BPL} = 14.5 V $V_{HD-to-LS}$ ≥ 100 V See Note C	1.7			
BYPASS High-Side Charge Current	$I_{CH1(HS)}$	V_{HB} = V_{LS} T_J = 25 °C	$V_{BPH-to-HB}$ = 0 $V_{BPH-to-HB}$ = 50 V	1.8			mA
	$I_{CH2(HS)}$		$V_{BPH-to-HB}$ = 14.5 V $V_{HD-to-HB}$ ≥ 100 V See Note C	10			

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
High-Side and Low-Side FREDFET Control							
INL Pull-Down Current	I_{INL}	V_{INL} = 2.5 V		0	1	1.15	µA
/INH Pull-Up Current	I_{INH}	V_{INH} = 2.5 V		-1.15	-1	0	
Input Voltage High	V_{IH}			2.5			V
Input Voltage Low	V_{IL}					0.8	V
Dead Time Low Off to High On	t_{DLH}	V_{BPL}= V_{BPH} = 14.5 V, V_{DS} = 325 V, I_D = 0.1 A See Figures 11 and 23		470	588	705	ns
Dead Time High Off to Low On	t_{DHL}	V_{BPL} = V_{BPH} = 14.5 V, V_{DS} = 325 V, I_D = 0.1 A See Figure 11		470	588	705	ns
Switching Time FREDFET Turn-On	t_{ON}	V_{BPL} = V_{BPH} = 14.5 V, V_{DS} = 325 V, I_D = 0.1 A /INH > V_{IH}, See Figure 23, Note C			0.7		µs
Switching Time FREDFET Turn-Off	t_{OFF}	V_{BPL} = V_{BPH} = 14.5 V, V_{DS} = 325 V, I_D = 0.1 A /INH > V_{IH}, See Figure 23, Note C			0.4		µs
Device Protection and System Level Monitoring							
FREDFET Junction Warning Temperature	T_{WA}	See Notes C		118	125	132	°C
FREDFET Junction Shutdown Temperature	T_{SD}	See Note C		143	150	157	°C
Current Limit Threshold	$I_{LIM(DEF)}$	R_{XL} = R_{XH} = 44.2 kΩ T_J = 25 °C di/dt =250 mA/µs	BRD1X60	0.665	0.700	0.735	A
			BRD1X61	1.425	1.500	1.575	
			BRD1X63	2.138	2.250	2.363	
			BRD1X65	2.850	3.000	3.150	
	$I_{LIM(RED)}$	R_{XL} = R_{XH} = 133 kΩ T_J = 25 °C di/dt =250 mA/µs	BRD1X60		0.305		
			BRD1X61		0.635		
			BRD1X63		0.921		
			BRD1X65		1.236		
Current Limit Delay Time	t_{ILD}	See Note B			150		ns
Leading Edge Blanking Time	t_{LEB}	See Note B		300			ns
Phase Current Output Gain	g_{IPH}	R_{XL} = R_{XH} = 44.2 kΩ, T_J = 25 °C $I_{D(LS)}$ = 0.75x $I_{LIM(DEF)}$ ON-time ≥ 2 µs	BRD1260	388	400	412	µA/A
			BRD1261	194	200	206	
			BRD1263	145	150	155	
			BRD1265	97	100	103	
Phase Current Output Delay Time	t_{IPH}	R_{XL} = R_{XH} = 44.2 kΩ , T_J = 25 °C, $I_{D(LS)}$ = 0.75x $I_{LIM(DEF)}$, di/dt = 250 mA/µs ON-time ≥ 2 µs, See Notes B, I			500		ns
XL/XH Pin Voltage	V_{XL} V_{XH}	V_{BPL} = V_{BPH} = 14.5 V R_{XL} = R_{XH} ≥ 44.2 kΩ T_J = 25 °C		1.15	1.20	1.25	V
XL/XH Pin Short-Circuit Current	$I_{XL(SC)}$ $I_{XH(SC)}$	T_J = 25 °C			-36	-30	µA
SM Pin Voltage	V_{SM}	SM Pin configured as bus voltage sense I_{SM} = 35 µA			1.6	1.9	V

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Device Protection and System Level Monitoring (cont.)							
High-Voltage Bus UV55 Threshold Current	I_{UV55}	T_J = 25 °C		18	20	22	µA
High-Voltage Bus UV70 Threshold Current	I_{UV70}	T_J = 25 °C		23	25	27	µA
High-Voltage Bus UV85 Threshold Current	I_{UV85}	T_J = 25 °C		28	30	32	µA
High-Voltage Bus UV100 Threshold Current	I_{UV100}	T_J = 25 °C		33	35	37	µA
High-Voltage Bus UV Delay Time	$t_{D(UV)}$	$I_{SM} = I_{UV100}$ See Note B			40		ms
High-Voltage Bus OV Threshold Current	I_{OV}	T_J = 25 °C		57	60	63	µA
High-Voltage Bus OV Delay Time	$t_{D(OV)}$	See Note C			80		µs
High-Voltage Bus OV Turn-Off Hysteresis	$I_{OV(HYST)}$				4		µA
System Over-Temperature Threshold	$V_{TM(TH)}$	SM Pin configured as external temperature sense See Figure 17		1.14	1.2	1.26	V
Over-Temperature Delay Time	$t_{D(TM)}$	See Note B and C			1		ms
Temperature Monitor Output Current	I_{TM}				96		µA
Temperature Monitor Current On-Time	$t_{ON(TM)}$	See Note C			10		ms
Temperature Monitor Current Duty Ratio	D_{ITM}	See Note B and C			1		%
Status Communication Bus							
INL High Time For Internal Communication	$t_{INLH(COM)}$	/INH > V_{IH} for ≥ t_{DHL} See Note G and Figure 24		2			µs
FAULT Pin Voltage High	V_{FAH}	R_{UP} = 267 Ω, V_{UP} = 3.3 V		2.5			V
FAULT Pin Voltage Low	V_{FAL}	R_{UP} = 267 Ω, V_{UP} = 3.3 V				0.8	V
FAULT Pin Current Sink	I_{FAS}	R_{UP} = 267 Ω, V_{UP} = 3.3 V, See Note F		3			mA
Device ID Time Period	t_{ID}	VFAULT < VFAL T_J = 25 °C	$V_{ID} = V_{BPL}$	38	40	42	µs
			V_{ID} = Floating	57	60	63	µs
			$V_{ID} = V_{SD}$	76	80	84	µs
Steady-State Time Period	t_{SS}	$V_{FAULT} > V_{FAH}$ See Note C			80		µs
Logic Bit 0 Time Period	t_{Bit0}	T_J = 25 °C		9.4	10	10.6	µs
Logic Bit 1 Time Period	t_{Bit1}	T_J = 25 °C		38	40	42	µs
Low Time Period	t_{LO}	T_J = 25 °C		9.4	10	10.6	µs

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Status Communication Bus (cont.)							
Idle Time Period	t_{IDLE}	See Note C			2x t_{SS}		µs
System Control ID Time Period	t_{SYSID}	V_{FAULT} < V_{FAL} See Note C			160		µs
Fault Latch Reset Time	t_{LARES}	V_{FAULT} < V_{FAL} See Note C			2x t_{SYSID}		µs
Power FREDFETs Channel and Diode							
DRAIN to SOURCE Breakdown Voltage	BV_{DSS}	I_D = 250 µA, T_J = 25 °C		600			V
High-Side DRAIN Supply Voltage	$V_{HD(START)}$			50			V
OFF-State Drain Leakage Current	I_{DSS}	V_{DS} = 540 V T_J = 100 °C See Note H				65	µA
ON-State DRAIN-to-SOURCE Resistance	$R_{DS(ON)}$	BRD1X60 V_{BPH} = V_{BPL} = 14.5 V I_D = 0.1 × $I_{LIM(DEF)}$	T_J = 25 °C		6.84	8.21	Ω
			T_J = 100 °C		9.65	11.58	
		BRD1X61 V_{BPH} = V_{BPL} = 14.5 V I_D = 0.1 × $I_{LIM(DEF)}$	T_J = 25 °C		2.95	3.54	
			T_J = 100 °C		4.28	5.14	
		BRD1X63 V_{BPH} = V_{BPL} = 14.5 V I_D = 0.1 × $I_{LIM(DEF)}$	T_J = 25 °C		1.53	1.84	
			T_J = 100 °C		2.11	2.53	
		BRD1X65 V_{BPH} = V_{BPL} = 14.5 V I_D = 0.1 × $I_{LIM(DEF)}$	T_J = 25 °C		0.83	0.99	
			T_J = 100 °C		1.13	1.35	
DRAIN Voltage Fall Time	t_{VF}	V_{HVBUS} = 325 V See Figure 23, Notes C and E			115		ns
DRAIN Voltage Rise Time	t_{VR}	V_{HVBUS} = 325 V See Figure 23, Notes C and E			95		ns
Diode Forward Voltage	V_{SD}	BRD1X60, I_S = 0.5 A See Note C	T_J = 25 °C		1.60		V
			T_J = 100 °C		1.42		
		BRD1X61, I_S = 0.7 A See Note C	T_J = 25 °C		1.49		
			T_J = 100 °C		1.22		
		BRD1X63, I_S = 1 A See Note C	T_J = 25 °C		1.46		
			T_J = 100 °C		1.13		
		BRD1X65, I_S = 1 A See Note C	T_J = 25 °C		1.09		
			T_J = 100 °C		0.91		

Parameter	Symbol	Conditions Low-Side SOURCE = 0 V T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Power FREDFETs Channel and Diode (cont.)							
Diode Reverse Recovery Time	t_{RR}	V_R = 400 V T_J = 125 °C See Note C	BRD1X60, I_S = 0.5 A di/dt = 50 A/µs		120		ns
			BRD1X61, I_S = 0.75 A di/dt = 50 A/µs		100		
			BRD1X63, I_S = 1 A di/dt = 50 A/µs		130		
			BRD1X65, I_S = 1 A di/dt = 75 A/µs		120		

NOTES:

A. Total current consumption is the sum of $I_{BPL(S1)}$ for $I_{BPH(S1)}$ and I_{DSS} when both FREDFETs are off and the sum of $I_{BPL(S2)}$ or $I_{BPH(S2)}$ and I_{DSS} when one FREDFET is switching (20 kHz maximum commutation frequency assumed).
B. Guaranteed by design. Not tested in production.
C. Guaranteed through characterization. Not tested in production.
D. Bypass shunt regulator voltage exceeds bypass voltage guaranteed by design.
E. Tested in a typical 3-phase inverter application circuit. Normally limited by internal circuitry.
F. Measured indirectly during device timing tests.
G. Assumes control input /INH was high for an idling period of $t_{IDLE} > t_{DHL}$. The required minimum INL high time for internal communication increases by $t_{DHL} - t_{IDLE}$ if $t_{IDLE} < t_{DHL}$ (refer to Figure 24).
H. Controller BYPASS pin voltage at V_{BPL} + 0.1 V or V_{BPH} + 0.1 V during FREDFET off-state.
I. IPH output connected to a 10 kΩ resistor in parallel to series RC network of 8 kΩ and 7 pF.

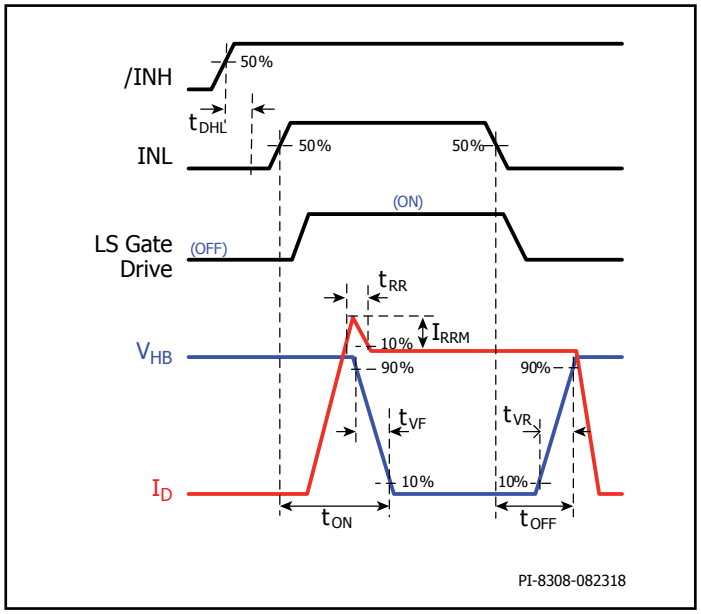


Figure 23. Low-Side FREDFET Switching Timing.

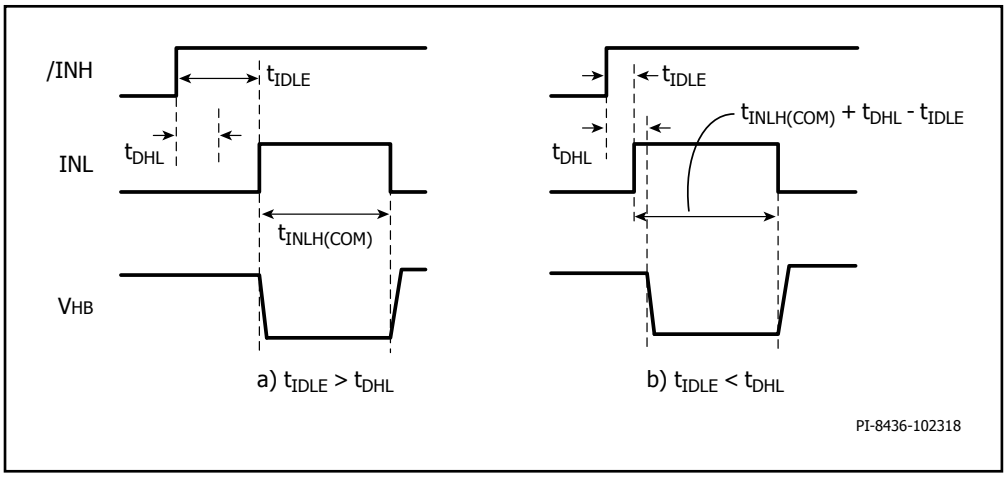


Figure 24. Minimum INL High Time Required for Device Internal High-Side Status Update a) $t_{IDLE} > t_{DHL}$ b) $t_{IDLE} < t_{DHL}$.

Typical Performance Characteristics

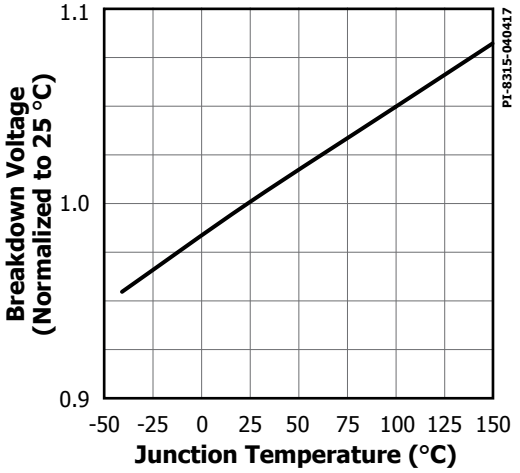


Figure 25. Power FREDFET Breakdown vs. Temperature.

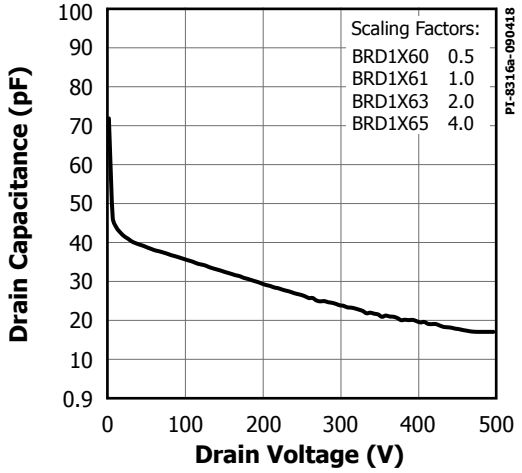


Figure 26. Power FREDFET C_{oss} vs. Voltage.

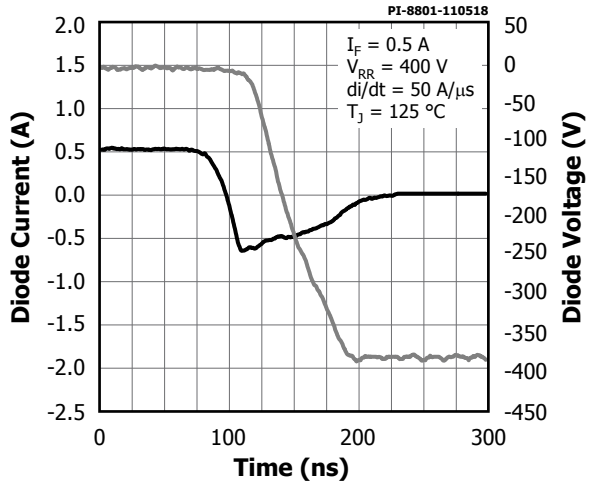


Figure 27. Typical Diode Reverse Recovery (BRD1X60).

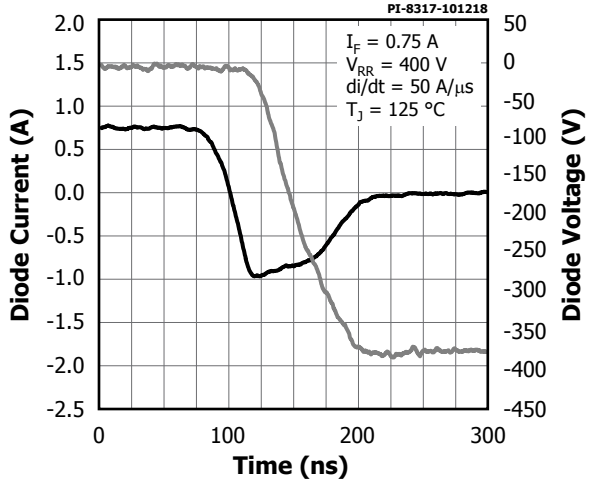


Figure 28. Typical Diode Reverse Recovery (BRD1X61).

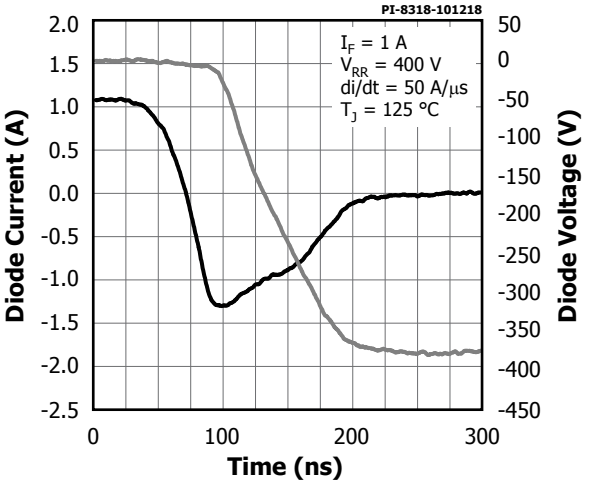


Figure 29. Typical Diode Reverse Recovery (BRD1X63).

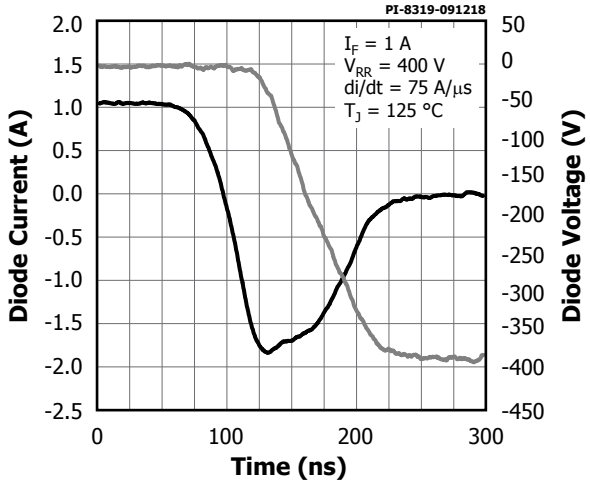


Figure 30. Typical Diode Reverse Recovery (BRD1X65).

Typical Performance Characteristics (cont.)

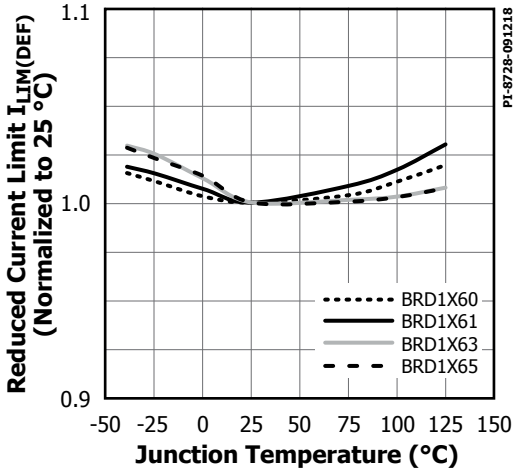


Figure 31. High-Side Current Limit vs. Temperature.

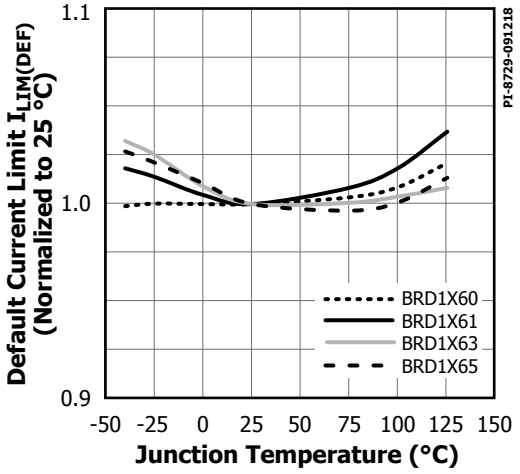


Figure 32. Low-Side Current Limit vs. Temperature.

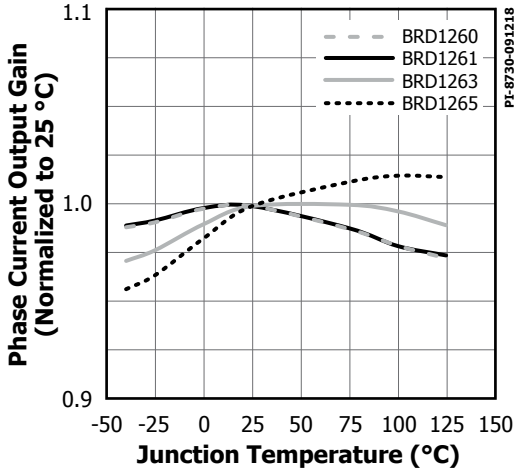


Figure 33. Phase Current Output Gain vs. Temperature.

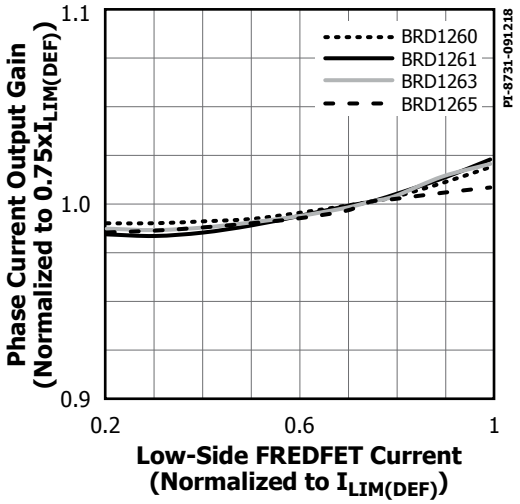


Figure 34. Phase Current Output Gain vs. Low-Side FREDFET Current.

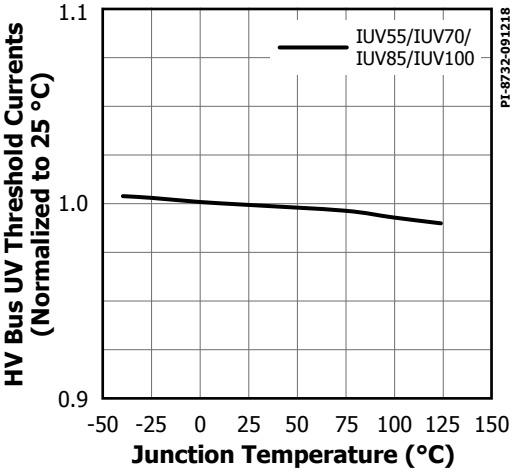


Figure 35. HV Bus UV Threshold Currents vs. Temperature.

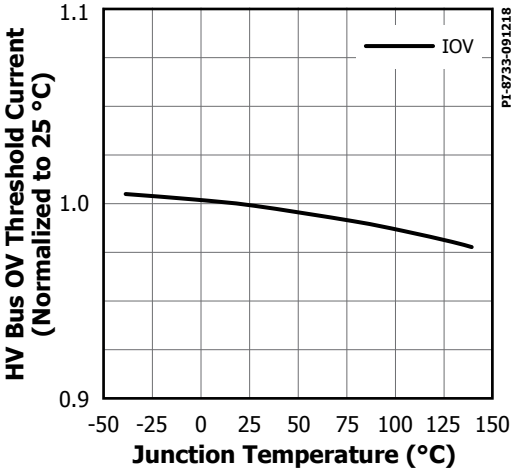
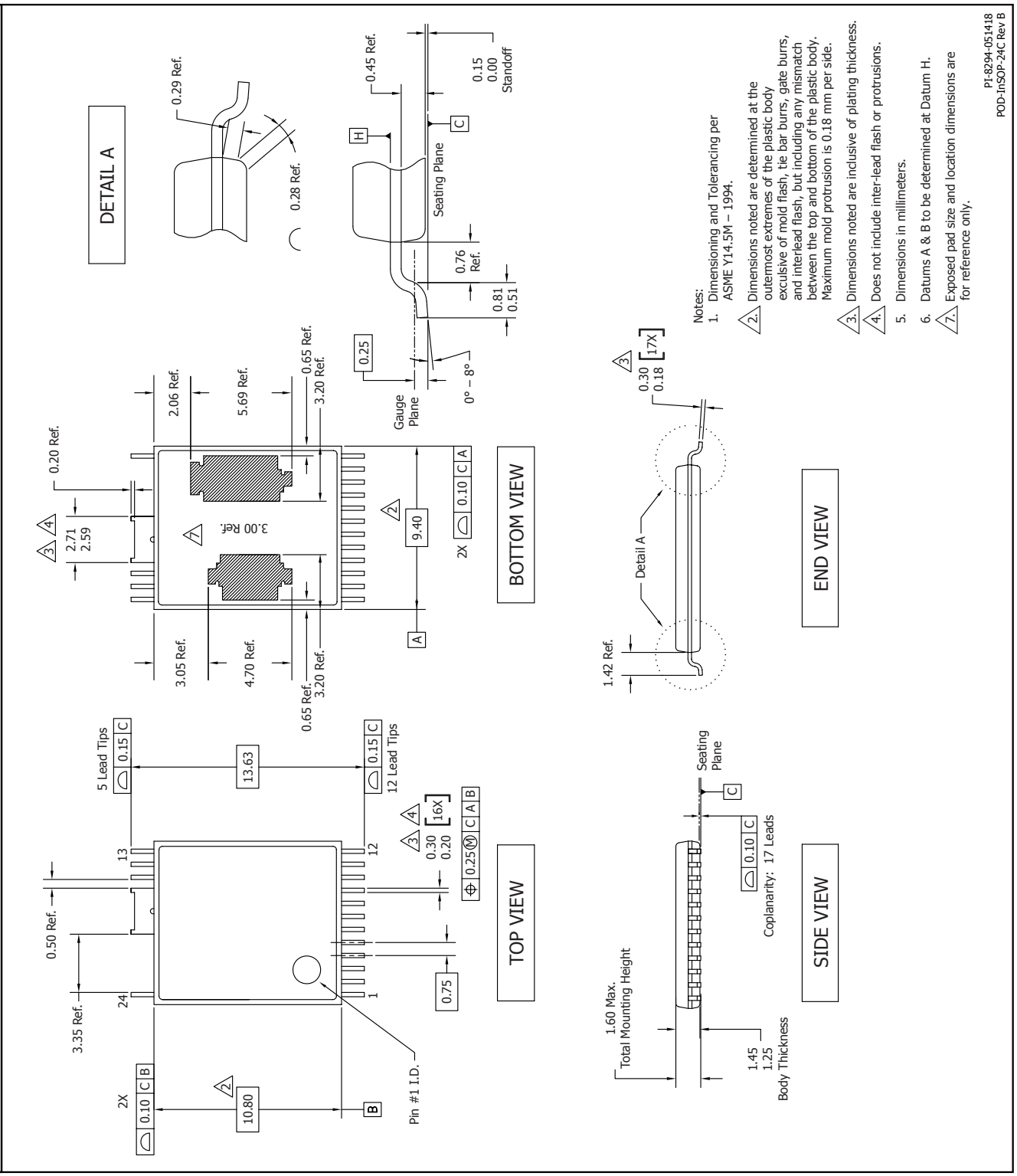


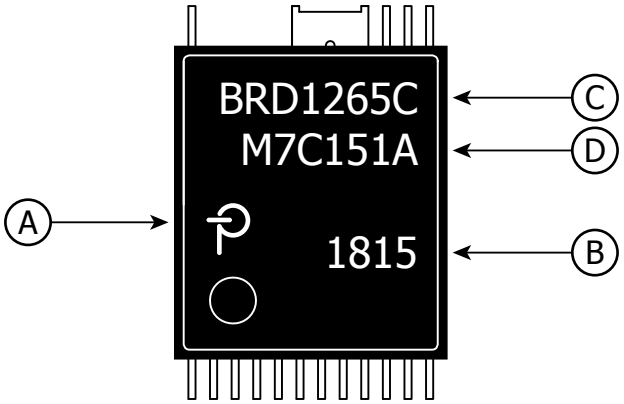
Figure 36. HV Bus OV Threshold Current vs. Temperature.

InSOP-24C


DETAIL A
0.29 Ref.
0.28 Ref.
0.45 Ref.
0.15
0.00
Standoff
Seating Plane
0.76
Ref.
0.81
0.51
0.25
Gauge
Plane
0° – 8°
0.20 Ref.
2.71
2.59
3.00 Ref.
2.06 Ref.
5.69 Ref.
0.65 Ref.
3.20 Ref.
9.40
2X 0.10 C A
BOTTOM VIEW
3.05 Ref.
4.70 Ref.
0.65 Ref.
3.20 Ref.
0.30
0.18 [17X]
Detail A
1.42 Ref.
END VIEW
Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. Exposed pad size and location dimensions are for reference only.
PI-8294-051418
POD-InSOP-24C Rev B
0.50 Ref.
3.35 Ref.
5 Lead Tips
0.15 C
13.63
12 Lead Tips
0.30
0.20 [16X]
0.25 M C A B
0.75
10.80
2X 0.10 C B
Pin #1 I.D.
TOP VIEW
1.60 Max.
Total Mounting Height
Seating
Plane
0.10 C
Coplanarity: 17 Leads
1.45
1.25
Body Thickness
SIDE VIEW

PACKAGE MARKING

InSOP-24C



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-8836-100118

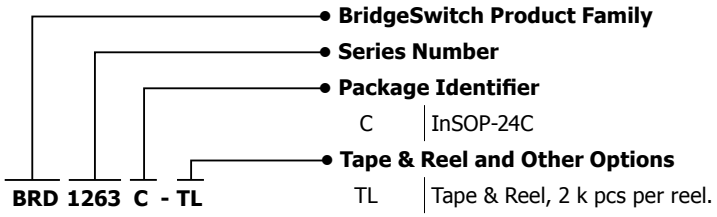
Part Ordering and MSL Table

Product / Part Number	MSL Rating
BRD1160C	3
BRD1161C	3
BRD1163C	3
BRD1165C	3
BRD1260C	3
BRD1261C	3
BRD1263C	3
BRD1265C	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2 kV on all pins except HD and HB pins > ±1.5 kV on HD and HB pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Notes

Revision	Notes	Date
E	Code A release.	10/18
F	Updated Figure 6 and 2nd paragraph under BYPASS LOW-SIDE Pin and HIGH-SIDE Pin Regulator section on page 5. Updated Figure 27 and edited text from middle row of Results column in ESD and Latch-Up Table.	11/18

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