10 W, GaN Power Amplifier, 2.7 GHz to 3.8 GHz

Data Sheet **HMC1114**

FEATURES

- High saturated output power (P_{SAT}): 41.5 dBm typical
- High small signal gain: 35 dB typical
- High power gain for saturated output power: 25.5 dB typical
- Bandwidth: 2.7 GHz to 3.8 GHz
- High power added efficiency (PAE): 54% typical
- High output IP3: 44 dBm typical
- Supply voltage: V_{DD} = 28 V at 150 mA
- 32-lead, 5 mm × 5 mm LFCSP_CAV package

APPLICATIONS

- Extended battery operation for public mobile radios
- Power amplifier stage for wireless infrastructure
- Test and measurement equipment
- Commercial and military radars
- General-purpose transmitter amplification

FUNCTIONAL BLOCK DIAGRAM

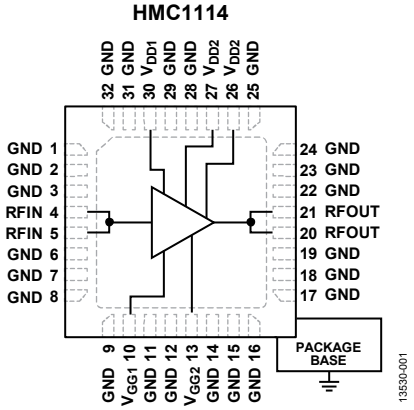

Figure 1.

GENERAL DESCRIPTION

The HMC1114 is a gallium nitride (GaN), broadband power amplifier, delivering 10 W with more than 50% power added efficiency (PAE) across a bandwidth of 2.7 GHz to 3.8 GHz. The HMC1114 provides ±0.5 dB gain flatness.

The HMC1114 is ideal for pulsed or continuous wave (CW) applications such as wireless infrastructure, radar, public mobile radio, and general-purpose amplification.

The HMC1114 is housed in a compact LFCSP_CAV package.

Rev. A

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REVISION HISTORY

3/2017—Rev. 0 to Rev. A

Changed EVL1HMC1114LP5D to EV1HMC1114LP5D ..... Throughout
Changes to Ordering Guide 15

9/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = 28 V, I_{DQ} = 150 mA, frequency range = 2.7 GHz to 3.2 GHz, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		2.7		3.2	GHz	
GAIN						
Small Signal Gain		32	35		dB	
Gain Flatness			±0.5		dB	
Power Gain for 4 dB Compression			29		dB	
Power Gain for Saturated Output Power			25.5		dB	Measurement taken at P_{IN} = 16 dBm
RETURN LOSS						
Input			14		dB	
Output			11		dB	
POWER						
Output Power for 4 dB Compression	P4dB		39		dBm	
Saturated Output Power	P_{SAT}		41.5		dBm	Measurement taken at P_{IN} = 16 dBm
Power Added Efficiency	PAE		54		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		44			Measurement taken at P_{OUT}/tone = 30 dBm
TARGET QUIESCENT CURRENT	I_{DQ}		150		mA	Adjust the gate control voltage (V_{GG1}, V_{GG2}) between −8 V and 0 V to achieve an I_{DQ} = 150 mA typical

T_A = 25°C, V_{DD} = 28 V, I_{DQ} = 150 mA, frequency range = 3.2 GHz to 3.8 GHz, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3.2		3.8	GHz	
GAIN						
Small Signal Gain		29	32		dB	
Gain Flatness			±1		dB	
Power Gain for 4 dB Compression			28		dB	
Power Gain for Saturated Output Power			25		dB	Measurement taken at P_{IN} = 16 dBm
RETURN LOSS						
Input			25		dB	
Output			9		dB	
POWER						
Output Power for 4 dB Compression	P4dB		40		dBm	
Saturated Output Power	P_{SAT}		40.5		dBm	Measurement taken at P_{IN} = 16 dBm
Power Added Efficiency	PAE		53		%	
OUTPUT THIRD-ORDER INTERCEPT	IP3		44			Measurement taken at P_{OUT}/tone = 30 dBm
TARGET QUIESCENT CURRENT	I_{DQ}		150		mA	Adjust the gate control voltage (V_{GG1}, V_{GG2}) between −8 V and 0 V to achieve an I_{DQ} = 150 mA typical

TOTAL SUPPLY CURRENT BY V_{DD}

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT	I_{DQ}					Adjust V_{GG1}, V_{GG2} to achieve an I_{DQ} = 150 mA typical
V_{DD} = 25 V			150		mA	
V_{DD} = 28 V			150		mA	
V_{DD} = 32 V			150		mA	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD1}, V_{DD2})	35 V dc
Gate Bias Voltage (V_{GG1}, V_{GG2})	−8 V to 0 V dc
RF Input Power (RFIN)	30 dBm
Maximum Forward Gate Current	4 mA
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 227 mW/°C Above 120°C)	24 W
Thermal Resistance, Junction to Back of Paddle	4.4°C/W
Channel Temperature	225°C
Maximum Peak Reflow Temperature (MSL3)[1]	260°C
Storage Temperature Range	−40°C to +125°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1A, passed 250 V

[1] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

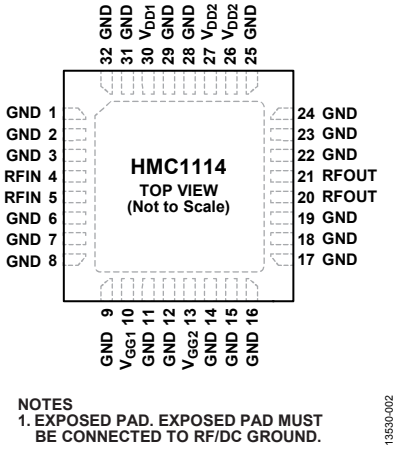

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 3, 6 to 9, 11, 12, 14 to 19, 22 to 25, 28, 29, 31, 32	GND	Ground. These pins and the package bottom (EPAD) must be connected to RF/dc ground. See Figure 3 for the GND interface schematic.
4, 5	RFIN	RF Input. These pins are dc-coupled and matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
10, 13	V_{GG1}, V_{GG2}	Gate Control Voltage Pins. External bypass capacitors of 1 µF and 10 µF are required. See Figure 5 for the V_{GG1} and V_{GG2} interface schematic.
20, 21	RFOUT	RF Output. These pins are ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
26, 27, 30	V_{DD1}, V_{DD2}	Drain Bias Pins for the Amplifier. External bypass capacitors of 100 pF, 1 µF, and 10 µF are required. See Figure 7 for the V_{DD1} and V_{DD2} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

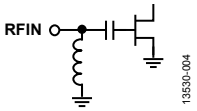

Figure 4. RFIN Interface

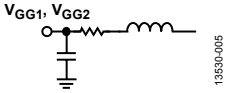

Figure 5. V_{GG1} and V_{GG2} Interface

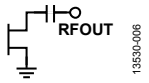

Figure 6. RFOUT Interface

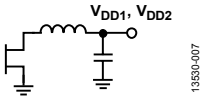

Figure 7. V_{DD1} and V_{DD2} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

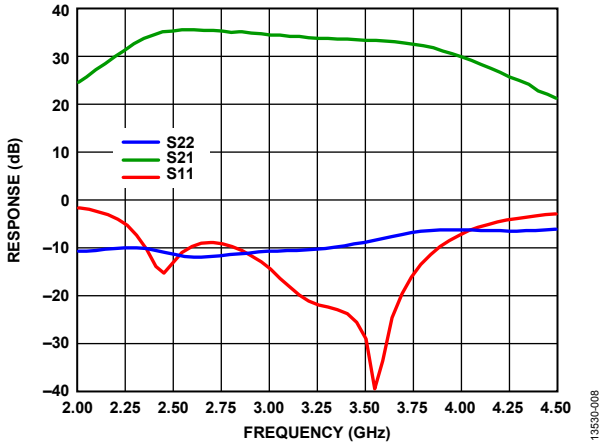

Figure 8. Response (Gain and Return Loss) vs. Frequency

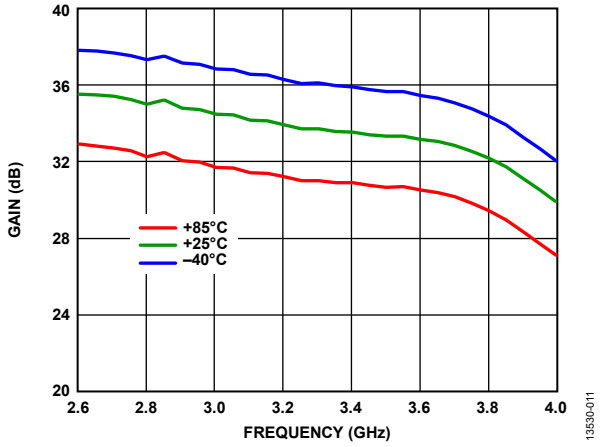

Figure 11. Gain vs. Frequency at Various Temperatures

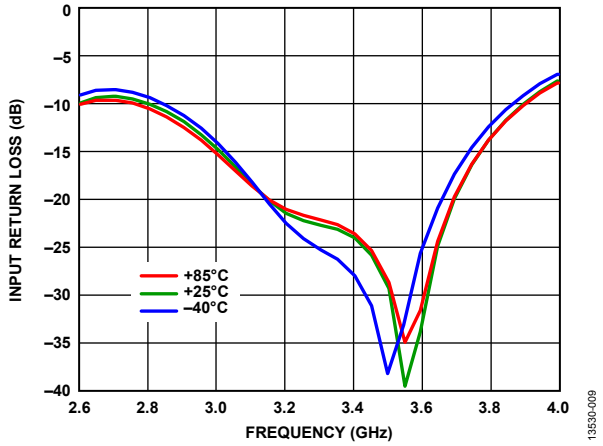

Figure 9. Input Return Loss vs. Frequency at Various Temperatures

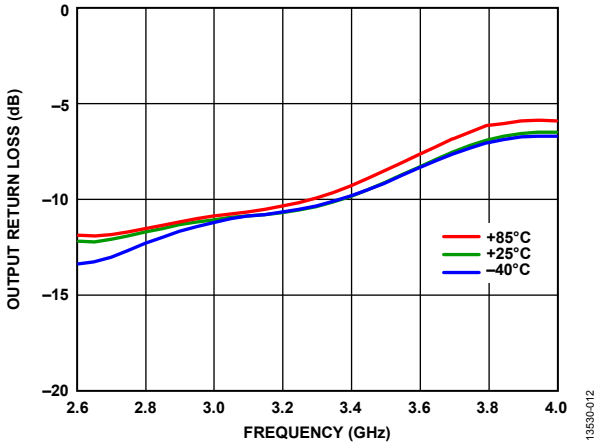

Figure 12. Output Return Loss vs. Frequency at Various Temperatures

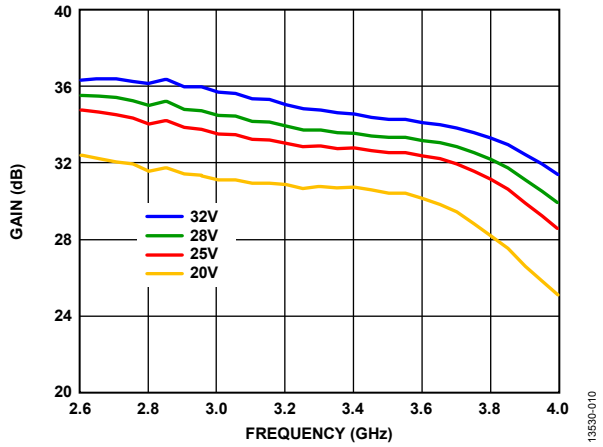

Figure 10. Gain vs. Frequency at Various Supply Voltages

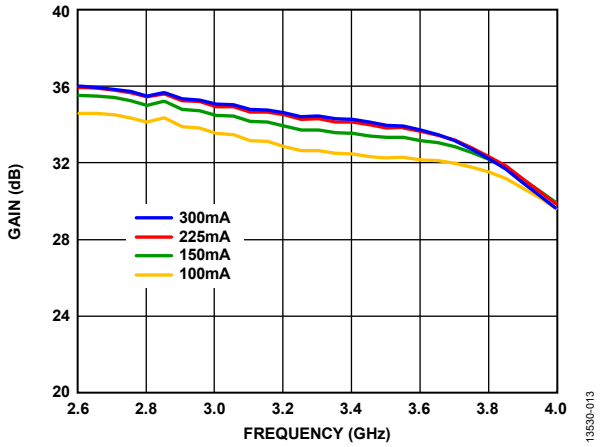

Figure 13. Gain vs. Frequency at Various Supply Currents

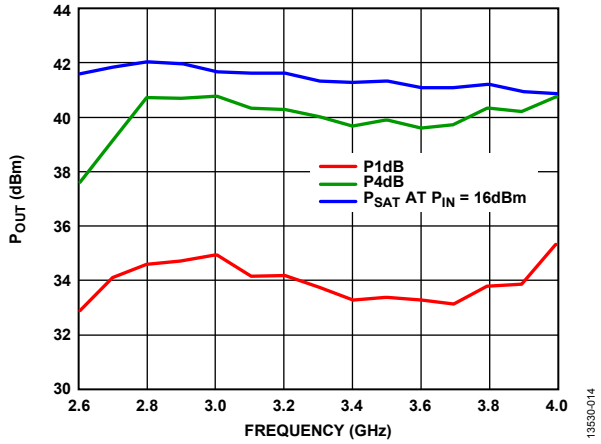

Figure 14. Output Power (P_{OUT}) vs. Frequency, Measurement Taken at P_{IN} = 16 dBm

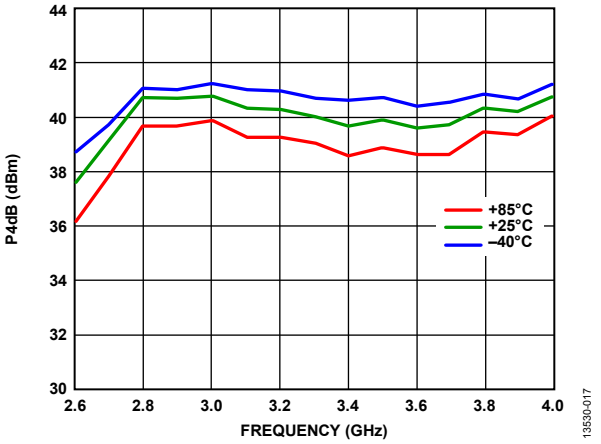

Figure 17. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Temperatures

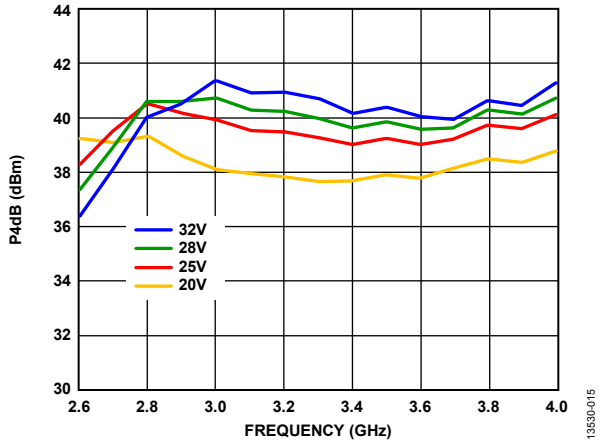

Figure 15. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Voltages

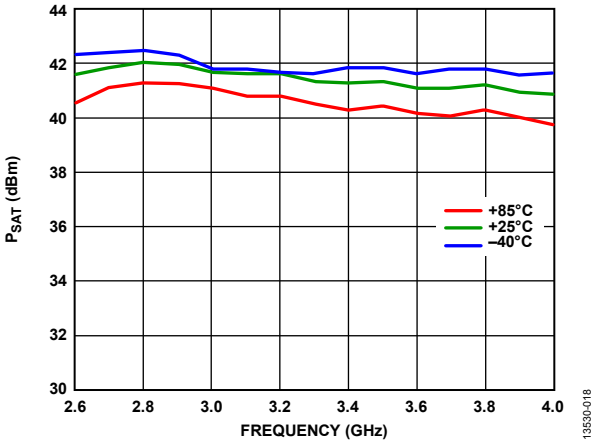

Figure 18. Saturated Output Power (P_{SAT}) vs. Frequency at Various Temperatures, Measurement Taken at P_{IN} = 16 dBm

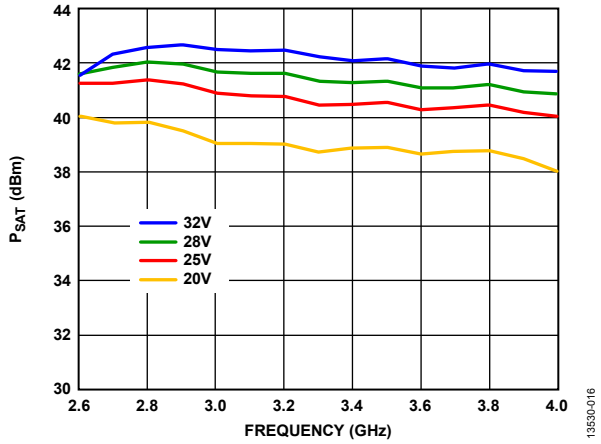

Figure 16. Saturated Output Power (P_{SAT}) vs. Frequency at Various Supply Voltages, Measurement Taken at P_{IN} = 16 dBm

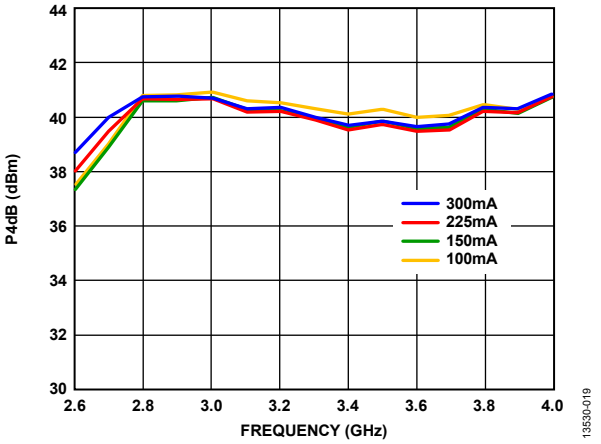

Figure 19. Output Power for 4 dB Compression (P4dB) vs. Frequency at Various Supply Currents

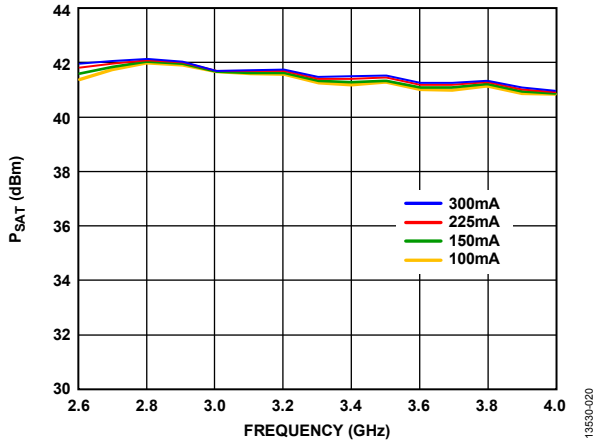

Figure 20. Saturated Output Power (P_{SAT}) vs. Frequency at Various Supply Currents, Measurement Taken at P_{IN} = 16 dBm

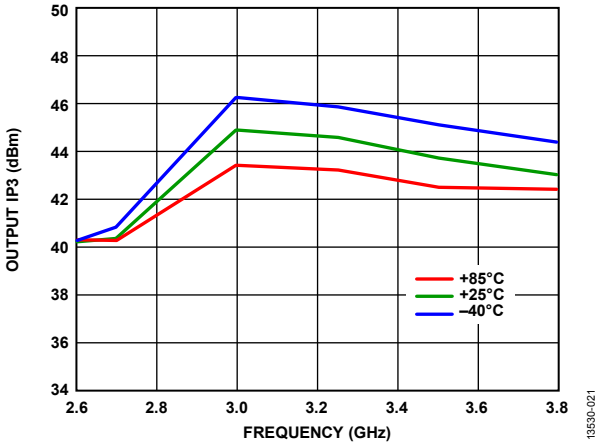

Figure 21. Output Third-Order Intercept (IP3) vs. Frequency at Various Temperatures, P_{OUT}/Tone = 30 dBm

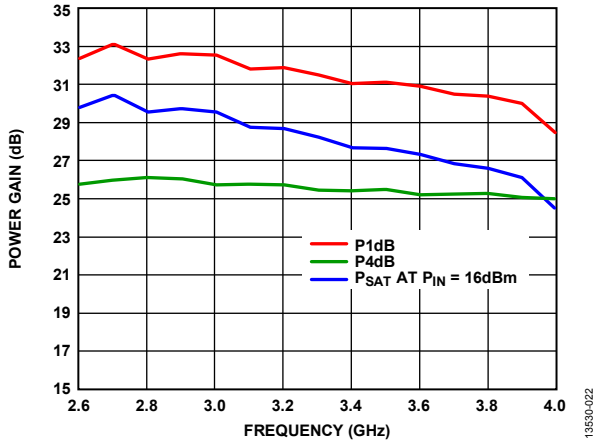

Figure 22. Power Gain vs. Frequency

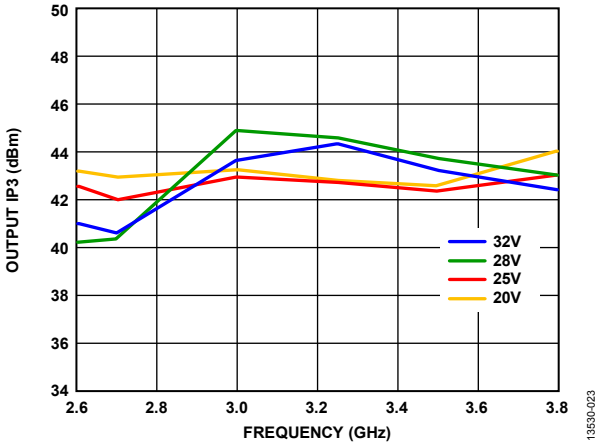

Figure 23. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Voltages, P_{OUT}/Tone = 30 dBm

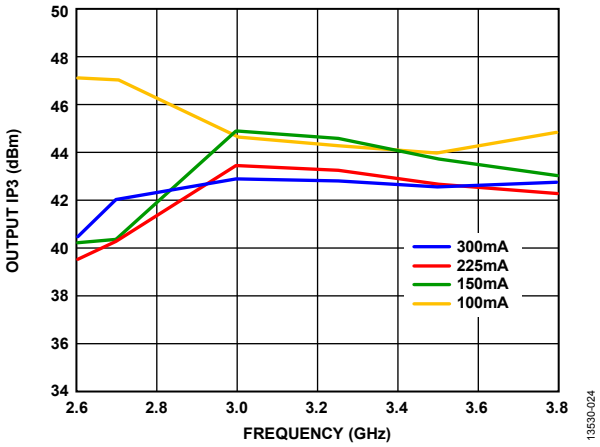

Figure 24. Output Third-Order Intercept (IP3) vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 30 dBm

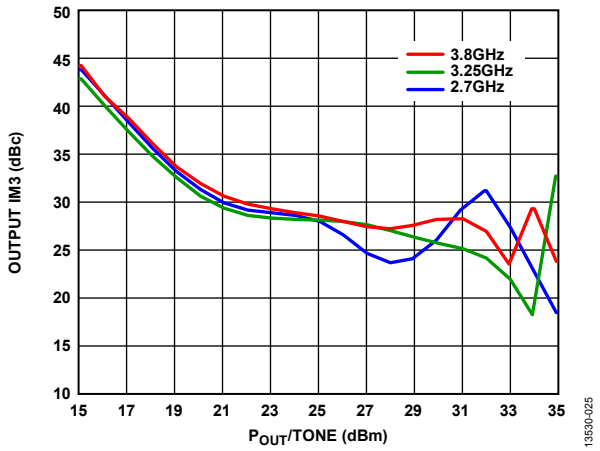

Figure 25. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 20 V

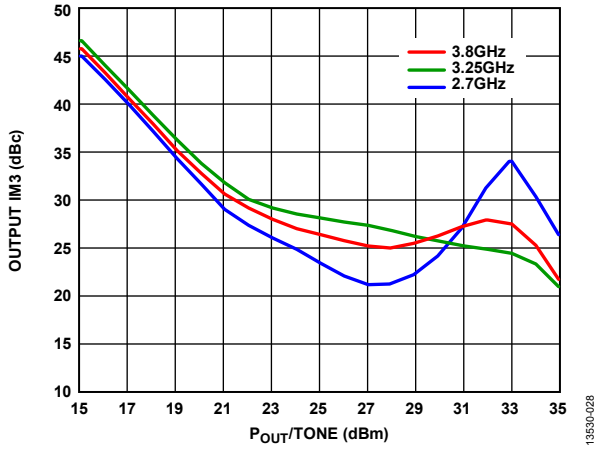

Figure 26. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 25 V

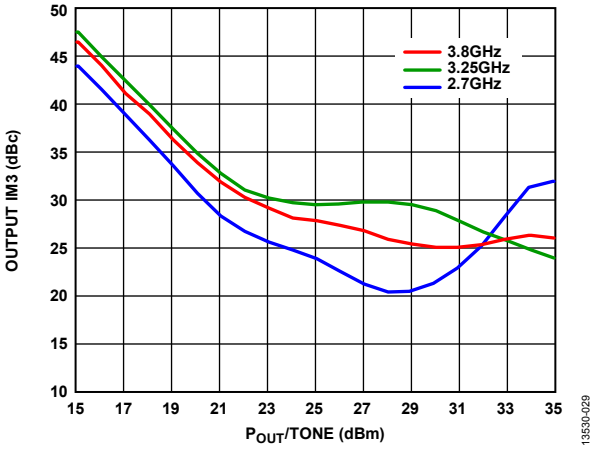

Figure 29. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 32 V

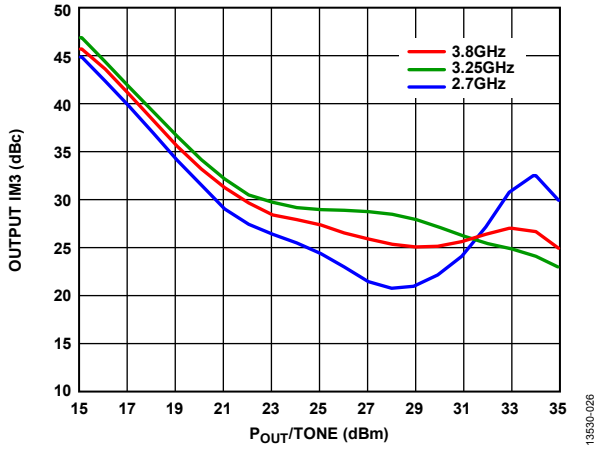

Figure 27. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 28 V

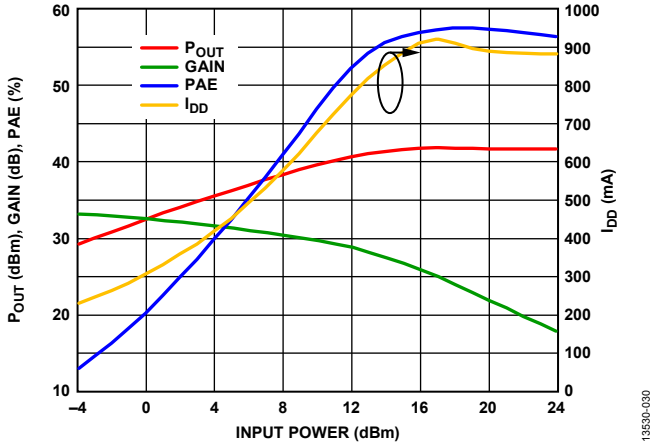

Figure 30. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), and Supply Current (I_{DD}) vs. Input Power at 3.2 GHz

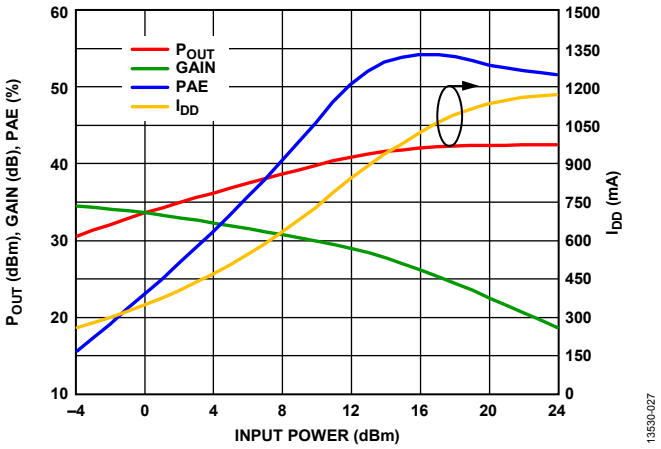

Figure 28. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), and Supply Current (I_{DD}) vs. Input Power at 2.7 GHz

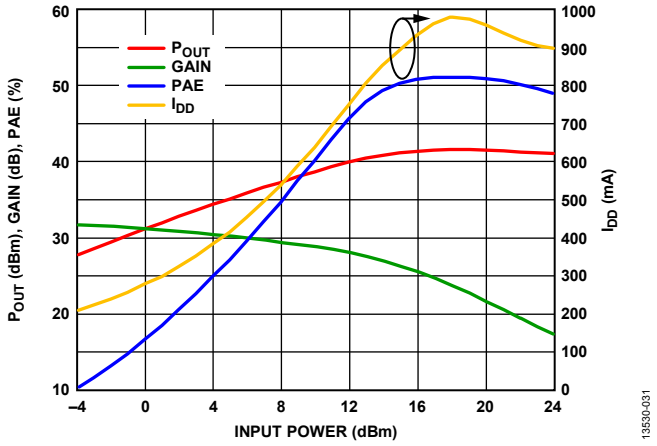

Figure 31. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), and Supply Current (I_{DD}) vs. Input Power at 3.8 GHz

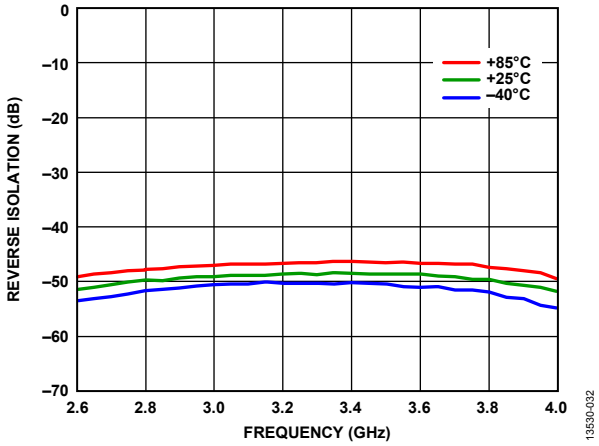

Figure 32. Reverse Isolation vs. Frequency at Various Temperatures

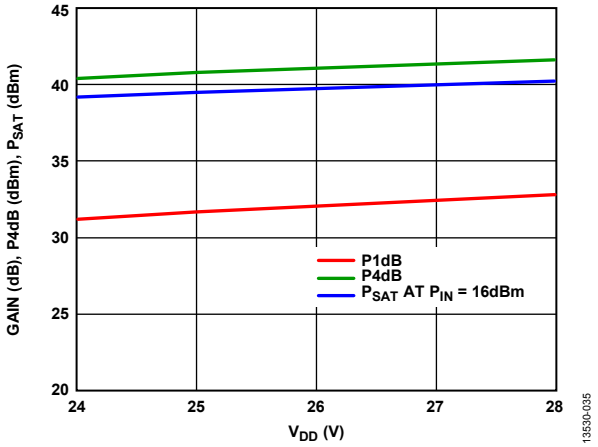

Figure 35. Gain, P4dB, and P_{SAT} vs. Supply Voltage (V_{DD}) at 3.2 GHz

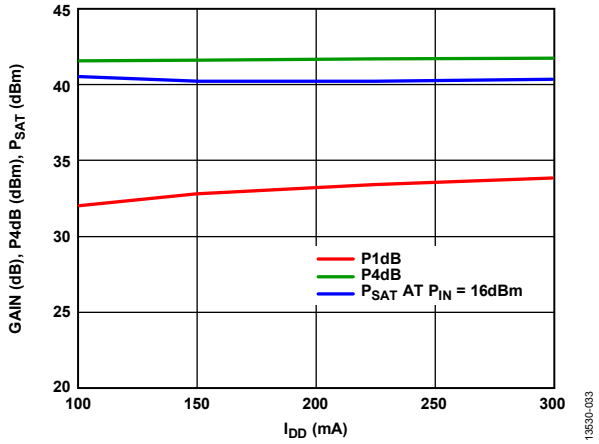

Figure 33. Gain, Output Power for 4 dB Compression (P4dB), and Saturated Output Power (P_{SAT}) vs. Supply Current (I_{DD})

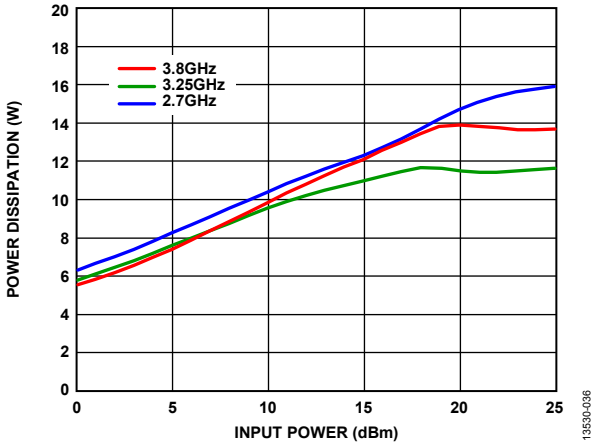

Figure 36. Power Dissipation vs. Input Power at 85°C

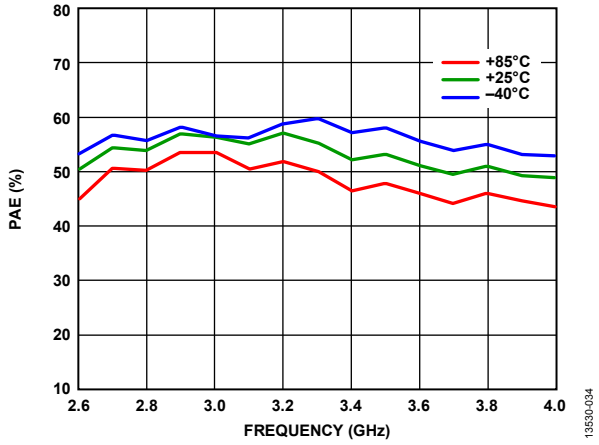

Figure 34. Power Added Efficiency (PAE) vs. Frequency at Various Temperatures, P_{IN} = 16 dBm

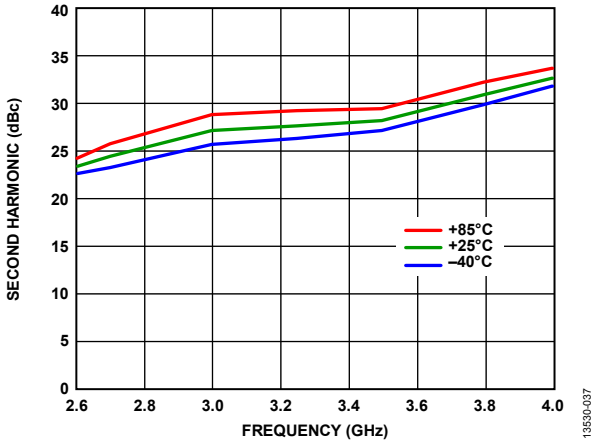

Figure 37. Second Harmonic vs. Frequency at Various Temperatures, P_{OUT} = 30 dBm

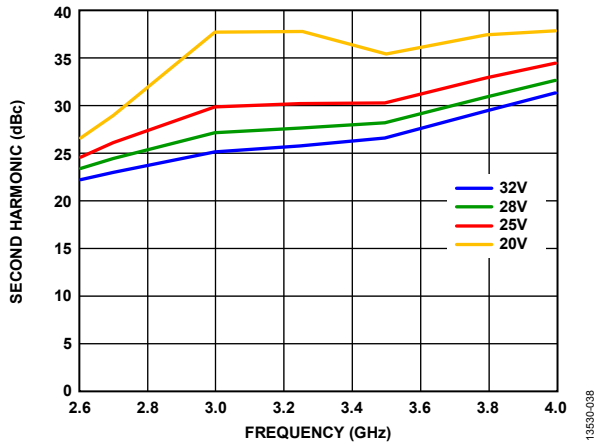

Figure 38. Second Harmonic vs. Frequency at Various Supply Voltages, P_{OUT} = 30 dBm

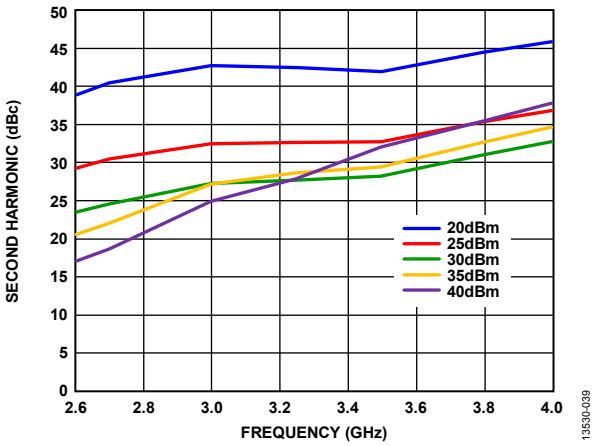

Figure 39. Second Harmonic vs. Frequency at Various Output Powers

THEORY OF OPERATION

The HMC1114 is a 10 W, gallium nitride (GaN), power amplifier that consists of two gain stages in series, and the basic block diagram for the amplifier is shown in Figure 40.

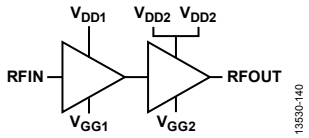

Figure 40. Basic Block Diagram

The recommended dc bias conditions put the device in deep Class AB operation, resulting in high P_{SAT} (41.5 dBm typical) at improved levels of PAE (54% typical). The voltage applied to the V_{GG1} and V_{GG2} pads sets the gate bias of the field effect transistors (FETs), providing control of the drain current. For this reason, the application of a bias voltage to the V_{GG1} and V_{GG2} pads is required and not optional.

The HMC1114 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the 2.7 GHz to 3.8 GHz frequency range. Consequently, it can directly insert into a 50 Ω system with no required impedance matching circuitry, which also means that multiple HMC1114 amplifiers can be cascaded back to back without the need for external matching circuitry. The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

Note that it is critical to supply very low inductance ground connections to the GND pins and the package base exposed pad to ensure stable operation. To achieve optimal performance from the HMC1114 and prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Figure 41 shows the basic connections for operating the HMC1114. The RFIN port is dc-coupled. An appropriate valued external dc block capacitor is required at RFIN port. The RFOUT port has on-chip dc block capacitors that eliminate the need for external ac coupling capacitors.

RECOMMENDED BIAS SEQUENCE

During Power-Up

The recommended bias sequence during power-up is the following:

1. Connect to ground.
2. Set V_{GG1} and V_{GG2} to −8 V.
3. Set V_{DD1} and V_{DD2} to 28 V.
4. Increase V_{GG1} and V_{GG2} to achieve a typical I_{DQ} = 150 mA.
5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is the following:

1. Turn off the RF signal.
2. Decrease V_{GG1} to −8 V to achieve a typical I_{DQ} = 0 mA.
3. Decrease V_{DD1} and V_{DD2} to 0 V.
4. Increase V_{GG1} to 0 V.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 41) on the evaluation board (see Figure 42) and biased per the conditions in the Recommended Bias Sequence section. The V_{DD1} and two V_{DD2} pins are connected together. Similarly, the V_{GG1} and V_{GG2} pins are also connected together. The bias conditions shown in the Recommended Bias Sequence section are the operating points recommended to optimize the overall performance. Operation using other bias conditions may provide performance that differs from what is in Table 1 and Table 2. Increasing the V_{DD1} and V_{DD2} levels typically increase gain and P_{SAT} at the expense of power consumption. This behavior is seen in the Typical Performance Characteristics section. For applications where the P_{SAT} requirement is not stringent, reduce the V_{DD1} and the V_{DD2} of the HMC1114 to improve power consumption. To obtain the best performance while not damaging the device, follow the recommended biasing sequence outlined in the Recommended Bias Sequence section.

TYPICAL APPLICATION CIRCUIT

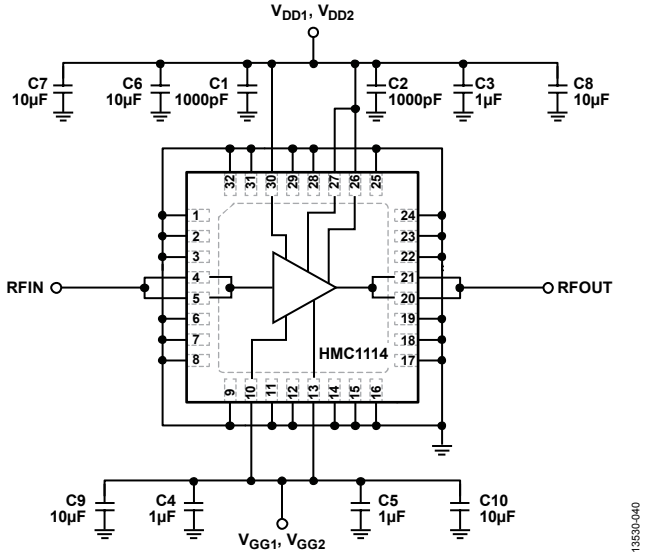

Figure 41. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The EV1HMC1114LP5D (600-01209-00) evaluation PCB is shown in Figure 42.

BILL OF MATERIALS

Use RF circuit design techniques for the circuit board used in the application. Provide 50 Ω impedance for the signal lines and directly connect the package ground leads and exposed paddle to the ground plane, similar to that shown in Figure 42. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation PCB shown in Figure 42 is available from Analog Devices, Inc., upon request.

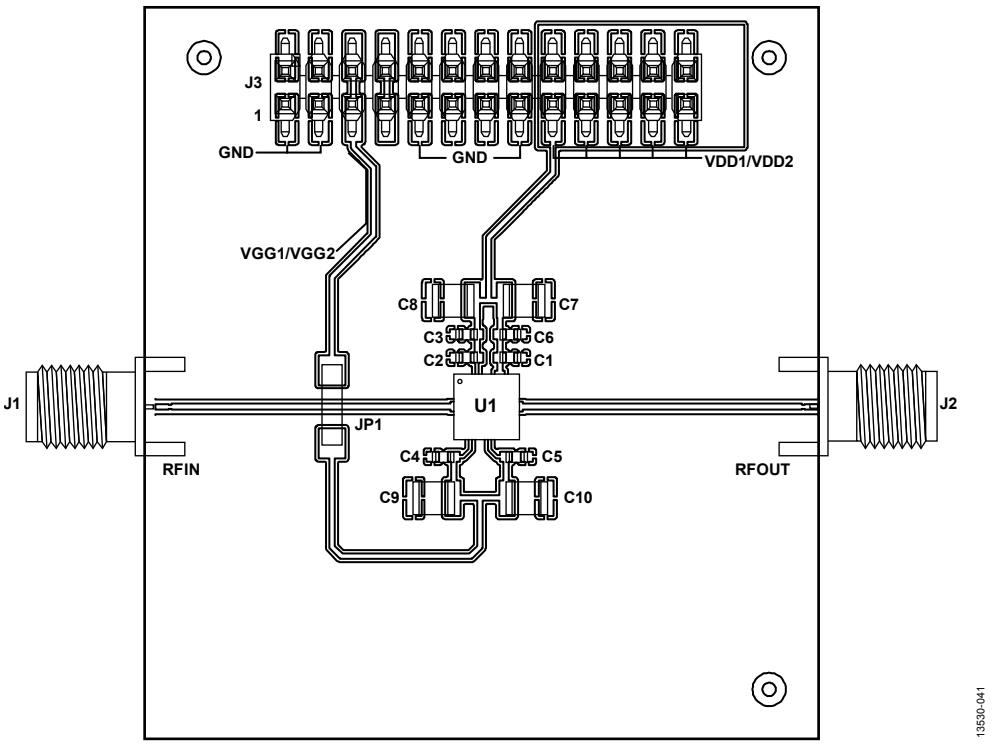

Figure 42. Evaluation Printed Circuit Board (PCB)

Table 6. Bill of Materials for Evaluation PCB EV1HMC1114LP5D (600-01209-00)

Item	Description
J1, J2	SMA connectors
J3	DC pins
JP1	Preform jumper
C1, C2	1000 pF capacitors, 0603 package
C3 to C6	1 µF capacitors, 0603 package
C7 to C10	10 µF capacitors, 1210 package
U1	HMC1114LP5DE
PCB	600-01209-00 evaluation PCB; circuit board material: Rogers 4350 or Arlon 25FR

OUTLINE DIMENSIONS

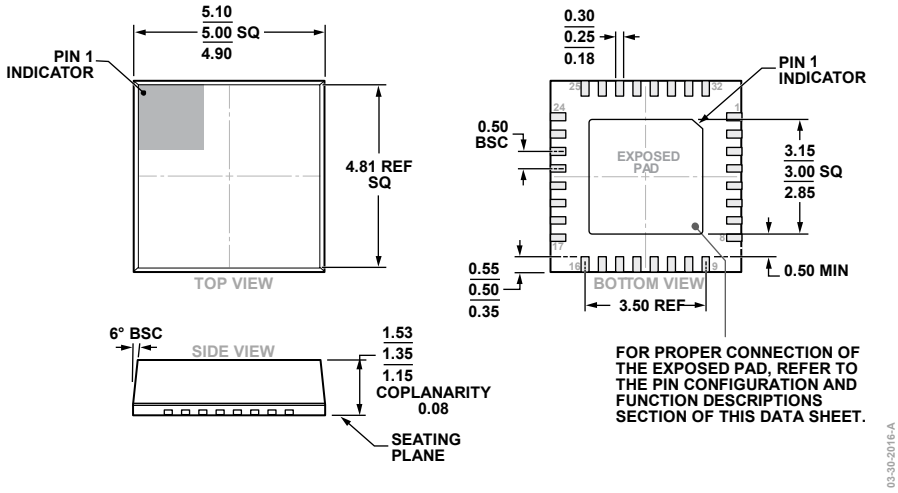

Figure 43. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.34 mm Package Height
(CG-32-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature	MSL Rating[3]	Description[4]	Package Option	Package Marking[5]
HMC1114LP5DE	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-1	H1114 XXXX
HMC1114LP5DETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-1	H1114 XXXX
EV1HMC1114LP5D			Evaluation Board		

[1] The HMC1114LP5DE and the HMC1114LP5DETR are LFCSP premolded copper alloy lead frame and RoHS Compliant Parts.
[2] When ordering the evaluation board only, reference the EV1HMC1114LP5D model number.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC1114LP5DE and HMC1114LP5DETR are nickel palladium gold (NiPdAu).
[5] The HMC1114LP5DE and HMC1114LP5DETR four-digit lot number is represented by XXXX.