TS51221

High Efficiency Regulator IC for Wireless Power Receiver Applications

TRIUNE PRODUCTS

Features

- Fixed output voltage choices: 1.5V, 1.8V, 2.5V, 3.3V, and 5V with +/- 2% output tolerance
- Adjustable version output voltage range: 0.9V to 5.5V with +/- 1.5% reference
- Wide input voltage range: 4.5V to 24V
- 1MHz +/- 10% fixed switching frequency
- Input under voltage lockout
- Full protection for over-current, over-temperature, and V_{OUT} over-voltage
- Low external component count

Summary Specification

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 16pin QFN (3x3)

Description

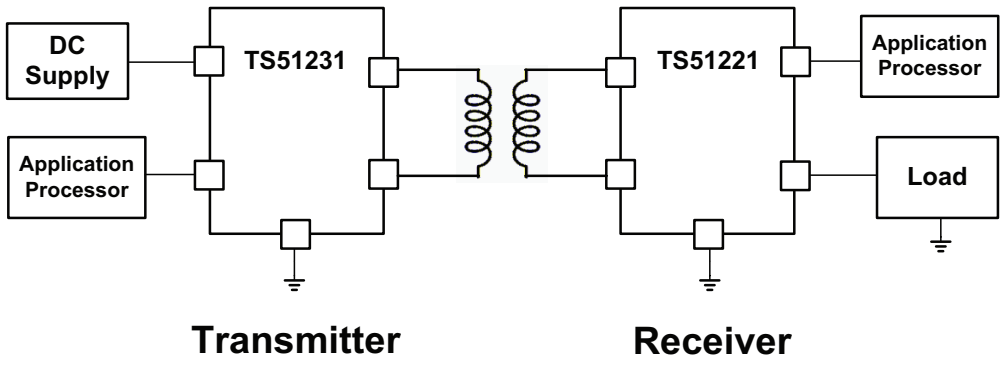
The TS51221 is a high-efficiency regulator device for low-power wireless power receiver applications. The switching frequency of 1MHz enables the use of small filter components resulting in minimal board space and reduced BOM costs.

The TS51221 integrates a wide range of protection circuitry including input supply under-voltage lockout, output voltage soft start, current limit, and thermal shutdown.

Applications

- Wireless Charging for portable devices
- Wear-ables, medical monitors
- Bluetooth headsets
- Smart watches

Typical Application Circuit



Pinout

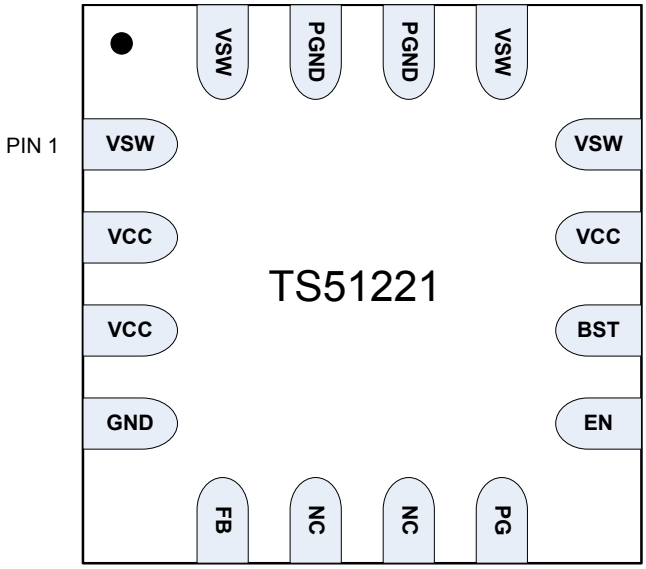


Figure 1: 16 Lead 3x3 QFN, Top View

Pin Description

Pin #	Pin Name	Pin Function	Description
1	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
2	VCC	Input Voltage	Input voltage
3	VCC	Input Voltage	Input voltage
4	GND	GND	Primary ground for the majority of the device except the low-side power FET
5	FB	Feedback Input	Regulator FB Voltage. Connects to V_{OUT} for fixed mode and the output resistor divider for adjustable mode
6	NC	No Connect	Not Connected
7	NC	No Connect	Not Connected
8	PG	Power Good Output	Open-drain output
9	EN	Enable Input	Above 2.2V the device is enabled. GND the pin to put device in standby mode. Includes internal pull-up
10	BST	Bootstrap Capacitor	Bootstrap capacitor for the high-side FET gate driver. 22nF ceramic capacitor from BST pin to VSW pin
11	VCC	Input Voltage	Input Voltage
12	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
13	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
14	PGND	Power GND	GND supply for internal low-side FET/integrated diode
15	PGND	Power GND	GND supply for internal low-side FET/integrated diode
16	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor

Functional Block Diagram

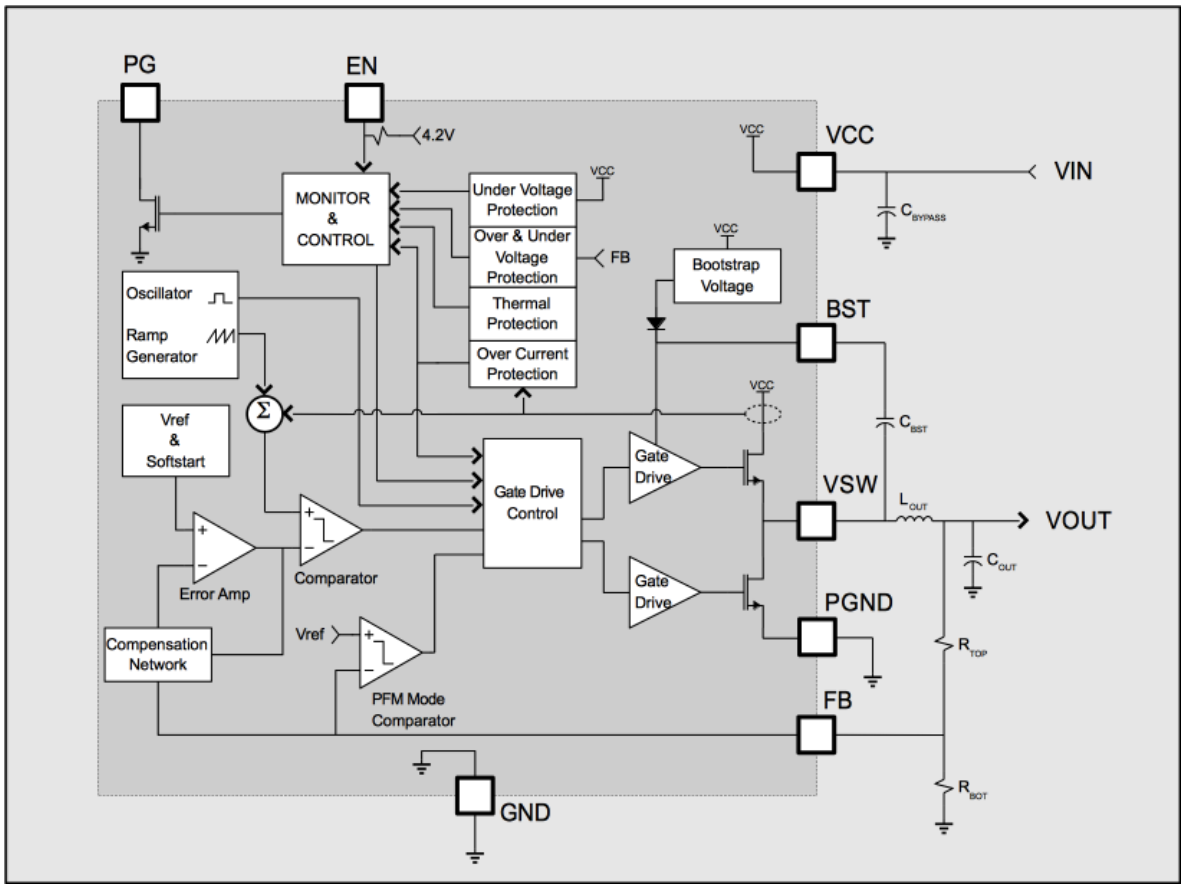


Figure 2: TS51221 Block Diagram

Absolute Maximum Rating

Over operating free–air temperature range unless otherwise noted(1, 2)

Parameter	Value	Unit
VCC	-0.3 to 26.4	V
BST	-0.3 to (VCC+6)	V
VSW	-1 to 26.4	V
EN, PG,FB	-0.3 to 6	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Thermal Characteristics

Symbol	Parameter	Value	Units
Θ_{JA}	Thermal Resistance Junction to Air (Note 1)	34.5	°C/W
Θ_{JC}	Thermal Resistance Junction to Case (Note 1)	2.5	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\ MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch2 of 1 oz Cu and 4 thermal vias connected to PAD

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Input Operating Voltage	4.5	12	24	V
C_{BST}	Bootstrap Capacitor	17.6	22	26.4	nF
L_{OUT}	Output Filter Inductor Typical Value (Note 1)	3.76	4.7	5.64	uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2)	33	44 (2 x 22)		uF
$C_{OUT-ESR}$	Output Filter Capacitor ESR	2		100	mΩ
C_{BYPASS}	Input Supply Bypass Capacitor Typical Value (Note 3)	8	10		uF

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple.

Note 2: For best performance, a low ESR ceramic capacitor should be used.

Note 3: For best performance, a low ESR ceramic capacitor should be used. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}.

Electrical Characteristics

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC Supply Voltage						
V_{CC}	Input Supply Voltage		4.5		24	V
$I_{CC-NORM}$	Quiescent current Normal Mode	V_{CC} = 12V, I_{LOAD} = 0A		5.2		mA
$I_{CC-NOSWITCH}$	Quiescent current Normal Mode – Non-switching	V_{CC}=12V, I_{LOAD}=0A, Non-switching		2.3		mA
$I_{CC-STBY}$	Quiescent current Standby Mode	V_{CC} = 12V, EN = 0V		5	10	uA
VCC Under Voltage Lockout						
V_{CC-UV}	Input Supply Under Voltage Threshold	V_{CC} Increasing		4.3	4.5	V
V_{CC-UV_HYST}	Input Supply Under Voltage Threshold Hysteresis			650		mV
OSC						
F_{OSC}	Oscillator Frequency		0.9	1	1.1	MHz
PG Open Drain Output						
T_{PG}	PG Release Timer			10		ms
I_{OH-PG}	High-Level Output Leakage	V_{PG} = 5V		0.5		uA
V_{OL-PG}	Low-Level Output Voltage	I_{PG} = -0.3mA			0.01	V
EN Input Voltage Thresholds						
V_{IH-EN}	High Level Input Voltage		2.2			V
V_{IL-EN}	Low Level Input Voltage				0.8	V
$V_{HYST-EN}$	Input Hysteresis			480		mV
I_{IN-EN}	Input Leakage	V_{EN}=5V		3.5		uA
		V_{EN}=0V		-1.5		uA
Thermal Shutdown						
TSD	Thermal Shutdown Junction Temperature	Note: not tested in production	150	170		°C
TSD_{HYST}	TSD Hysteresis	Note: not tested in production		10		°C

Regulator Characteristics

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switch Mode Regulator: L=4.7uH and C=2 x 22uF						
$V_{OUT-PWM}$	Output Voltage Tolerance in PWM Mode	I_{LOAD} =1A	V_{OUT} – 2%	V_{OUT}	V_{OUT} + 2%	V
$V_{OUT-PFM}$	Output Voltage Tolerance in PFM Mode	I_{LOAD} = 0A	V_{OUT} – 1%	V_{OUT} + 1%	V_{OUT} + 3.5%	V
R_{DSON}	High Side Switch On Resistance	I_{VSW} = -1A (Note 1)		180		mΩ
	Low Side Switch On Resistance	I_{VSW} = 1A (Note 1)		120		mΩ
I_{OUT}	Output Current				1	A
I_{OCD}	Over Current Detect	HS switch current	1.4	1.8	2.4	A
FB_{TH}	Feedback Reference (Adjustable Mode)	(Note 3)	0.886	0.9	0.914	V
FB_{TH-TOL}	Feedback Reference Tolerance	(Note 3)	-1.5		1.5	%
T_{SS}	Soft start Ramp Time			4		ms
FB_{TH-PFM}	PFM Mode FB Comparator Threshold			V_{OUT} + 1%		V
V_{OUT-UV}	V_{OUT} Under Voltage Threshold		91% V_{OUT}	93% V_{OUT}	95% V_{OUT}	
V_{OUT-UV_HYST}	V_{OUT} Under Voltage Hysteresis			1.5% V_{OUT}		
V_{OUT-OV}	V_{OUT} Over Voltage Threshold			103% V_{OUT}		
V_{OUT-OV_HYST}	V_{OUT} Over Voltage Hysteresis			1% V_{OUT}		
$DUTY_{MAX}$	Max Duty Cycle	(Note 2)	95%	97%	99%	

Note 1: R_{DSON} is characterized at 1A and tested at lower current in production.
Note 2: Regulator VSW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished.
Note 3: For the adjustable version, the ratio of VCC/V_{OUT} cannot exceed 16.
Note 4: Based on Over Current Detect testing

Functional Description

The TS51221 wireless power receiver device is a switching converter that includes flexibility to be used for a wide range of input voltages and is optimized for high efficiency power conversion with low R_{DSON} integrated synchronous switches. A 1MHz internal switching frequency facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor.

Detailed Pin Descripttion

Unregulated input, VCC

This terminal is the unregulated input voltage source from the rectified receiver coil voltage. It is recommended that a 10uF bypass capacitor be placed close to the device for best performance. Since this is also the main supply for the IC, good layout practices need to be followed for this connection.

Bootstrap control, BST

This terminal will provide the bootstrap voltage required for the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal and the VSW pin will provide the necessary voltage for the upper switch. In normal operation the capacitor is re-charged on every low side synchronous switching action. In the case of where the switch mode approaches 100% duty cycle for the high side FET, the device will automatically reduce the duty cycle switch to a minimum off time on every 8th cycle to allow this capacitor to re-charge.

Sense feedback, FB

This is the input terminal for the output voltage feedback.

For the fixed mode versions, this should be hooked directly to V_{OUT}. The connection on the PCB should be kept as short as possible, and should be made as close as possible to the capacitor. The trace should not be shared with any other connection. (Figure 23)

For adjustable mode versions, this should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.9\ (1 + R_{TOP}/R_{BOT})$$

The input to the FB pin is high impedance, and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short as possible and minimum width to reduce stray capacitance and to reduce the injection of noise.

For the adjustable version, the ratio of VCC/V_{OUT} cannot exceed 16.

Switching output, VSW

This is the switching node of the regulator. It should be connected directly to the 4.7uH inductor with a wide, short trace and to one end of the Bootstrap capacitor. It is switching between VCC and PGND at the switching frequency.

Ground, GND

This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

Power Ground, PGND

This is a separate ground connection used for the low side synchronous switch to isolate switching noise from the rest of the device. (Figure 23)

Enable, high-voltage, EN

This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.

Power Good Output, PG

This is an open drain, active low output. The switched mode output voltage is monitored and the PG line will remain low until the output voltage reaches the $V_{OUT\text{-}UV}$ threshold. Once the internal comparator detects the output voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted to high once this delay timer expires. In the event the output voltage decreases below $V_{OUT\text{-}UV}$, the PG line will be asserted low and remain low until the output rises above $V_{OUT\text{-}UV}$ and the delay timer times out. See Figure 2 for the circuit schematic for the PG signal.

Internal Protection Details

Internal Current Limit

The current through the high side FET is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. In addition, the device senses the FB pin to identify hard short conditions and will direct the VSW output to skip 4 cycles if current limit occurs when FB is low. This allows current built up in the inductor during the minimum on time to decay sufficiently. Current limit is always active when the regulator is enabled. Soft start ensures current limit does not prevent regulator startup.

Under extended over current conditions (such as a short), the device will automatically disable. Once the over current condition is removed, the device returns to normal operation automatically. (Alternately the factory can configure the device's NVM to shutdown the regulator if an extended over current event is detected and require a toggle of the Enable pin to return the device to normal operation.)

Thermal Shutdown

If the temperature of the die exceeds 170°C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will start up again, following the normal soft start sequence. If the device reaches 170°C, the shutdown/ restart sequence will repeat.

Reference Soft Start

The reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the Enable pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active, and will still protect the device in case of a short on the output.

Output Overvoltage

If the output of the regulator exceeds 103% of the regulation voltage, the VSW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete, and the VSW outputs will tri-state at the beginning of the next cycle.

VCC Under-Voltage Lockout

The device is held in the off state until VCC reaches 4.5V (typical). There is a 500mV hysteresis on this input, which requires the input to fall below 4.0V (typical) before the device will disable.

Typical Performance Characteristics

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

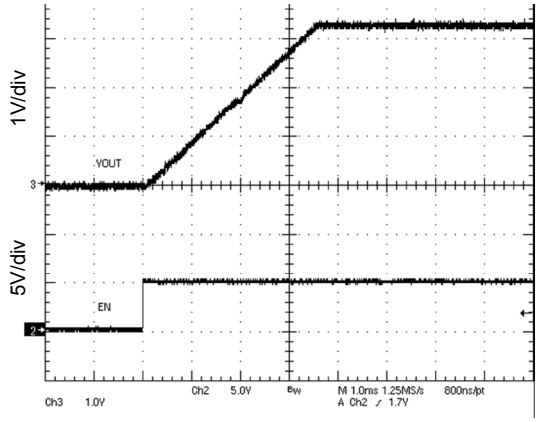


Figure 3. Startup Response

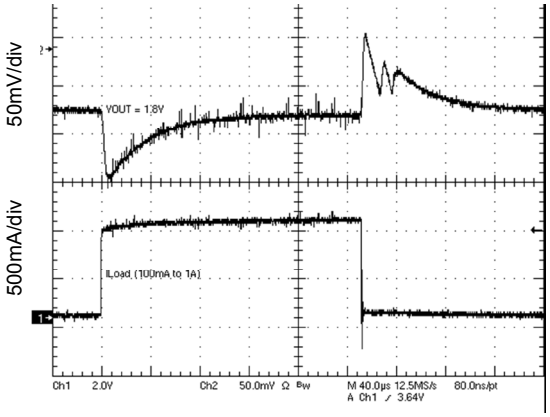


Figure 4. 100mA to 1A Load Step (Vcc=12V, V_{OUT}=1.8V)

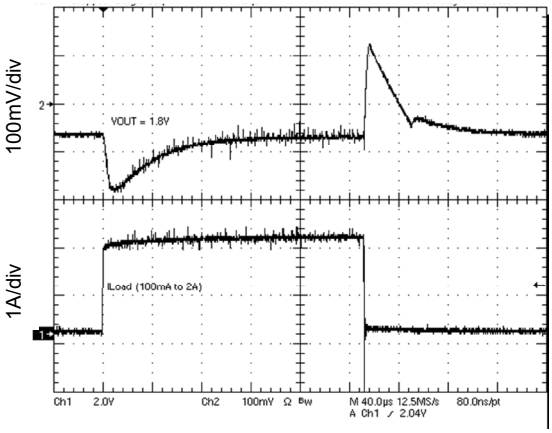


Figure 5. 100mA to 2A Load (V_{CC}=12V, V_{OUT}=1.8V)

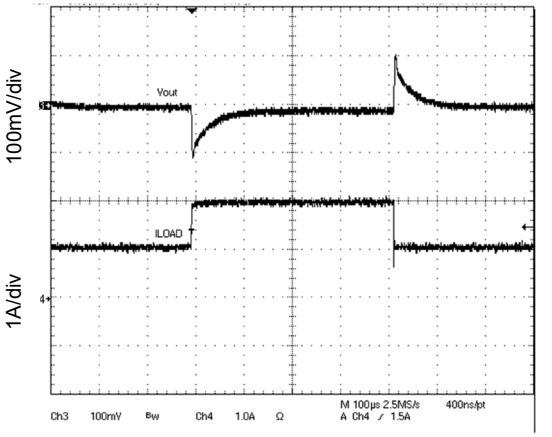


Figure 6. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

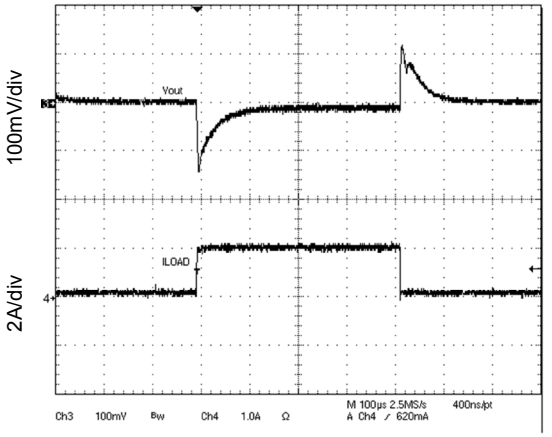


Figure 7. 100mA to 2A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

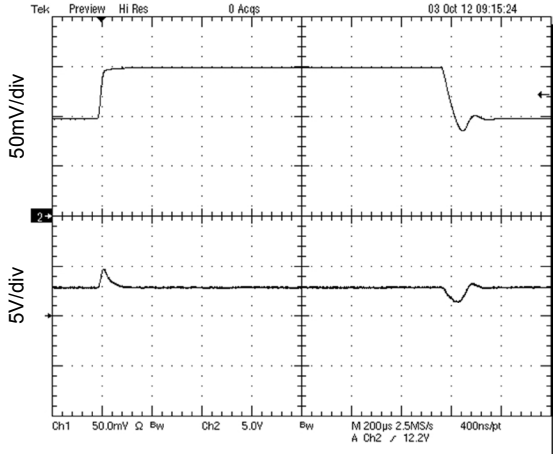


Figure 8. Line Transient Response (VCC=12V, V_{OUT}=3.3V)

Typical Performance Characteristics

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

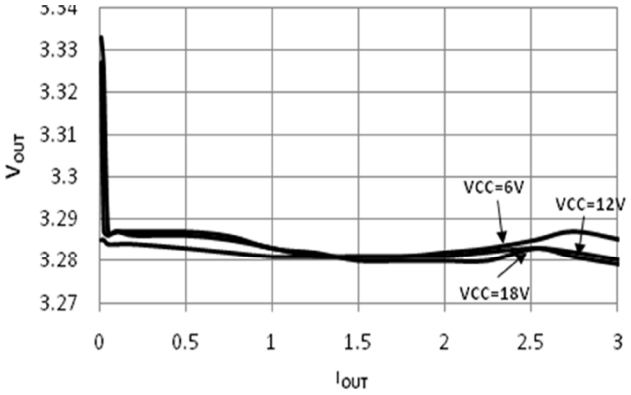


Figure 9. Load Regulation

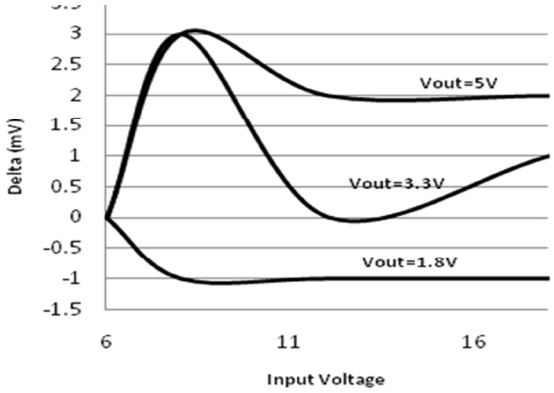


Figure 10. Line Regulation (I_{OUT}=1A)

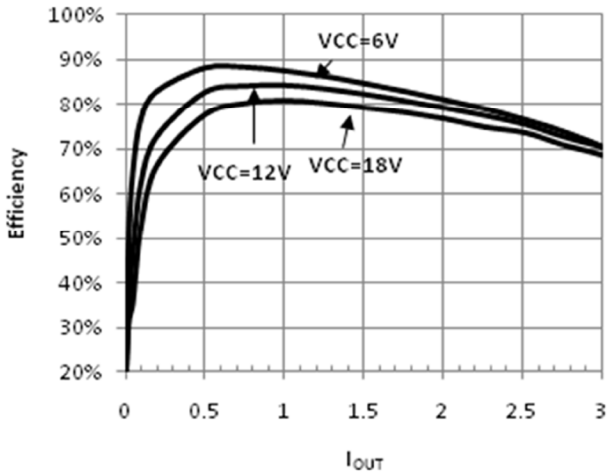


Figure 11. Efficiency vs. Output Current (V_{OUT} = 1.8V)

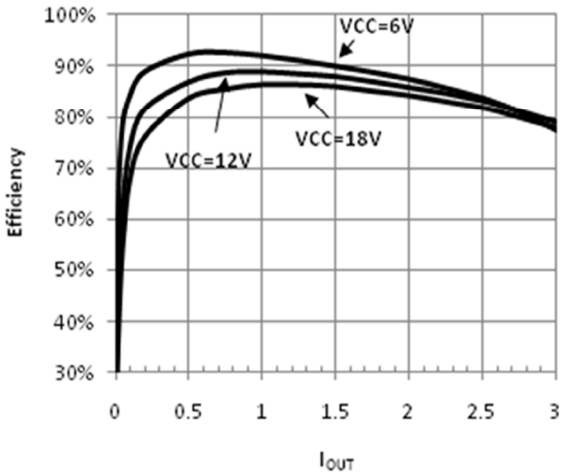


Figure 12. Efficiency vs. Output Current (V_{OUT} = 3.3V)

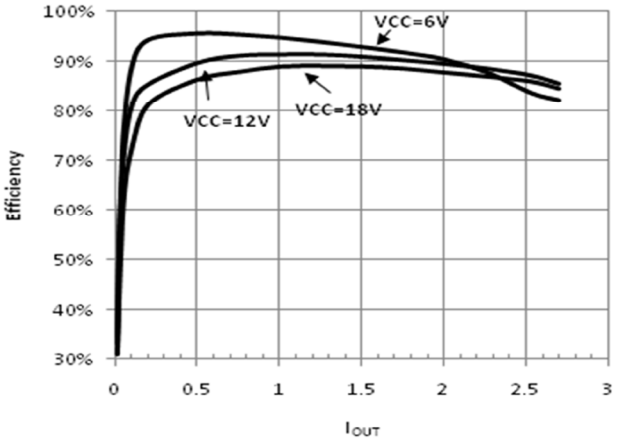


*Figure **13**. Efficiency vs. Output Current (V_{OUT} = 5V)*

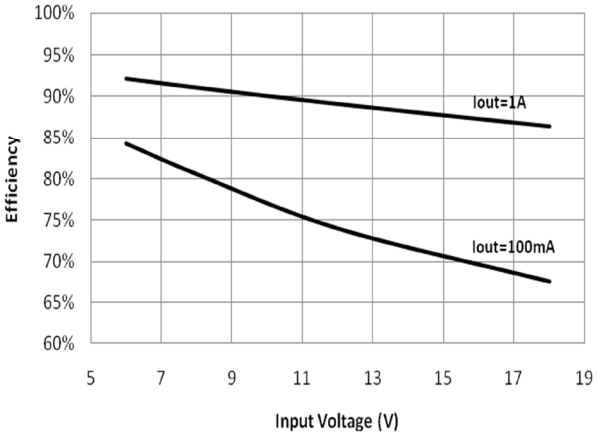


*Figure **14**. Efficiency vs. Input Voltage (V_{OUT} = 3.3V)*

Typical Performance Characteristics

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

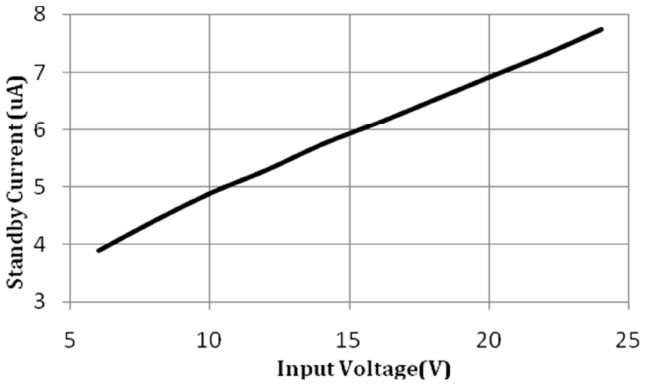


Figure 15. Standby Current vs. Input Voltage

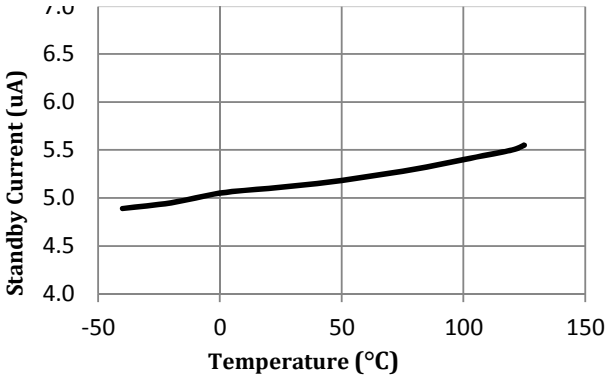


Figure 16. Standby Current vs. Temperature

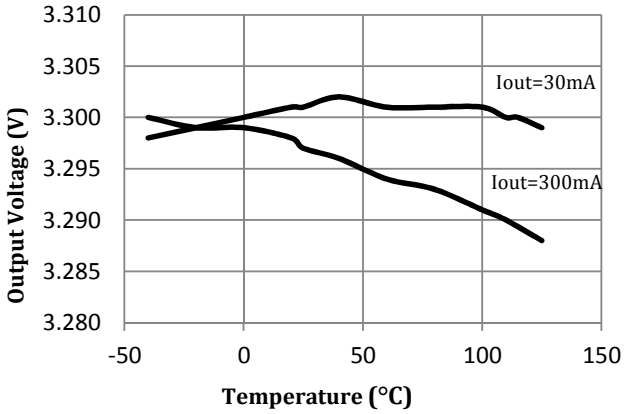


Figure 17. Output Voltage vs. Temperature

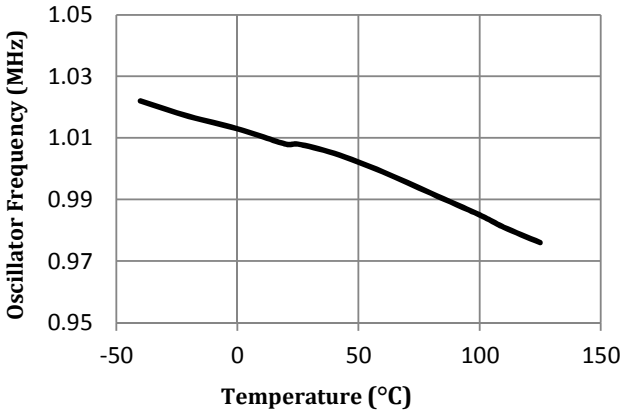


Figure 18. Oscillator Frequency vs. Temperature (Iout=300mA)

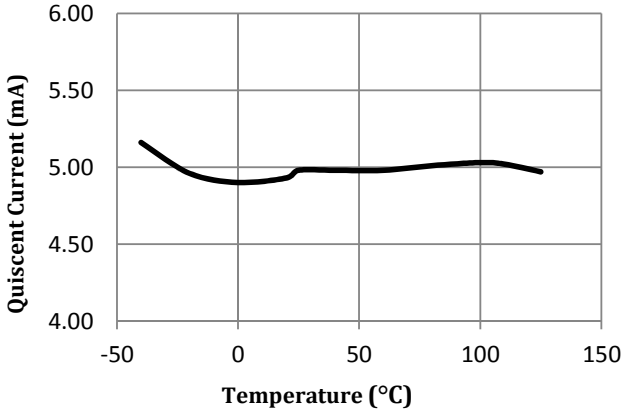


Figure 19. Quiescent Current vs. Temperature (No load)

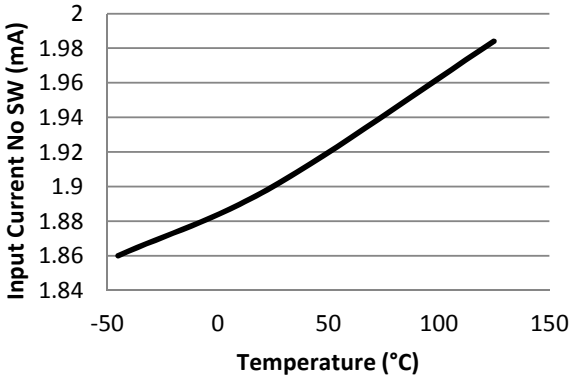


Figure 20. Input Current vs. Temperature (No load, No switching)

Typical Application Schematic

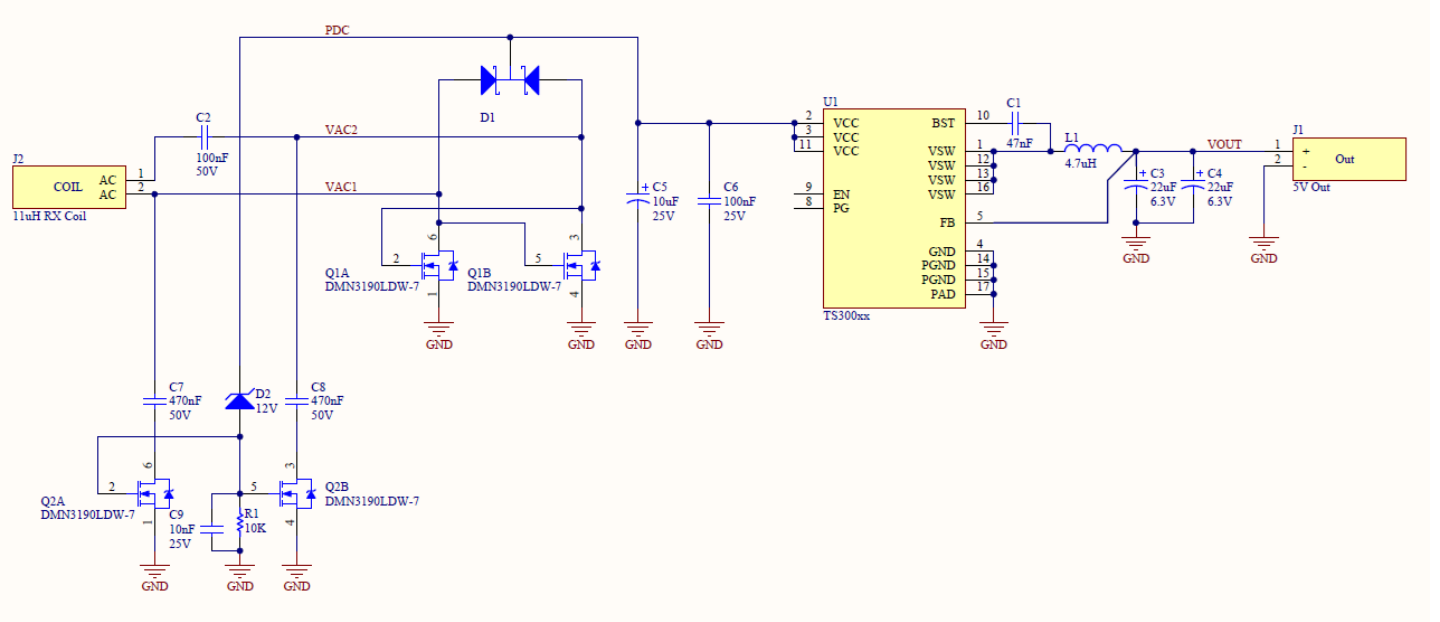


Figure 1: TS51221 Application Schematic

PCB Layout

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity and increased EMI radiation. (figure 23) The main guidelines are the following:

- provide low inductive and resistive paths for loops with high di/dt,
- provide low capacitive paths with respect to all the other nodes for traces with high di/dt,
- sensitive nodes not assigned to power transmission should be referenced to the analog signal ground (GND) and be always separated from the power ground (PGND).

The negative ends of C_{BYPASS}, C_{OUT} and the Schottky diode D_{CATCH} (optional) should be placed close to each other and connected using a wide trace. Vias must be used to connect the PGND node to the ground plane. The PGND node must be placed as close as possible to the TS51221 PGND pins to avoid additional voltage drop in traces.

The bypass capacitor C_{BYPASS} (optionally paralleled to a 0.1µF capacitor) must be placed close to the VCC pins of TS51221.

The inductor must be placed close to the VSW pins and connected directly to C_{OUT} in order to minimize the area between the VSW pin, the inductor, the C_{OUT} capacitor and the PGND pins. The trace area and length of the switching nodes VSW and BST should be minimized.

For the adjustable output voltage version of the TS51221, feedback resistors R_{BOT} and R_{TOP} are required for Vout settings greater than 0.9V and should be placed close to the TS51221 in order to keep the traces of the sensitive node FB as short as possible and away from switching signals. RBOT should be connected to the analog ground pin (GND) directly and should never be connected to the ground plane. The analog ground trace (GND) should be connected in only one point to the power ground (PGND). A good connection point is under the TS51221 package to the exposed thermal pad and vias which are connected to PGND. R_{BOT} will be connected to the VOUT node using a trace that ends close to the actual load.

For fixed output voltage versions of the TS51221, R_{BOT} and R_{TOP} are not required and the FB pin should be connected directly to the V_{OUT}.

The exposed thermal pad must be soldered to the PCB for mechanical reliability and to achieve good power dissipation. Vias must be placed under the pad to transfer the heat to the ground plane.

PCB Layout

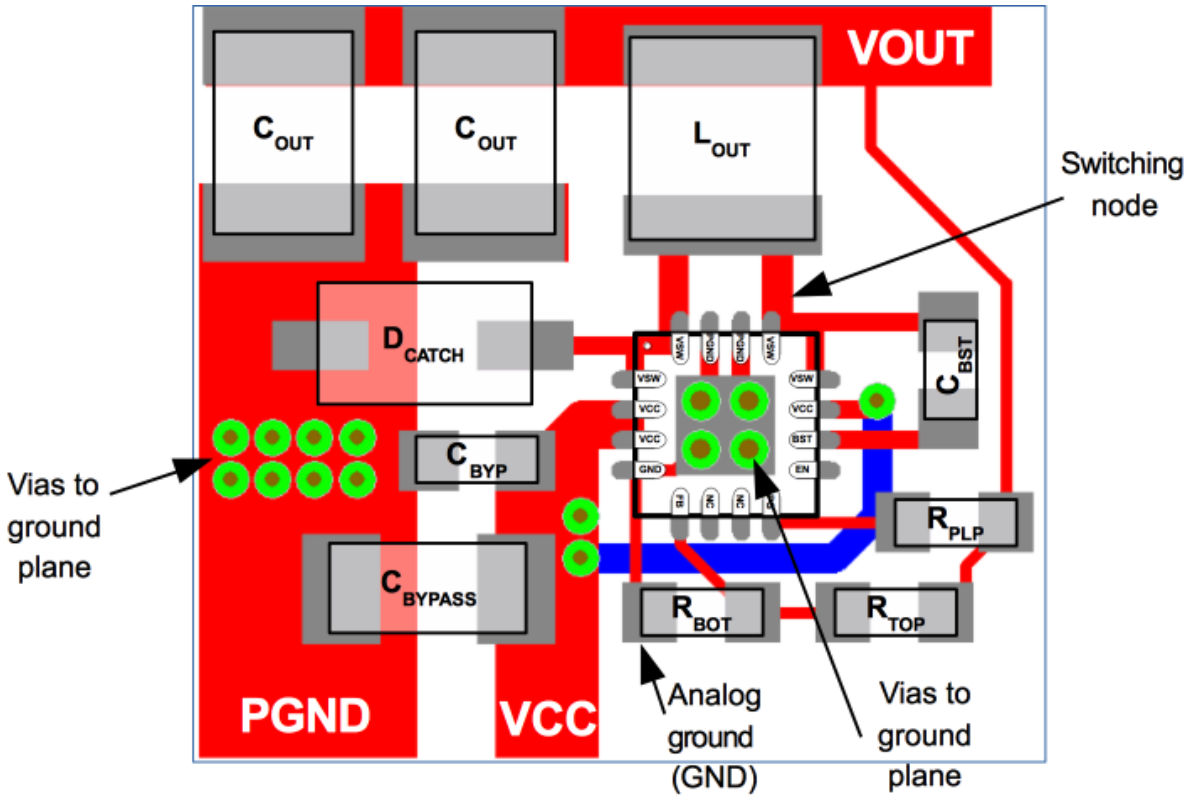


Figure : TS51221 PCB Layout, Top View

External Component Bill of Materials

Designator	Function	Description	Suggested Manufacturer	Manufacturer Code	Qty
C_{BYPASS}	Input Supply Bypass Capacitor	10uF 10% 35V	TDK	CGA5L3X5R1V106K160AB	1
C_{OUT}	Output Filter Capacitor	22uF 10% 10V	TDK	C2012X5R1A226K125AB	2
L_{OUT}	Output Filter Inductor	4.7uH 2A	TDK Wurth	SLF7045T-4R7M2R0-PF 7447745047	1
c_{BST}	Boost Capacitor	22nF 10V	TDK	C1005X7R1C223K	1
R_{TOP}	Voltage Feedback Resistor (optional)	17.8K (Note 1)			1
R_{BOT}	Voltage Feedback Resistor (optional)	10K (Note 1)			1
R_{PLP}	PG Pin Pull-up Resistor (optional)	10K			1
D_{CATCH}	Catch Diode (optional)	30V 2A SOD-123FL	On Semiconductor	MBR230LSFT1G	1

Note 1: The voltage divider resistor values are calculated for an output voltage of 2.5V. For fixed output versions, the FB pin is connected directly to V_{OUT}.

External Component Selection

The 1MHz internal switching frequency of the TS51221 facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The internal compensation is optimized for a 44uF output capacitor and a 4.7uH inductor.

For best performance, a low ESR ceramic capacitor should be used for C_{BYPASS}. If C_{BYPASS} is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}.

The minimum allowable value for the output capacitor is 33uF. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended. Multiple capacitors can be paralleled to reduce the ESR.

The inductor range is 4.7uH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation. Otherwise, an inductor with a saturation current rating higher than the maximum I_{OUT} load requirement plus the inductor current ripple should be used.

For high current modes, the optional Schottky diode will improve the overall efficiency and reduce the heat. It is up to the user to determine the cost/benefit of adding this additional component in the user's application. The diode is typically not needed.

For the adjustable output version of the TS51221, the output voltage can be adjusted by sizing R_{TOP} and R_{BOT} feedback resistors. The equation for the output voltage is

$$Vout = 0.9 \cdot \left(1 + \left(\frac{R_{TOP}}{R_{BOT}}\right)\right)$$

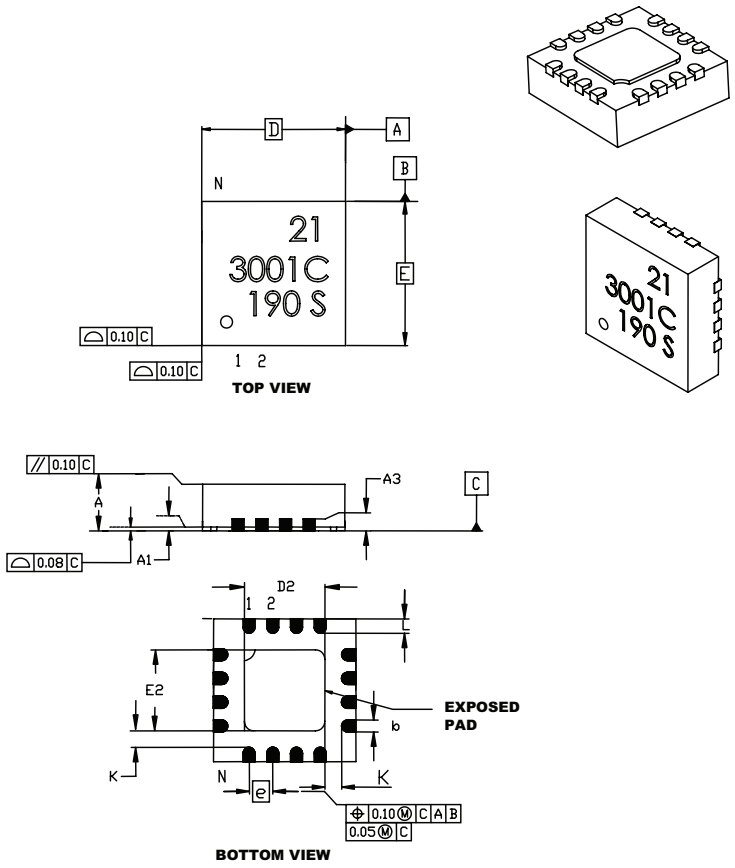
For the adjustable version, the ratio of VCC/V_{OUT} cannot exceed 16.

R_{PUP} is only required when the Power Good signal (PG) is utilized.

Thermal Information

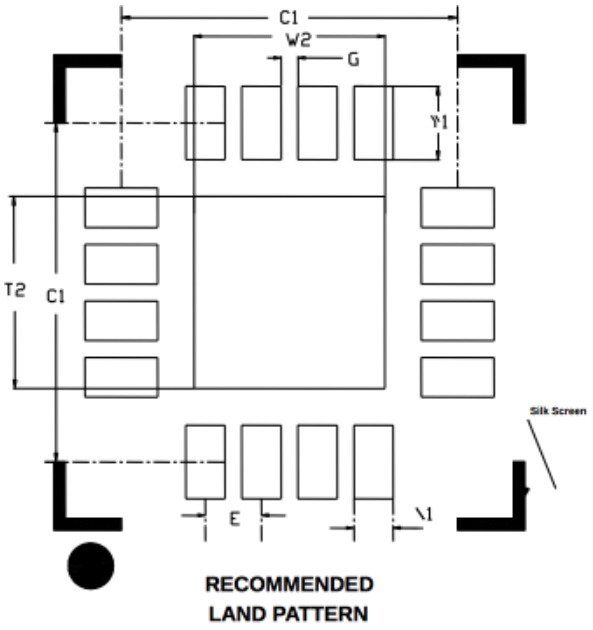
TS51221 is designed for a maximum operating junction temperature T_J of 125°C. The maximum output power is limited by the power losses that can be dissipated over the thermal resistance given by the package and the PCB structures. The PCB must provide heat sinking to keep the TS51221 cool. The exposed metal on the bottom of the QFN package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias. Adding more copper to the top and the bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. For a hi-K JEDEC board and 13.5 square inch of 1 oz Cu, the thermal resistance from junction to ambient can be reduced to Θ_{JA} = 38°C/W. The power dissipation of other power components (catch diode, inductor) cause additional copper heating and can further increase what the TS51221 sees as ambient temperature.

Package Mechanical Drawings (all dimensions in mm)



Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.30	0.40
Contact-to-Exposed Pad	K	0.20	-	-

Recommended PCB Land Pattern



Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2	-	-	1.70
Optional Center Pad Length	T2	-	-	1.70
Contact Pad Spacing	C1	-	3.00	-
Contact Pad Spacing	C2	-	3.00	-
Contact Pad Width (X16)	X1	-	-	0.35
Contact Pad Length (X16)	Y1	-	-	0.65
Distance Between Pads	G	0.15	-	-

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

Package Information

Pb-Free (RoHS): The TS51221 devices are fully compliant for all materials covered by European Union Directive 2002/95/EC, and meet all IPC-1752 Level 3 materials declaration requirements.

MSL, Peak Temp: The TS51221 family has a Moisture Sensitivity Level (MSL) 1 rating per JEDEC J-STD-020D. These devices also have a Peak Profile Solder Temperature (Tp) of 260°C.

Ordering Information

TS51221-MvvvQFNR

vvv	Output Voltage
015	1.5 V
018	1.8 V
025	2.5 V
033	3.3 V
050	5.0 V
000	Adjustable

Contact Information

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