19-5714; Rev 1; 3/11

EVALUATION KIT AVAILABLE

6-Channel, Digital Ground-Level Translator

MAX14842

General Description

The MAX14842 translates digital signals between two domains that have different ground references of up to 72V. The device features six communication channels, two bidirectional and four unidirectional. Two of the four unidirectional channels go in each direction. The device is powered by two supply voltages that independently define the logic levels of each ground domain.

The MAX14842 supports guaranteed data rates up to 30Mbps on the four unidirectional channels and up to 2Mbps on the two bidirectional channels. The bidirectional channels have open-drain outputs, making them suitable for I²C signals. I²C clock stretching and hot swapping is supported on the bidirectional channels.

Undervoltage lockout ensures that the output pins have a defined behavior during power-up, power-down, and during supply transients. For proper operation, ensure that $0V \le (V_{GNDB} - V_{GNDA}) \le 72V$. Note that GNDB must be greater than or equal to GNDA.

The MAX14842 is available in a 16-pin TQFN package and is specified over the -40°C to +125°C automotive temperature range.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14842ATE+	-40°C to +125°C	16 TQFN-EP**

***EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Features

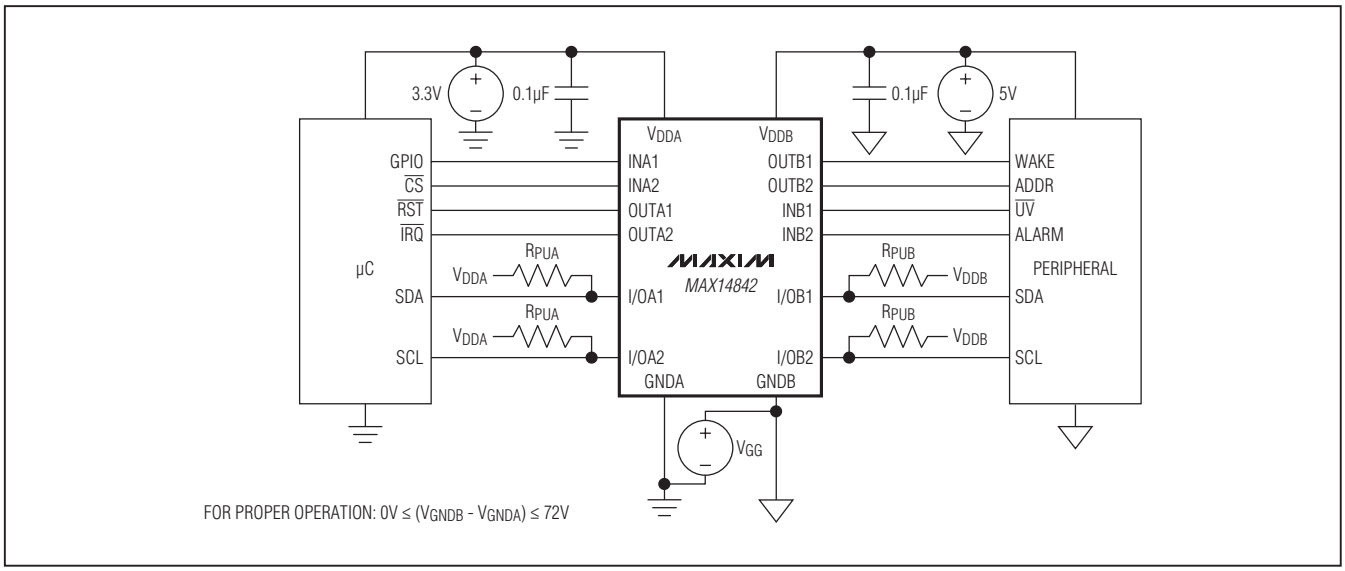
- **Supports Ground Differences Up to 72V**
- **Four Unidirectional Channels: Two In/Two Out**
- **Two Bidirectional Channels**
- **I²C Compatible**
- **Supports I²C Clock Stretching**
- **30Mbps Unidirectional Data Rates**
- **2Mbps Bidirectional Data Rates**
- **+3.3V to +5V Level Translation**
- **Undervoltage Lockout**
- **4mm x 4mm, 16-Pin TQFN Package**
- **-40°C to +125°C Automotive Temperature Range**

Applications

Telecommunication Systems
Battery Management
I²C, SMBus™, SPI™, and MICROWIRE™ Signals
Medical Systems
Power-Over-Ethernet

SMBus is a trademark of Intel Corp.
SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Typical Operating Circuit



6-Channel, Digital Ground-Level Translator

ABSOLUTE MAXIMUM RATINGS

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB .....-0.3V to +6V
GNDB to GNDA.....-0.3V to +80V
INA1, INA2 to GNDA..... -0.3V to (V_{DDA} + 0.3V)
INB1, INB2 to GNDB..... -0.3V to (V_{DDB} + 0.3V)
OUTA1, OUTA2 to GNDA ..... -0.3V to (V_{DDA} + 0.3V)
OUTB1, OUTB2 to GNDB ..... -0.3V to (V_{DDB} + 0.3V)
I/OA1, I/OA2 to GNDA .....-0.3V to +6V
I/OB1, I/OB2 to GNDB .....-0.3V to +6V
Common-Mode Transients (i.e., Transients Between GNDA and GNDB)..... 10V/µs
Short-Circuit Duration (OUTA1, OUTA2 to GNDA; OUTB1, OUTB2 to GNDB).....Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Characteristics (θ_{JA}) ....40°C/W
Junction-to-Case Thermal Characteristics (θ_{JC}) .....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Supply Voltage	V_{DDA}	Relative to GNDA	3.0		5.5	V
	V_{DDB}	Relative to GNDB	3.0		5.5	
Supply Current	I_{DDA} I_{DDB}	V_{DDA} - V_{GNDA} = +5.5V; V_{DDB} - V_{GNDB} = +5.5V; V_{GNDB} - V_{GNDA} = +70V; all inputs at V_{GNDA}, V_{GNDB}, or +5.5V; no load			7.5	mA
Voltage Between GNDB and GNDA	V_{GG}	V_{GNDB} - V_{GNDA}	0		72	V
Side B Leakage Current	I_L				1	mA
Undervoltage-Lockout Threshold	V_{UVLO}	V_{DDA} - V_{GNDA}, V_{DDB} - V_{GNDB}		2		V
Undervoltage-Lockout Hysteresis	$V_{UVLOHYS}$	V_{DDA} - V_{GNDA}, V_{DDB} - V_{GNDB}		0.1		V
LOGIC INPUTS AND OUTPUTS						
Input Logic Threshold Voltage	V_{IT}	I/OA1, I/OA2, relative to GNDA	0.5		0.7	V
Input Logic-High Voltage	V_{IH}	INA1, INA2, relative to GNDA	0.7 x V_{DDA}			V
		INB1, INB2, relative to GNDB	0.7 x V_{DDB}			
		I/OA1, I/OA2, relative to GNDA	0.7			
		I/OB1, I/OB2, relative to GNDB	0.7 x V_{DDB}			

ELECTRICAL CHARACTERISTICS (continued)

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Logic-Low Voltage	V_{IL}	INA1, INA2, relative to GNDA			0.8	V
		INB1, INB2, relative to GNDB			0.8	
		I/OA1, I/OA2, relative to GNDA			0.5	
		I/OB1, I/OB2, relative to GNDB			0.3 x V_{DDB}	
Output Logic-High Voltage	V_{OH}	OUTA1, OUTA2, relative to GNDA, source current = 4mA	V_{DDA} - 0.4V			V
		OUTB1, OUTB2, relative to GNDB, source current = 4mA	V_{DDB} - 0.4V			
Output Logic-Low Voltage	V_{OL}	OUTA1, OUTA2, relative to GNDA, sink current = 4mA			0.8	V
		OUTB1, OUTB2, relative to GNDB, sink current = 4mA			0.8	
		I/OA1, I/OA2, relative to GNDA, sink current = 10mA	0.6		0.9	
		I/OA1, I/OA2, relative to GNDA, sink current = 0.5mA	0.6		0.85	
		I/OB1, I/OB2, relative to GNDB, sink current = 30mA			0.4	
Input/Output Logic-Low Threshold Difference	ΔV_{TOL}	I/OA1, I/OA2 (Note 3)	50			mV
Input Leakage Current	I_L	V_{INA1}, V_{INA2}, V_{DDA} = +3.6V, V_{INB1},V_{INB2}, V_{DDB} = +3.6V	-2		+2	µA
		$V_{I/OA1}$, $V_{I/OA2}$, V_{DDA} = +3.6V, $V_{I/OB1}$, $V_{I/OB2}$, V_{DDB} = +3.6V	-2		+2	
Input Capacitance	C_{IN}	INA1, INA2, INB1, INB2, f = 1MHz (Note 4)		4		pF
DYNAMIC SWITCHING CHARACTERISTICS						
Maximum Data Rate	DR_{MAX}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2	30			Mbps
		I/OA1 to I/OB1, I/OA2 to I/OB2, I/OB1 to I/OA1, I/OB2 to I/OA2	2			
Minimum Pulse Width	PW_{MIN}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2	30			ns
Propagation Delay	t_{DPLH} t_{DPHL}	INA1 to OUTB1, INA2 to OUTB2, INB1 to OUTA1, INB2 to OUTA2, V_{DDA} = V_{DDB} = +3.0V, R_L = 1MΩ, C_L = 15pF, Figure 1		20	30	ns
	t_{DPLH} t_{DPHL}	I/OA1 to I/OB1, I/OA2 to I/OB2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	100	
	t_{DPLH} t_{DPHL}	I/OB1 to I/OA1, I/OB2 to I/OA2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		60	100	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DDA} - V_{GNDA} = +3.0V to +5.5V, V_{DDB} - V_{GNDB} = +3.0V to +5.5V, V_{GNDB} - V_{GNDA} = 0 to +72V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	I/OA1 to I/OB1, I/OA2 to I/OB2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		3	6	ns
		I/OB1 to I/OA1, I/OB2 to I/OA2, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	100	
Channel-to-Channel Skew	$t_{DSKEWCC}$	OUTB1 to OUTB2 output skew, Figure 1		3	6	ns
		OUTA1 to OUTA2 output skew, Figure 1		3	6	
		I/OB1 to I/OB2 output low skew, Figure 2		3	10	
		I/OA1 to I/OA2 output low skew, Figure 2		3	10	
Rise Time	t_R	OUTB1, OUTB2, OUTA1, OUTA2, 10% to 90%, Figure 1			5	ns
Fall Time	t_F	OUTB1, OUTB2, OUTA1, OUTA2, 90% to 10%, Figure 1			5	ns
		I/OA1, I/OA2, 90% to 10%, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1.6kΩ, R_2 = 180Ω, C_{L1} = C_{L2} = 15pF, Figure 2		30	60	
		I/OB1, I/OB2, 90% to 10%, V_{DDA} = V_{DDB} = +3.0V, R_1 = 1kΩ, R_2 = 120Ω, C_{L1} = C_{L2} = 15pF, Figure 2		3	6	

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All voltages of side A are referenced to GNDA; all voltages of side B are referenced to GNDB, unless otherwise noted.

Note 3: ΔV_{TOL} = V_{OL} - V_{IL}. This is the minimum difference between the output logic-low voltage and the input logic threshold for the same I/O pin. This ensures that the I/O channels are not latched low when any of the I/O inputs are driven low (see the *Bidirectional Channels* section).

Note 4: Guaranteed by design; not production tested.

Test Circuits/Timing Diagrams

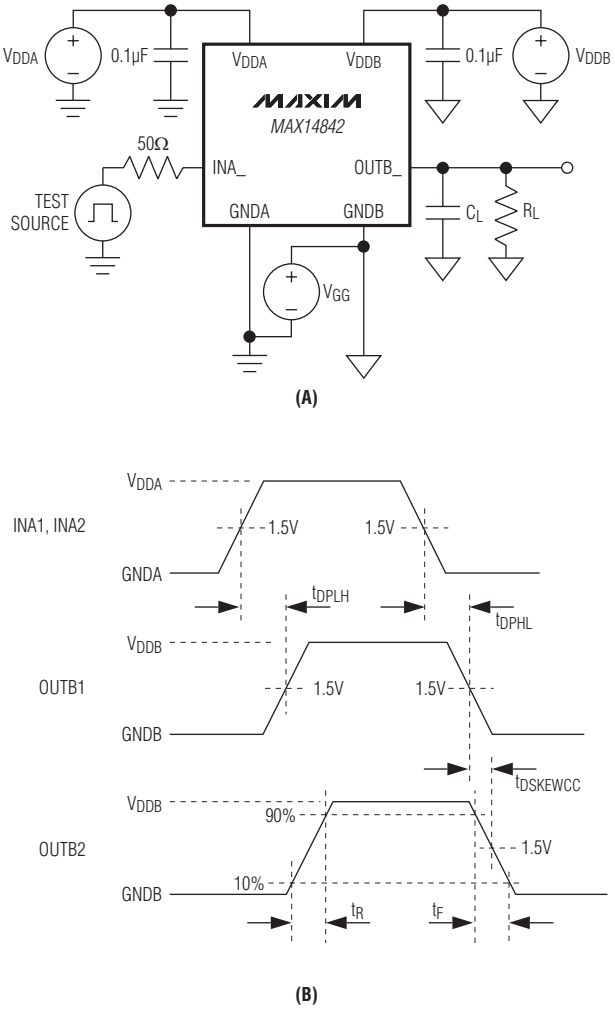

Figure 1. Test Circuit (A) and Timing Diagram (B) for Unidirectional Testing

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Test Circuits/Timing Diagrams (continued)

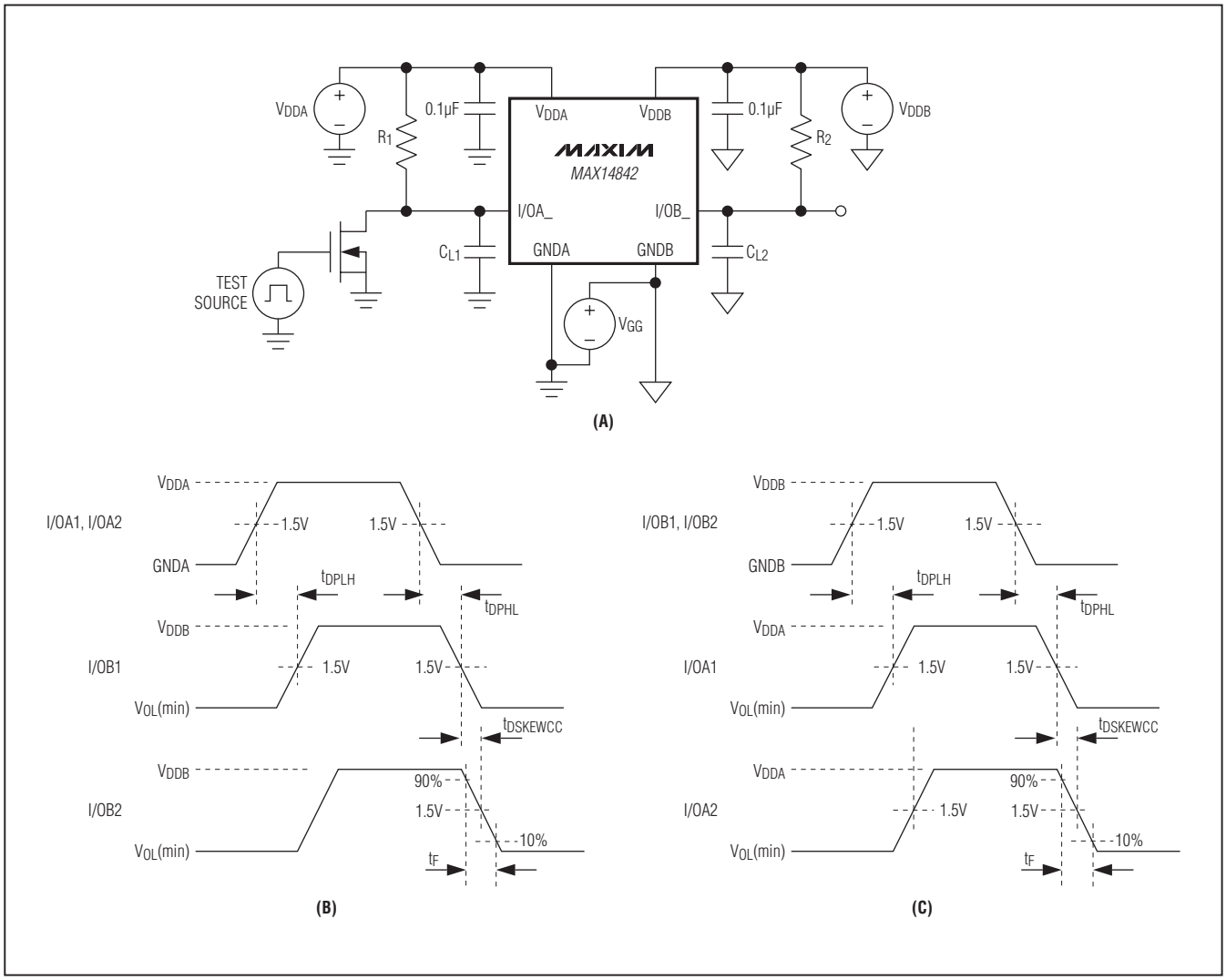
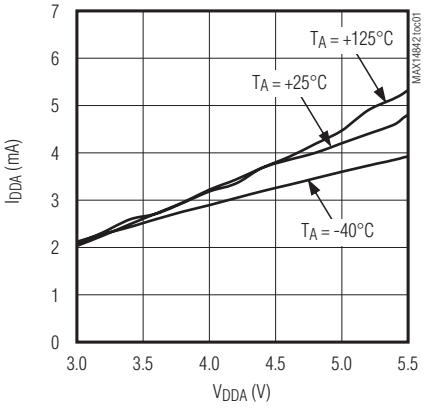


Figure 2. Test Circuit (A) and Timing Diagrams (B) and (C) for Bidirectional Testing

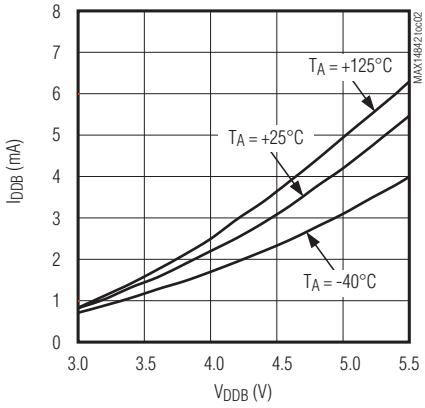
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

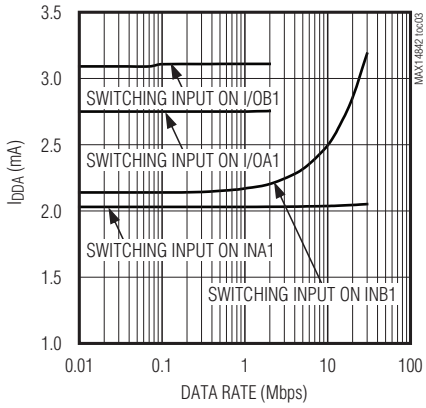
I_{DDA} vs. V_{DDA}



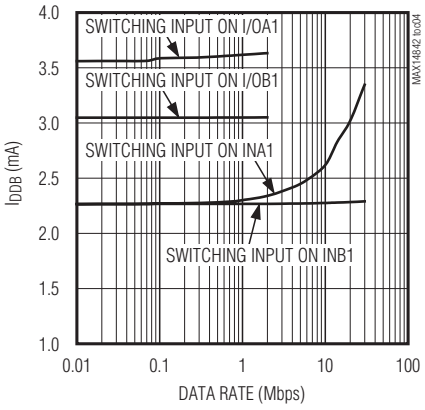
I_{DDB} vs. V_{DDB}



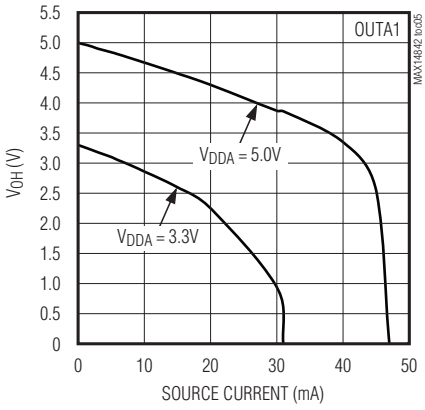
I_{DDA} vs. DATA RATE



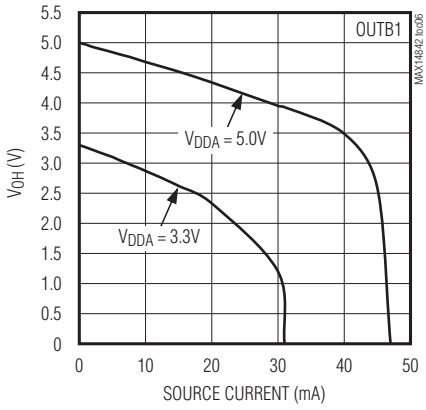
I_{DDB} vs. DATA RATE



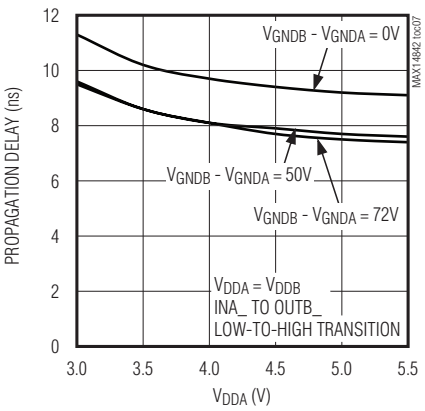
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT



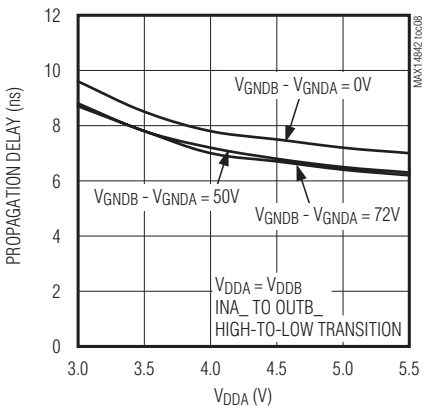
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT



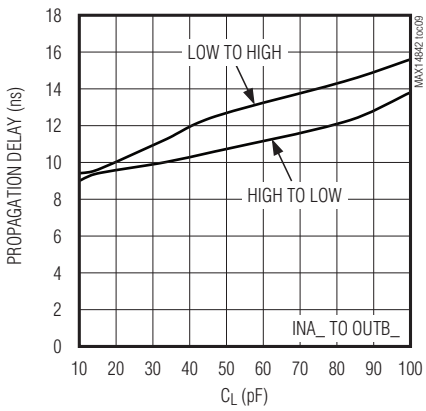
PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. CAPACITIVE LOAD

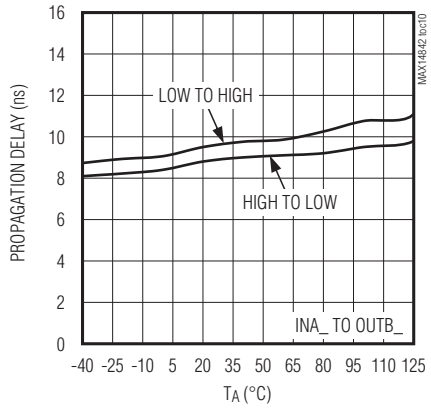


6-Channel, Digital Ground-Level Translator

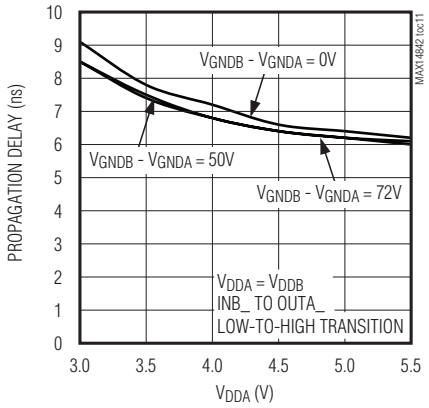
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

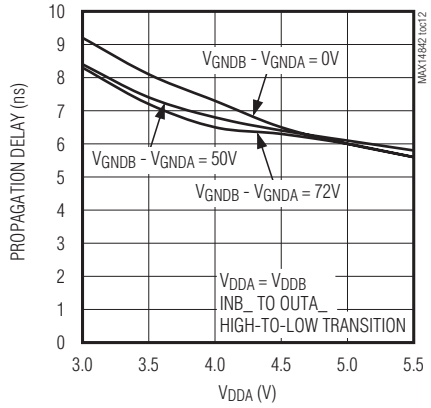
PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



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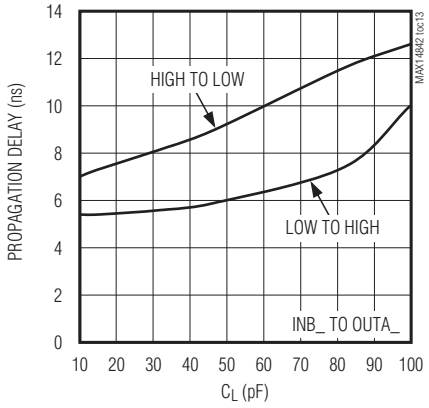
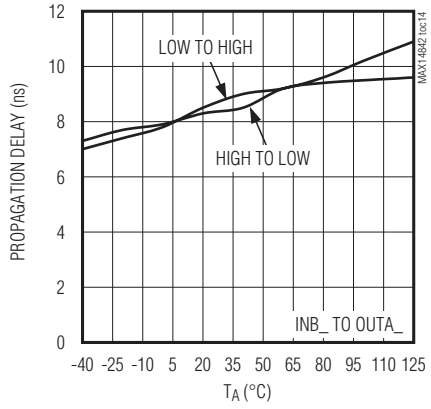
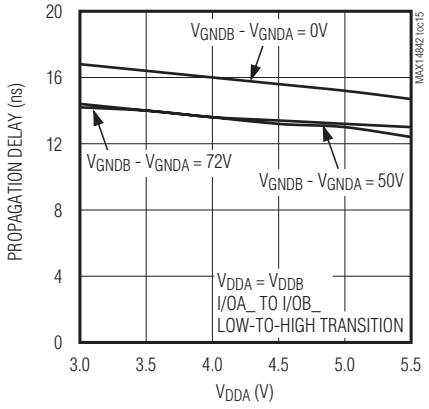


PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. SUPPLY VOLTAGE



Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDB} - V_{GNDA} = +50V, R_{PUA} = R_{PUB} = 2kΩ, C_L = 15pF, see the *Typical Operating Circuit*, T_A = +25°C, unless otherwise noted.)

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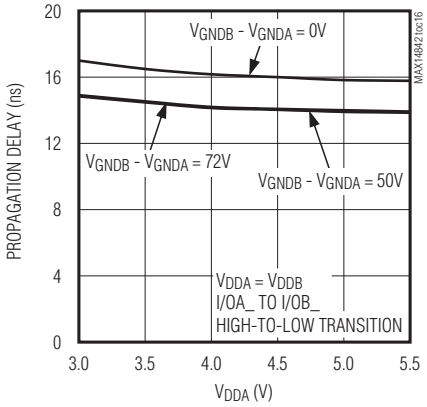
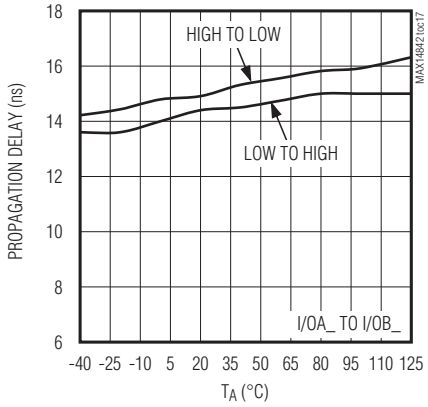
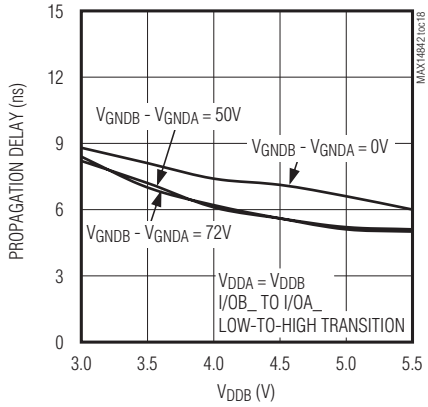


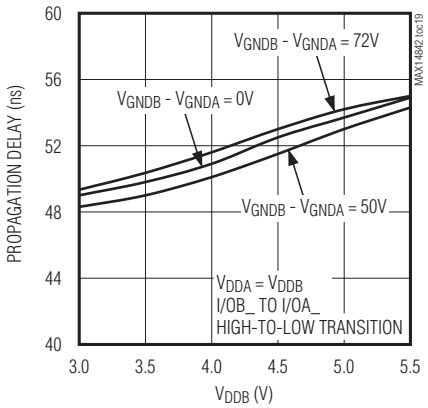
PROPAGATION DELAY vs. TEMPERATURE



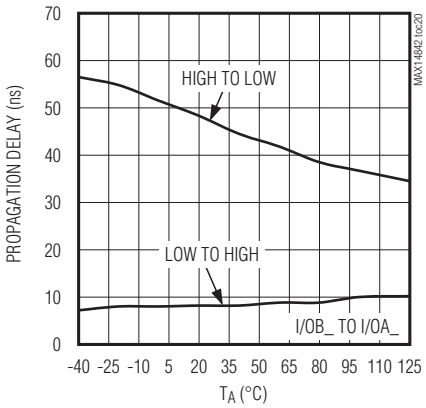
PROPAGATION DELAY vs. SUPPLY VOLTAGE



PROPAGATION DELAY vs. SUPPLY VOLTAGE

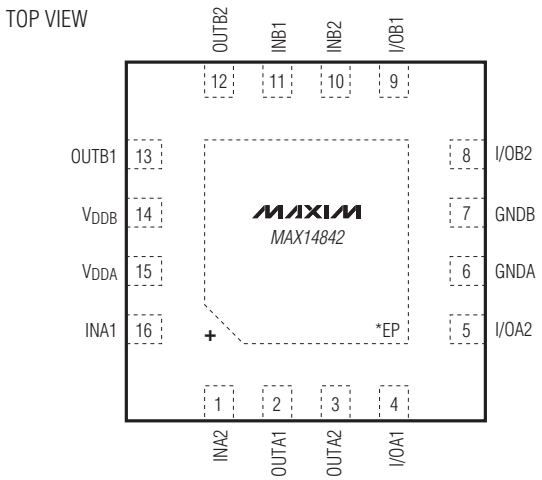


PROPAGATION DELAY vs. TEMPERATURE



6-Channel, Digital Ground-Level Translator

Pin Configuration



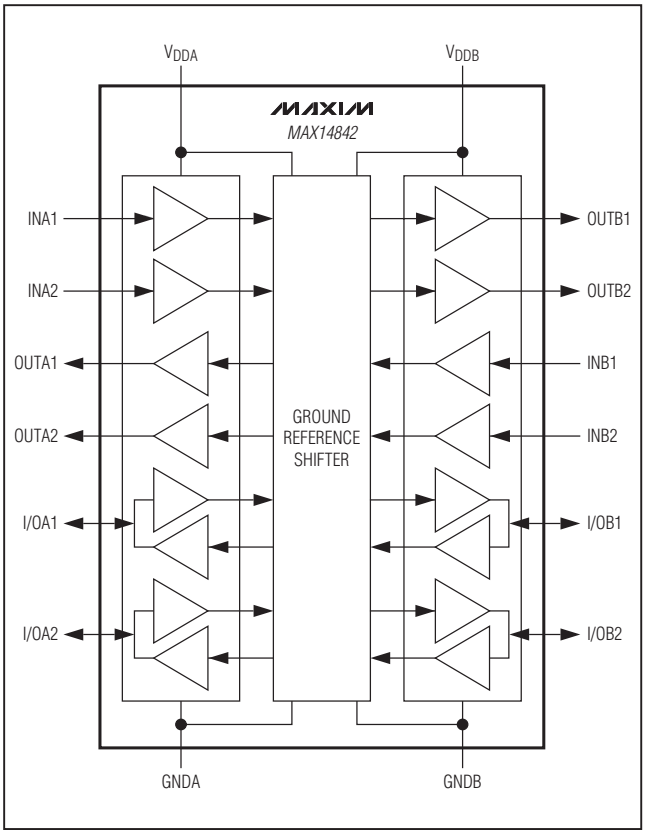
TQFN
(4mm × 4mm)

*CONNECT EXPOSED PAD TO GNDA.

Pin Description

PIN	NAME	FUNCTION	VOLTAGE RELATIVE TO
1	INA2	Logic Input 2 on Side A. INA2 is translated to OUTB2.	GNDA
2	OUTA1	Logic Output 1 on Side A. OUTA1 is a push-pull output.	GNDA
3	OUTA2	Logic Output 2 on Side A. OUTA2 is a push-pull output.	GNDA
4	I/OA1	Bidirectional Input/Output 1 on Side A. I/OA1 is translated to/from I/OB1 and is an open-drain output.	GNDA
5	I/OA2	Bidirectional Input/Output 2 on Side A. I/OA2 is translated to/from I/OB2 and is an open-drain output.	GNDA
6	GNDA	Ground Reference for Side A. V_{GNDA} must be ≤ V_{GNDB}.	—
7	GNDB	Ground Reference for Side B. V_{GNDB} must be ≥ V_{GNDA}.	—
8	I/OB2	Bidirectional Input/Output 2 on Side B. I/OB2 is translated to/from I/OA2 and is an open-drain output.	GNDB
9	I/OB1	Bidirectional Input/Output 1 on Side B. I/OB1 is translated to/from I/OA1 and is an open-drain output.	GNDB
10	INB2	Logic Input 2 on Side B. INB2 is translated to OUTA2.	GNDB
11	INB1	Logic Input 1 on Side B. INB1 is translated to OUTA1.	GNDB
12	OUTB2	Logic Output 2 on Side B. OUTB2 is a push-pull output.	GNDB
13	OUTB1	Logic Output 1 on Side B. OUTB1 is a push-pull output.	GNDB
14	V_{DDB}	Supply Voltage of Logic Side B. Bypass V_{DDB} with a 0.1µF ceramic capacitor to GNDB.	GNDB
15	V_{DDA}	Supply Voltage of Logic Side A. Bypass V_{DDA} with a 0.1µF ceramic capacitor to GNDA.	GNDA
16	INA1	Logic Input 1 on Side A. INA1 is translated to OUTB1.	GNDA
—	EP	Exposed Pad. Connect EP to GNDA.	—

Functional Diagram



Detailed Description

The MAX14842 provides both ground-level translation and logic-level shifting needed in systems where there is a difference in ground references of up to 72V. The device is powered by two supply voltages, V_{DDA} and V_{DDB}, which independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are separately referenced to GNDA and GNDB, respectively. The MAX14842 supports data rates of up to 30Mbps on each of the four unidirectional channels and 2Mbps on the two bidirectional channels.

Ground Translation/Level Shifting

For proper operation, ensure that $0V \le (V_{GNDB} - V_{GNDA}) \le 72V$. Note that GNDB must be greater than or equal to GNDA.

Also ensure that $3.0V \le (V_{DDA} - V_{GNDA}) \le 5.5V$ and $3.0V \le (V_{DDB} - V_{GNDB}) \le 5.5V$. $(V_{DDA} - V_{GNDA})$ can be greater than or less than $(V_{DDB} - V_{GNDB})$, as long as each is within the normal operating range.

Unidirectional Channels

The device features four unidirectional channels that can each operate independently with a guaranteed data rate of up to 30Mbps. The output driver of each unidirectional channel is push-pull, eliminating the need for pullup resistors. The drivers are also able to drive both TTL and CMOS logic inputs.

Bidirectional Channels

The device features two bidirectional translation channels that have open-drain outputs. The bidirectional channels do not require a direction input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the translator. To prevent latching of the bidirectional channels, the input logic-low threshold (V_{IT}) of I/OA1 and I/OA2 is at least 50mV lower than the output logic-low voltages (V_{OL}) of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B and vice versa.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 30mA for side B and 10mA for side A (see the *Electrical Characteristics* table).

The bidirectional channels of the device support I^2C clock stretching.

Separate Ground References

The device is designed to translate logic signals to and from domains with isolated and offset ground references.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a slump in the supplies. When an undervoltage event occurs on either of the supplies, all outputs on both sides are automatically controlled, regardless of the status of the inputs. The bidirectional outputs become high impedance and are pulled high by the external pullup resistor on the open-drain output. The unidirectional outputs are pulled high internally to the voltage of the V_{DDA} or V_{DDB} supply during undervoltage conditions.

6-Channel, Digital Ground-Level Translator

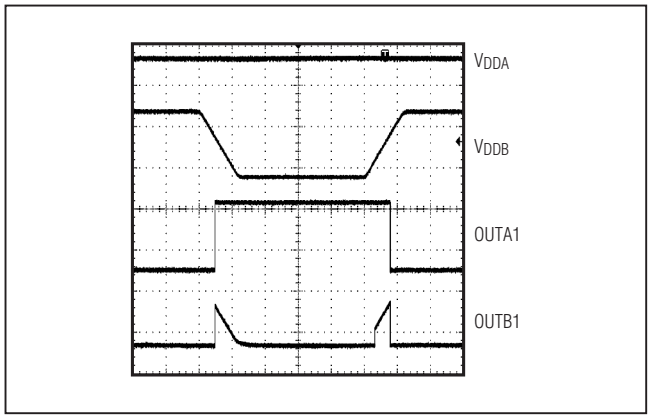


Figure 3. Undervoltage Lockout Behavior

Figure 3 shows the behavior of the outputs during power up and power down.

Applications Information

AC Components on VGG

When the ground difference voltage, V_{GG}, has a time varying (AC) component, limit the amplitude to ensure that the MAX14842 operates as specified. The maximum allowable amplitude of an AC signal on V_{GG} is a function of frequency.

Power-Supply Sequencing

The MAX14842 does not require power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Unidirectional and Bidirectional Level Translator

The MAX14842 operates both as a unidirectional device and bidirectional device simultaneously. Each unidirectional channel can only be used in the direction shown in the *Functional Diagram*. The bidirectional channels function without requiring a direction input.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1644+4	21-0139	90-0070

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	3/11	Deleted the MAX14842ETE+ from the *Ordering Information*, removed the future status from the MAX14842ATE+ in the *Ordering Information*, added the automotive temperature range to the *Features*, *Absolute Maximum Ratings*, and the *Electrical Characteristics* sections	1–4