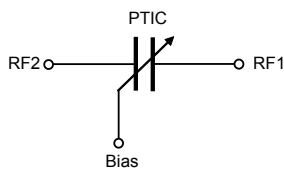


Parascan™ tunable integrated capacitor



WLCSP 3 solder bars



Features

- High power capability
- 5:1 tuning range
- High linearity (48x)
- High quality factor (Q)
- Low leakage current
- Compatible with high voltage control IC (STHVDAC series)
- RF tunable passive implementation in mobile phones to optimize antenna radiated performance
- Available in wafer level chip scale package:
 - WLCSP package 0.75 x 0.72 x 0.32 mm
- ECOPACK®2 compliant component

Applications

- Cellular antenna open loop tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- Open loop tunable RF filters

Description

The ST integrated tunable capacitor offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan™, which is a version of barium strontium titanate (BST) developed by Paratek microwave.

BST capacitors are tunable capacitors intended for use in mobile phone application and dedicated to RF tunable applications. These tunable capacitors are controlled through an extended bias voltage ranging from 1 to 24 V. The implementation of BST tunable capacitor in mobile phones enables significant improvement in terms of radiated performance making the performance almost insensitive to the external environment.

Parascan is a trademark of Paratek Microwave Inc.

| |
|-----------------------------|
| Product status link |
| STPTIC-15C4 |

1 STPTIC-15C4 characteristics

Table 1. Absolute maximum ratings (limiting values)

| Symbol | Parameter | Rating | Unit |
|----------------|---|-------------|------|
| P_{IN} | Input power RF_{IN} (CW model) / all RF ports | +40 | dBm |
| $V_{ESD(HBM)}$ | Human body model, JESD22-A114-B, all I/O | Class 1B | V |
| $V_{ESD(MM)}$ | Machine model, JESD22-A115-A, all I/O | +100 | V |
| T_{device} | Device temperature | +125 | °C |
| T_{stg} | Storage temperature | -55 to +150 | |
| V_x | Bias voltage | 25 | V |

1. Class 1B defined as passing 500 V, but fails after exposure to 1000V ESD pulse.

Table 2. Recommended operating conditions

| Symbol | Parameter | Rating | | | Unit |
|--------------|-----------------------|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| P_{IN} | RF input power | | +33 | +39 | dBm |
| F_{OP} | Operating frequency | 700 | | 2700 | MHz |
| T_{device} | Device temperature | | | +100 | °C |
| T_{OP} | Operating temperature | -30 | | +85 | |
| V_{BIAS} | Bias voltage | 1 | | 24 | V |

Table 3. Representative performance ($T_{amb} = 25\text{ °C}$ otherwise specified)

| Symbol | Parameter | Conditions | Value | | | Unit |
|------------|-----------------------------|---|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| C_{1V} | Capacitor at 1 V bias | | 1.58 | 1.8 | 2.02 | pF |
| C_{2V} | Capacitor at 2 V bias | | 1.35 | 1.5 | 1.65 | pF |
| C_{20V} | Capacitor at 20 V bias | | 0.39 | 0.42 | 0.46 | pF |
| C_{24V} | Capacitor at 24 V bias | | 0.35 | 0.38 | 0.42 | pF |
| C | Capacitance accuracy | V_{BIAS} range = 2 V/ 20 V | | | 10 | % |
| ΔC | Tuning range | Ratio between C_{1V}/C_{24V} ⁽¹⁾ | | 5/1 | | |
| I_L | Leakage current | Measured with $V_{BIAS} = 24\text{ V}$ | | | 100 | nA |
| Q_{LB} | Quality factor | Measured at 700 MHz at 2 V | 50 | 55 | | |
| Q_{HB} | Quality factor | Measured at 2700 MHz at 2 V | 35 | 40 | | |
| IP3 | Third order intercept point | $V_{BIAS} = 2\text{ V}$ ^{(2) (3)} | 60 | | | dBm |
| | | $V_{BIAS} = 20\text{ V}$ ⁽²⁾⁽³⁾ | 80 | | | dBm |
| H2 | Second harmonic | $V_{BIAS} = 2\text{ V}$ ⁽⁴⁾⁽³⁾ | | -70 | -55 | dBm |
| | | $V_{BIAS} = 20\text{ V}$ ^{(4) (3)} | | -80 | -70 | dBm |

| Symbol | Parameter | Conditions | Value | | | Unit |
|--------|-----------------|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| H3 | Third harmonic | $V_{BIAS} = 2\text{ V}$ ⁽⁴⁾⁽³⁾ | | -55 | -45 | dBm |
| | | $V_{BIAS} = 20\text{ V}$ ⁽⁴⁾⁽³⁾ | | -85 | -70 | dBm |
| t_T | Transition time | Transition between 20 V to 2 V ⁽⁵⁾ | | | 120 | μs |
| | | Transition between 2 V to 20 V ⁽⁵⁾ | | | 70 | μs |
| | | Transition between 20 V to 4 V ⁽⁵⁾ | | | 70 | μs |
| | | Transition between 4 V to 20 V ⁽⁵⁾ | | | 50 | μs |

1. Measured at low frequency
2. $F_1 = 894\text{ MHz}$, $F_2 = 849\text{ MHz}$, $P_1 = +25\text{ dBm}$, $P_2 = +25\text{ dBm}$, $2f_1 - f_2 = 939\text{ MHz}$
3. $IP3$ and harmonics are measured in the shunt configuration in a $50\ \Omega$ environment
4. 850 MHz , $P_{IN} = +34\text{ dBm}$
5. One or both of RF_{IN} and RF_{OUT} must be connected to DC ground, using the HVDAC turbo mode. Transition time for tuner between $C_{min.}$ to 90% of $C_{max.}$ or $C_{max.}$ to 90% of $C_{min.}$ include MIPI order work time (trig with last MIPI CLK).

1.1 RF measurements

Figure 1. Capacitor variation versus bias voltage

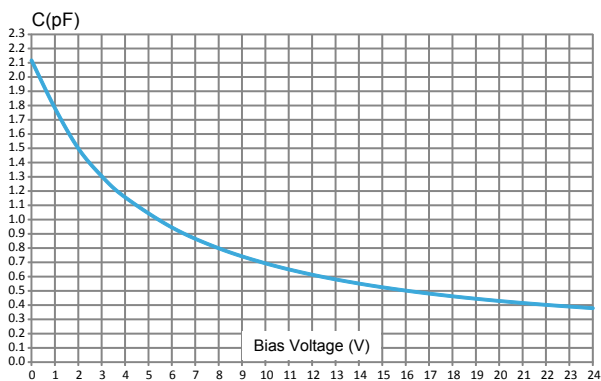


Figure 2. Quality factor versus frequency

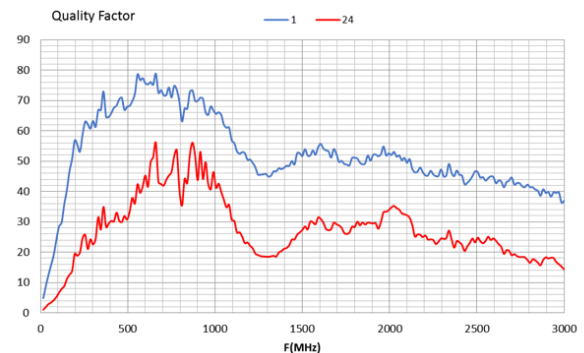


Figure 3. Harmonic power versus bias voltage (shunt)

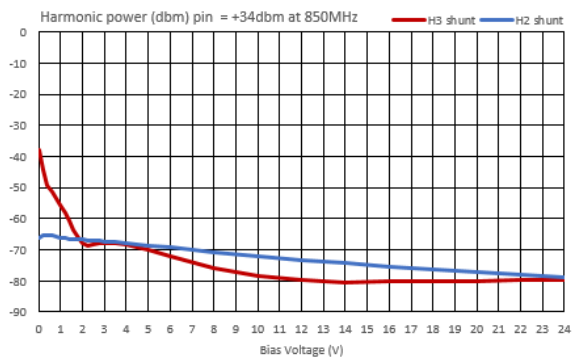


Figure 4. Harmonic power versus bias voltage (series)

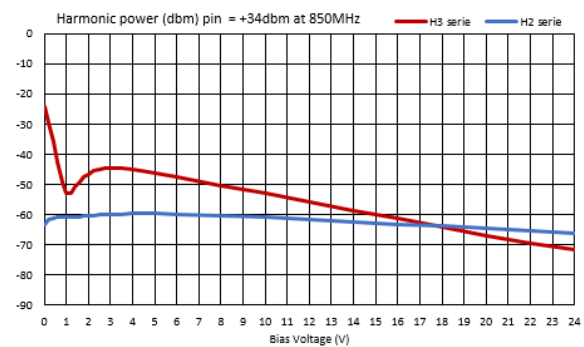
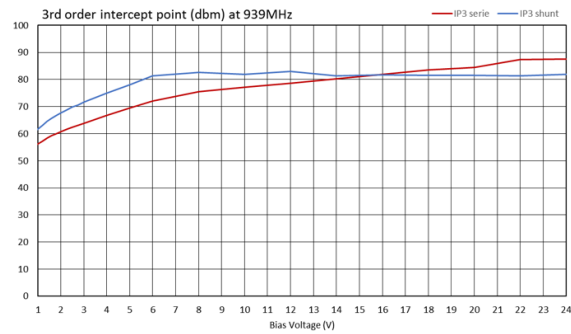
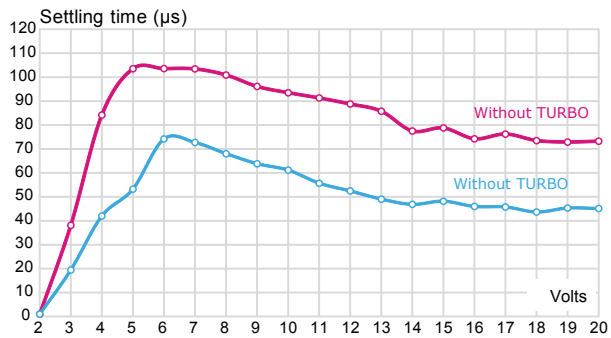
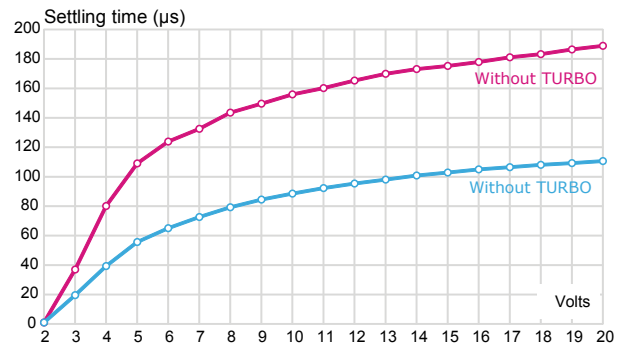


Figure 5. Third order intercept point (IP3)

Figure 6. Settling time from 2 V to V_{FINAL}

Figure 7. Settling time from V_{START} to 2 V


2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 WLCSP 3 solder bars package information

Figure 8. WLCSP 3 solder bars package outline

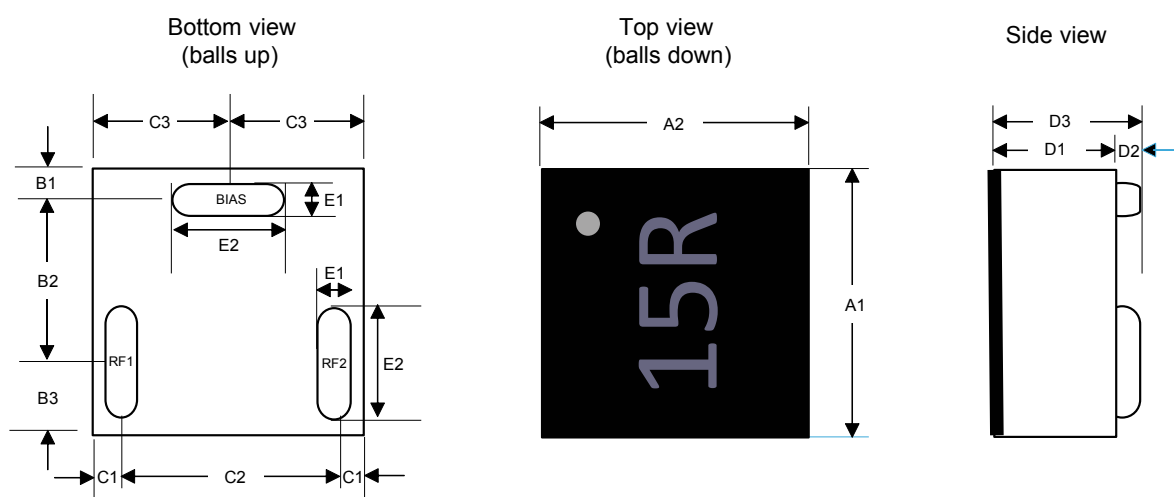


Table 4. WLCSP 3 solder bars package dimensions

| Dimensions | A1 | A2 | B1 | B2 | B3 | C1 | C2 | C3 | D1 | D2 | D3 | E1 | E2 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| STPTIC-15L2C4 | 720 | 750 | 100 | 420 | 200 | 100 | 550 | 375 | 225 | 90 | 315 | 125 | 300 |
| Tolerance | ±30 | ±30 | ±15 | ±10 | ±15 | ±15 | ±10 | ±15 | ±20 | ±25 | ±40 | ±25 | ±25 |

Figure 9. Recommended PCB land pattern for WLCSP 3 solder bars package

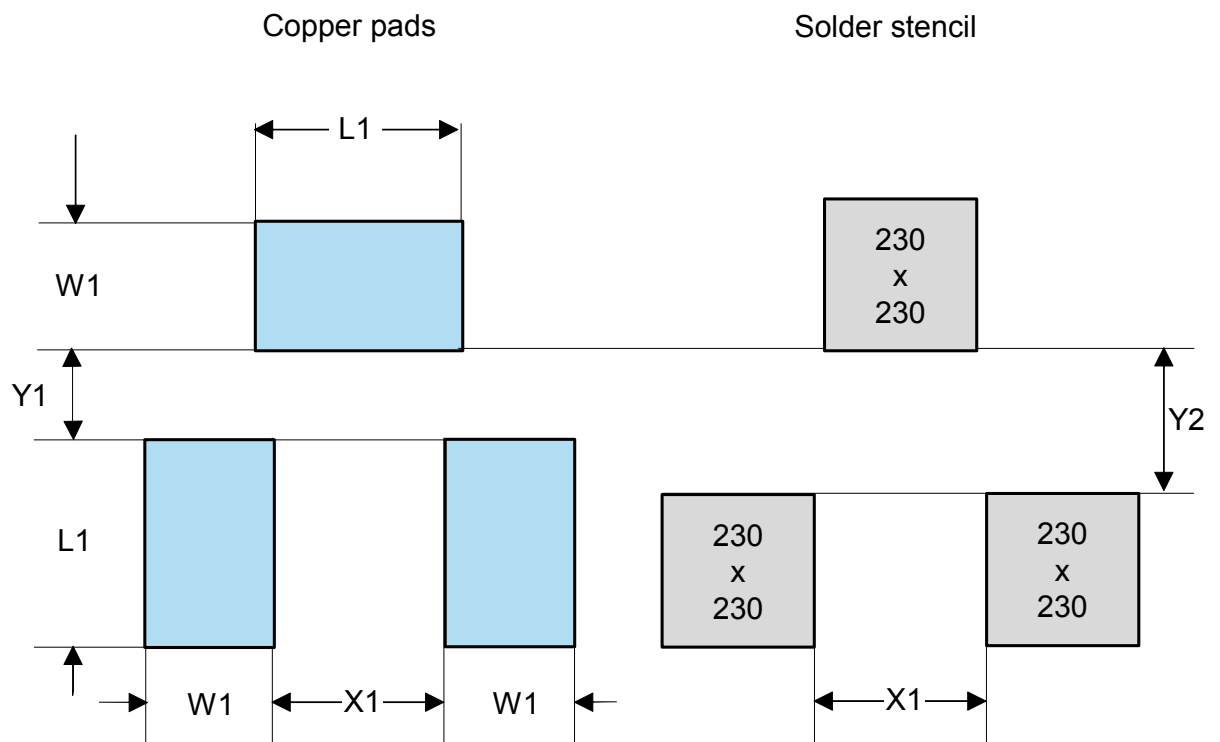


Table 5. Dimensions

| Ball | L1 | W1 | X1 | Y1 | Y2 |
|-----------------------------|-----|-----|-----|-----|-----|
| Typical values (in microns) | 300 | 200 | 270 | 130 | 200 |

2.2 Packing information

Figure 10. Tape and reel outline

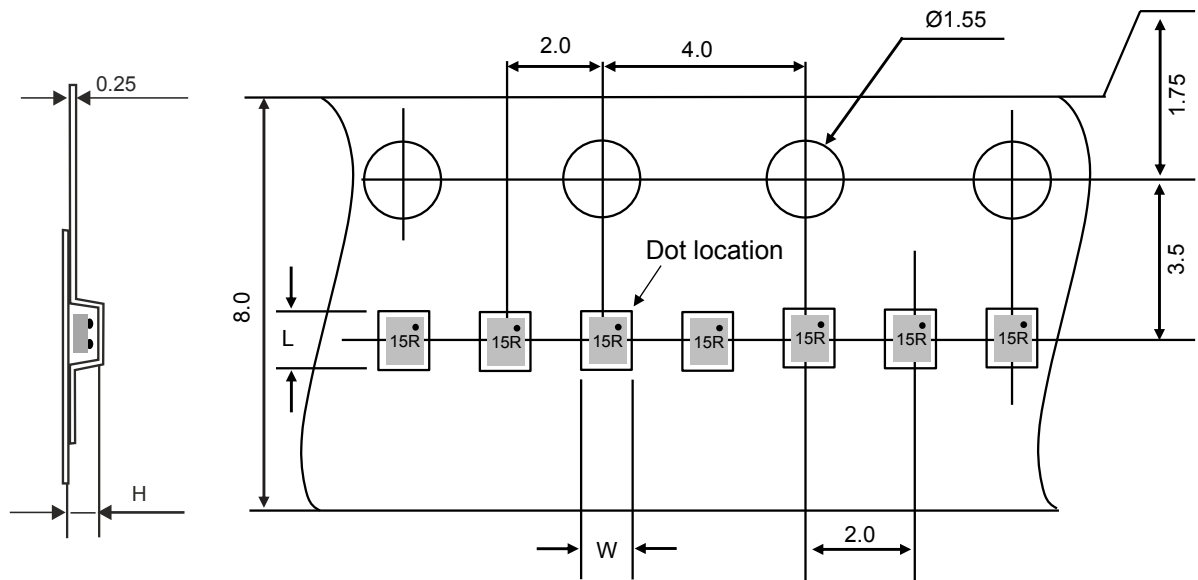


Table 6. Pocket dimensions

| Pocket dimensions | L | W | H |
|-------------------|-----|-----|-----|
| STPTIC-15L2C4 | 820 | 790 | 385 |

Figure 11. Marking

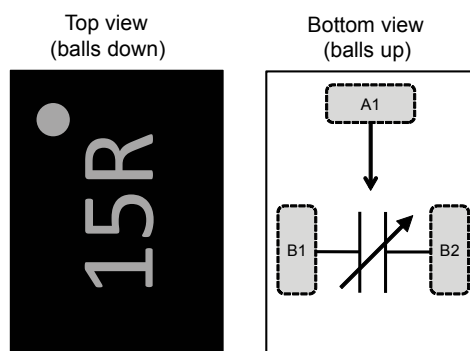


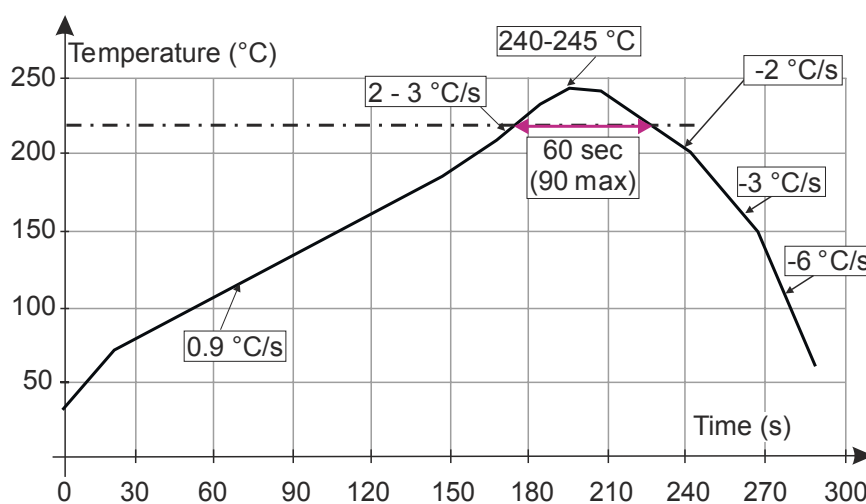
Table 7. Pinout description

| Pad / ball number | pin name | Description |
|-------------------|--------------------|-------------------|
| A1 | DC bias | DC bias voltage |
| B1 | RF1 | RF input / output |
| B2 | RF2 ⁽¹⁾ | RF input / output |

1. When connected in shunt, please connect RF2 (B2 ball) to GND

2.3 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 8. Recommended values for soldering reflow

| Profile | Value | |
|---|---------------|---------|
| | Typical | Max. |
| Temperature gradient in preheat (T = 70-180 °C) | 0.9 °C/s | 3 °C/s |
| Temperature gradient (T = 200-225 °C) | 2 °C/s | 3 °C/s |
| Peak temperature in reflow | 240-245 °C | 260 °C |
| Time above 220 °C | 60 s | 90 s |
| Temperature gradient in cooling | -2 to -3 °C/s | -6 °C/s |
| Time from 50 to 220 °C | 160 to 220 s | |

3 Evaluation board

Figure 13. Series and shunt connection

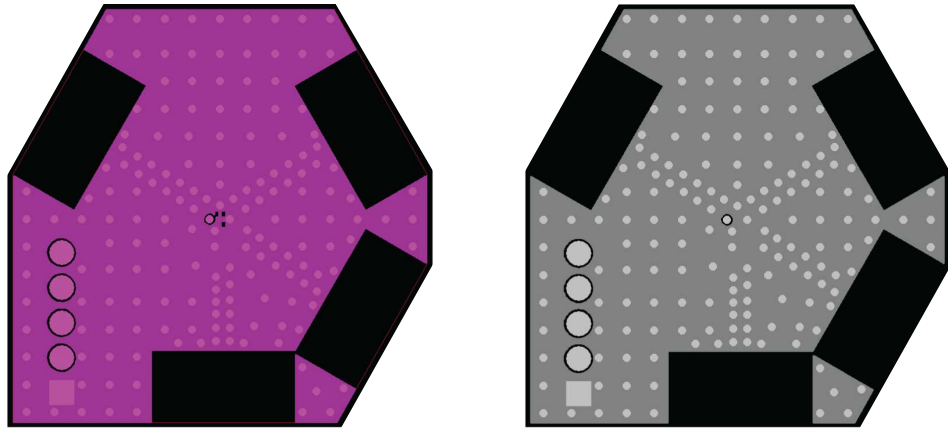


Figure 14. Layer 1 and layer 4

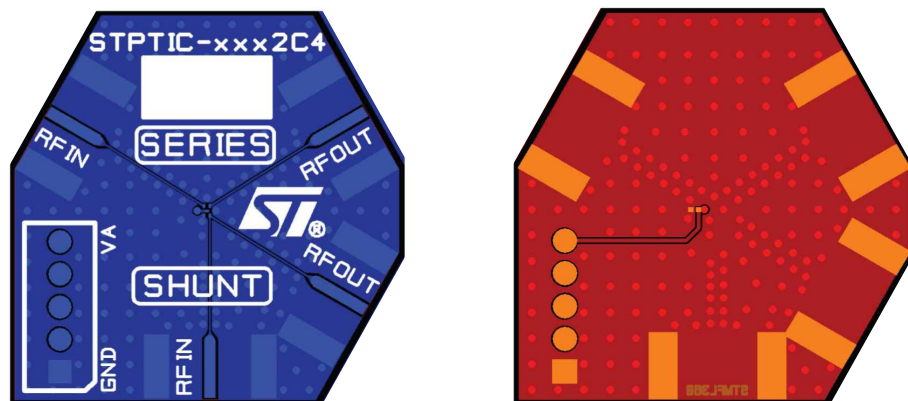
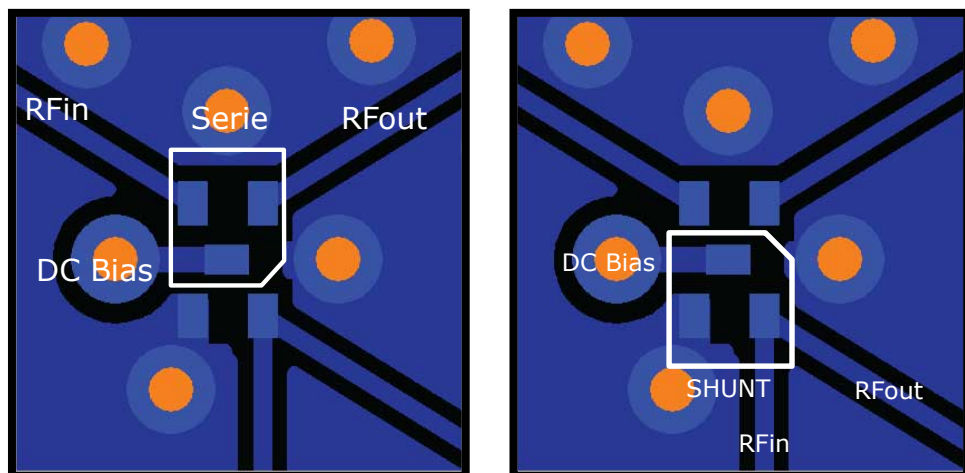


Figure 15. Layer 2 and layer 3





4 Ordering information

Figure 16. Ordering information scheme

| | | | | | | |
|------------------------|---|---|--|---|----------------------------------|---|
| ST | PTIC | - | 15 | L | 2 | C4 |
| <u>Manufacturer</u> | <u>Product family</u> | - | <u>Capacitor value</u> | <u>Linearity</u> | <u>Tuning</u> | <u>Package</u> |
| ST Microelectronics | PTIC Parascan™ tunable Integrated capacitor | | 15 = 1.5 pF 27 = 2.7 pF 33 = 3.3 pF 39 = 3.9 pF 47 = 4.7 pF 56 = 5.6 pF 68 = 6.8 pF 82 = 8.2 pF | F: Standard (x24) G: Standard (x24) L: High (x48) | 1 = 4/1 tuning 2 = 5/1 tuning | M6 : QFN C5 : WLCSP 400 µm coating C4 : WLCSP 3 solder bars |

Table 9. Ordering information

| Order code | Marking | Base qty. | Package | Delivery mode |
|---------------|---------|-----------|---------------------|---------------|
| STPTIC-15L2C4 | 15R | 15 000 | WLCSP 3 solder bars | Tape and reel |



Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 03-Jul-2018 | 1 | Initial release. |

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