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Kind regards,

Team Nexperia



PBSS4032ND

30 V, 3.5 A NPN low V_{CEsat} (BISS) transistor Rev. 01 — 30 January 2010

Product data sheet

Product profile

1.1 General description

NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

PNP complement: PBSS4032PD.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- Optimized switching time
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High energy efficiency due to less heat generation
- AEC-Q101 qualified
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- Battery-driven devices
- Power management
- Charging circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	30	V
I _C	collector current		-	-	3.5	Α
I _{CM}	peak collector current	$\begin{array}{l} \text{single pulse;} \\ t_p \leq 1 \text{ ms} \end{array}$	-	-	6	Α
R _{CEsat}	collector-emitter saturation resistance	$I_{C} = 4 \text{ A};$ $I_{B} = 400 \text{ mA}$	<u>[1]</u> _	50	75	mΩ

[1] Pulse test: $t_p \le 300~\mu s;~\delta \le 0.02.$



2. Pinning information

Table 2. Pinning

	3		
Pin	Description	Simplified outline	Graphic symbol
1	collector	G. G. G.	
2	collector	<u> </u>	1, 2, 5, 6
3	base		3 —
4	emitter	1 12 13	
5	collector		4 sym014
6	collector		<i>5,</i>

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4032ND	SC-74	plastic surface-mounted package; 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4032ND	ZF

5. Limiting values

Table 5. Limiting values

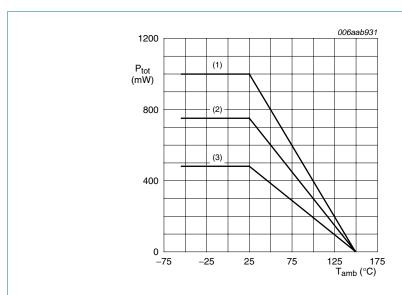
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	30	V
V_{CEO}	collector-emitter voltage	open base	-	30	V
V_{EBO}	emitter-base voltage	open collector	-	5	V
I _C	collector current		-	3.5	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	6	Α
I _B	base current		-	0.5	Α

Table 5. Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	$T_{amb} \leq 25~^{\circ}C$	<u>[1]</u> -	480	mW
			[2] -	750	mW
			[3] _	1	W
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		–55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



- (1) Ceramic PCB, Al₂O₃, standard footprint
- (2) FR4 PCB, mounting pad for collector 6 cm²
- (3) FR4 PCB, standard footprint

Fig 1. Power derating curves

Thermal characteristics 6.

Table 6. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
· -ui(j-a)	thermal resistance from	in free air	<u>[1]</u> -	-	260	K/W
	junction to ambient		[2] _	-	160	K/W
			<u>[3]</u> _	-	125	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	45	K/W

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

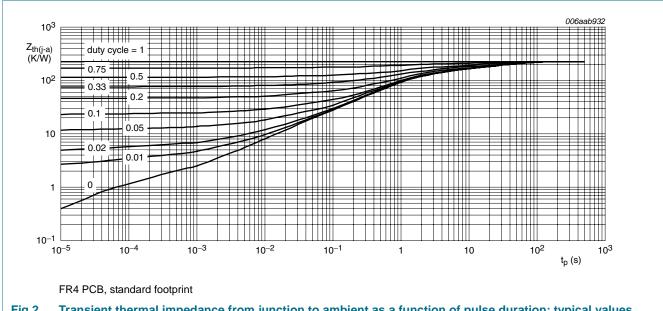


Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

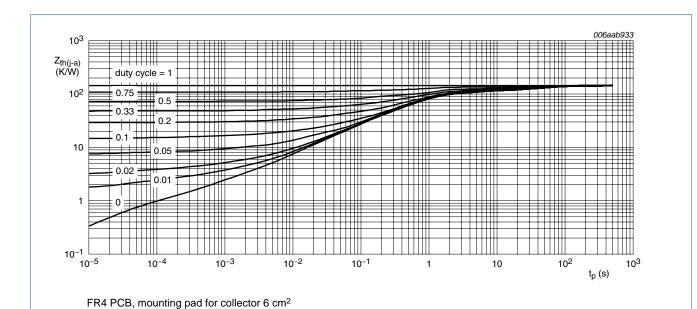


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

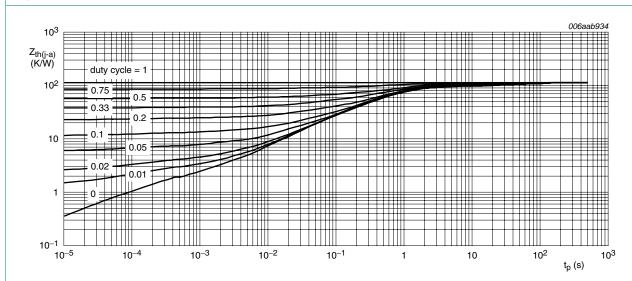


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

Ceramic PCB, Al₂O₃, standard footprint

7. Characteristics

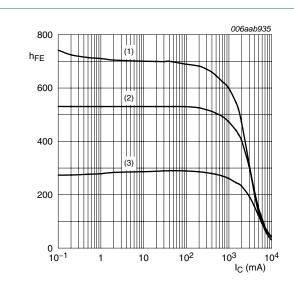
Table 7. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
I _{CBO}	collector-base cut-off	$V_{CB} = 30 \text{ V}; I_{E} = 0 \text{ A}$		-	-	100	nΑ
	current	$V_{CB} = 30 \text{ V; } I_E = 0 \text{ A;}$ $T_j = 150 \text{ °C}$		-	-	50	μА
I _{CES}	collector-emitter cut-off current	$V_{CE} = 24 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	100	nA
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$		-	-	100	nA
h _{FE} DC current gain		$V_{CE} = 2 \text{ V}; I_{C} = 500 \text{ mA}$	[1]	300	500	-	
		V _{CE} = 2 V; I _C = 1 A	[1]	300	460	-	
		$V_{CE} = 2 \text{ V}; I_{C} = 2 \text{ A}$	[1]	250	400	-	
		V _{CE} = 2 V; I _C = 4 A	[1]	120	200	-	
		$V_{CE} = 2 \text{ V}; I_{C} = 6 \text{ A}$	[1]	60	100	-	
V_{CEsat}	collector-emitter	$I_C = 500 \text{ mA}; I_B = 50 \text{ mA}$	[1]	-	70	100	mV
	saturation voltage	$I_C = 1 A$; $I_B = 50 \text{ mA}$	[1]	-	110	155	mV
		I _C = 1 A; I _B = 10 mA	[1]	-	155	220	mV
		$I_C = 2 \text{ A}; I_B = 40 \text{ mA}$	[1]	-	180	250	mV
		$I_C = 3 A$; $I_B = 300 \text{ mA}$	[1]	-	180	250	mV
	$I_C = 4 \text{ A}; I_B = 400 \text{ mA}$	[1]	-	200	300	mV	
R _{CEsat}	collector-emitter saturation resistance	$I_C = 4 \text{ A}; I_B = 400 \text{ mA}$	[1]	-	50	75	mΩ
V_{BEsat}	base-emitter	$I_C = 1 A$; $I_B = 100 \text{ mA}$	[1]	-	0.78	0.9	V
	saturation voltage	$I_C = 3 \text{ A}; I_B = 300 \text{ mA}$	[1]	-	0.98	1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2 \text{ V}; I_{C} = 2 \text{ A}$		-	0.79	0.85	V
t _d	delay time	$V_{CC} = 12.5 \text{ V}; I_C = 1 \text{ A};$		-	23	-	ns
t _r	rise time	$I_{Bon} = 0.05 \text{ A};$ $I_{Boff} = -0.05 \text{ A}$		-	25	-	ns
t _{on}	turn-on time	IROII — _0.00 K		-	48	-	ns
ts	storage time			-	140	-	ns
t _f	fall time			-	65	-	ns
t _{off}	turn-off time			-	205	-	ns
f _T	transition frequency	$V_{CE} = 10 \text{ V};$ $I_{C} = 100 \text{ mA};$ f = 100 MHz		-	135	-	MHz
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	44	-	pF

^[1] Pulse test: $t_p \leq 300~\mu s;~\delta \leq 0.02.$

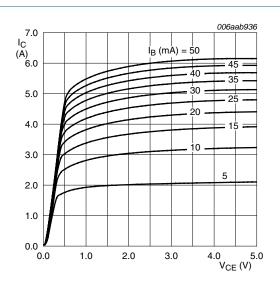
30 V, 3.5 A NPN low V_{CEsat} (BISS) transistor



$$V_{CE} = 2 V$$

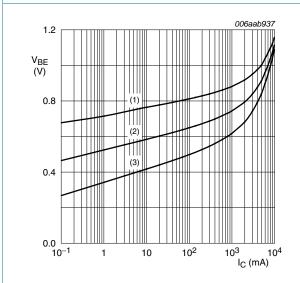
- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -55 \, ^{\circ}C$

Fig 5. DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

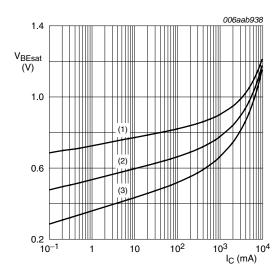
Fig 6. Collector current as a function of collector-emitter voltage; typical values





- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

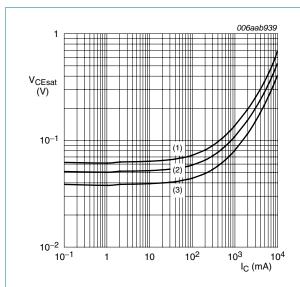
Fig 7. Base-emitter voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

- (1) $T_{amb} = -55 \,^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = 100 \, ^{\circ}C$

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



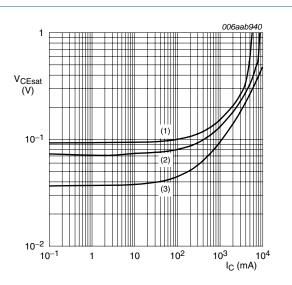
$$I_{\rm C}/I_{\rm B}=20$$

(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3) $T_{amb} = -55 \, ^{\circ}C$

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



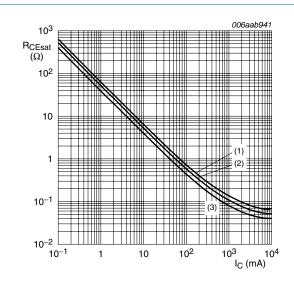
$$T_{amb} = 25 \, ^{\circ}C$$

(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B} = 20$

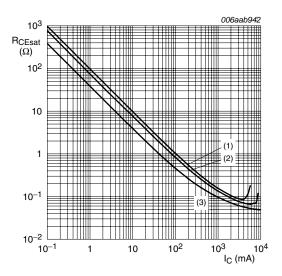
(1)
$$T_{amb} = 100 \, ^{\circ}C$$

(2)
$$T_{amb} = 25 \, ^{\circ}C$$

(3)
$$T_{amb} = -55 \, ^{\circ}C$$

Product data sheet

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



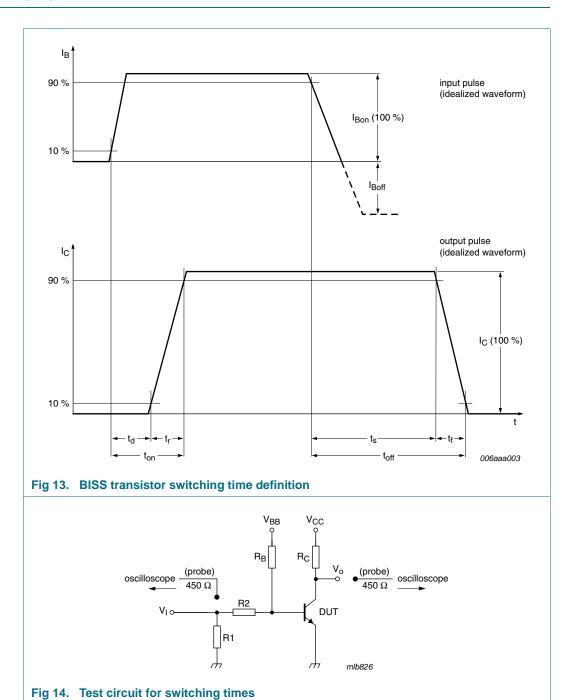
(1)
$$I_C/I_B = 100$$

(2)
$$I_C/I_B = 50$$

(3)
$$I_C/I_B = 10$$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

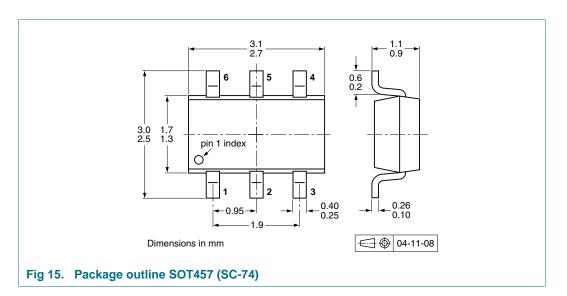
8. Test information



8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

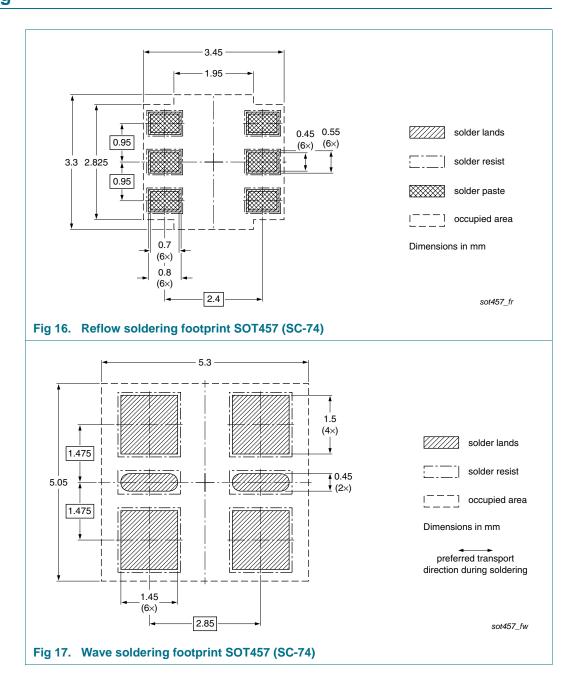
Type number	Package	Description		Packing quantity	
				3000	10000
PBSS4032ND	SOT457	4 mm pitch, 8 mm tape and reel	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel	[3]	-215	-235

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering



PBSS4032ND

30 V, 3.5 A NPN low V_{CEsat} (BISS) transistor

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4032ND_1	20100130	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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PBSS4032ND

30 V, 3.5 A NPN low V_{CEsat} (BISS) transistor

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