

N-channel 650 V, 0.35 Ω typ., 12 A MDmesh™ II Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

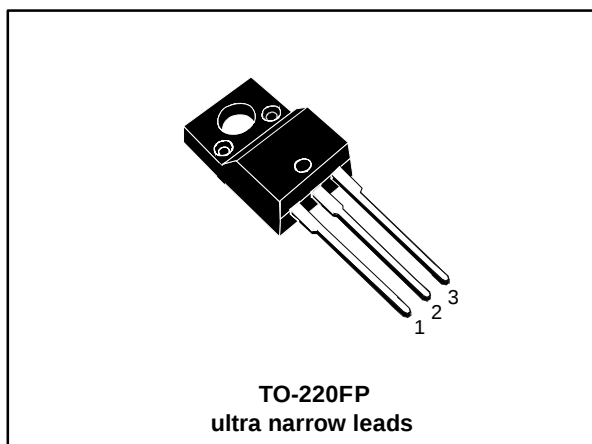
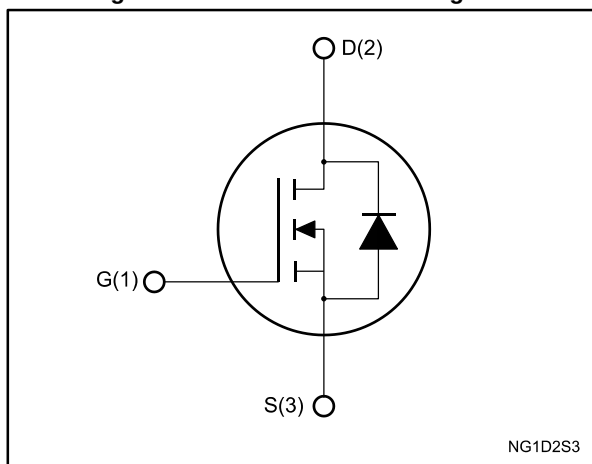


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STFU15NM65N	650 V	0.38 Ω	12 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STFU15NM65N	15NM65N	TO-220FP ultra narrow leads	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuit	8
4	Package information	9
	4.1 TO-220FP ultra narrow leads package information.....	9
5	Revision history	11

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	650	V
V_{GS}	Gate source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	12 ⁽¹⁾	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	7.56	
I_{DM} ⁽²⁾	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:⁽¹⁾Limited by maximum junction temperature.⁽²⁾Pulse width limited by safe operating area.⁽³⁾ $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.17	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	187	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	650			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 650 V			1	μA
		V _{DS} = 650 V, T _C = 125 °C			100	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			±100	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 6 A		0.35	0.38	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	983	-	pF
C _{oss}	Output capacitance		-	57	-	
C _{rss}	Reverse transfer capacitance		-	4.5	-	
C _{oss eq. (1)}	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	146	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.9	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 12 A, V _{GS} = 10 V	-	33.3	-	nC
Q _{gs}	Gate-source charge		-	5.7	-	
Q _{gd}	Gate-drain charge		-	17	-	

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 6 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	55.5	-	ns
t _r	Rise time		-	8.5	-	
t _{d(off)}	Turn-off delay time		-	14	-	
t _f	Fall time		-	11.4	-	

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$	-	428		ns
Q_{rr}	Reverse recovery charge		-	4.7		μC
I_{RRM}	Reverse recovery current		-	21.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	570		ns
Q_{rr}	Reverse recovery charge		-	6.2		μC
I_{RRM}	Reverse recovery current		-	22		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

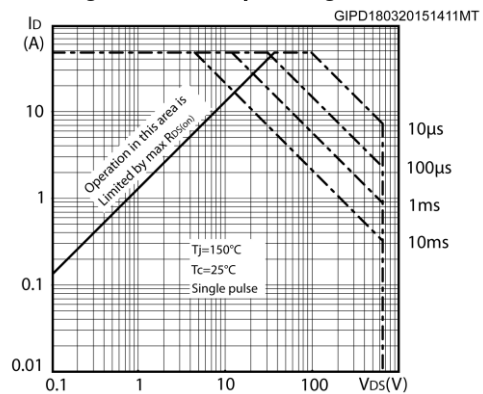


Figure 3: Thermal impedance

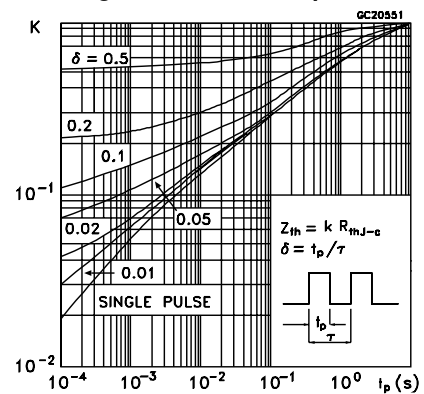


Figure 4: Output characteristics

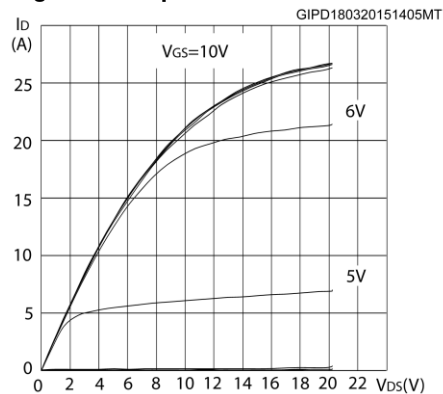


Figure 5: Transfer characteristics

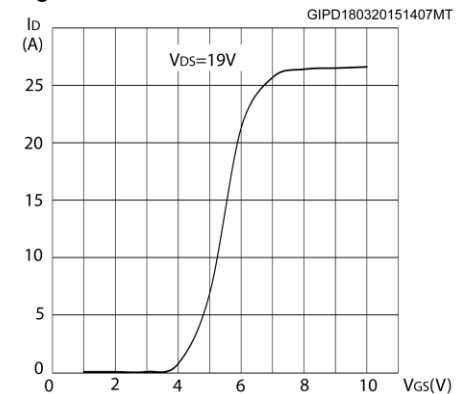


Figure 6: Static drain-source on-resistance

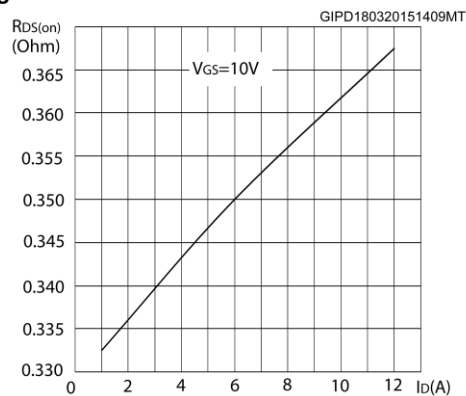


Figure 7: Gate charge vs gate-source voltage

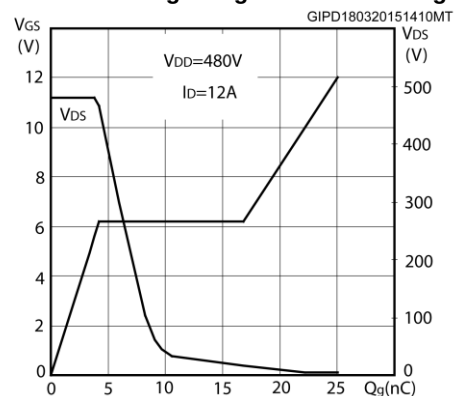


Figure 8: Capacitance variations

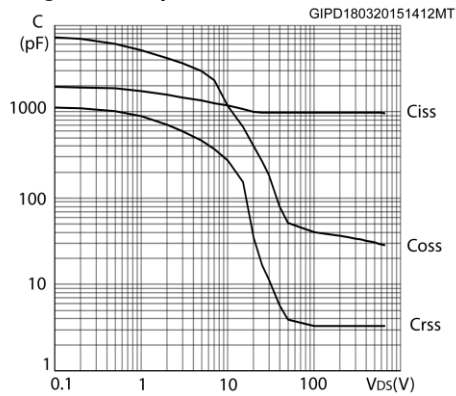


Figure 9: Normalized gate threshold voltage vs temperature

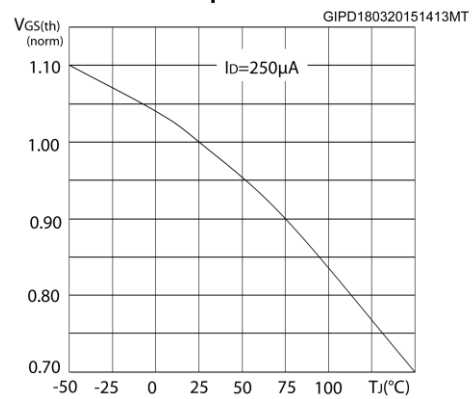


Figure 10: Normalized on-resistance vs temperature

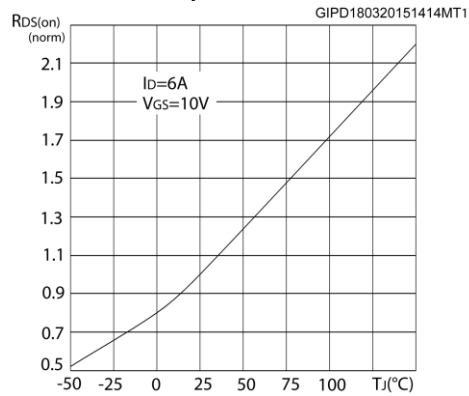
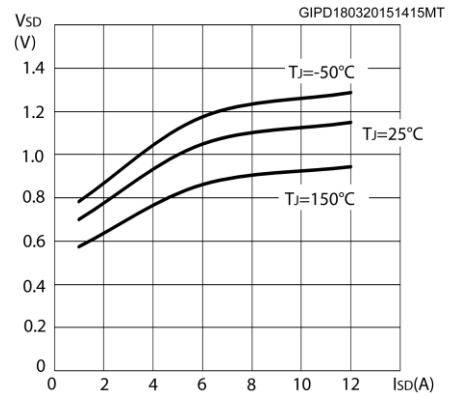
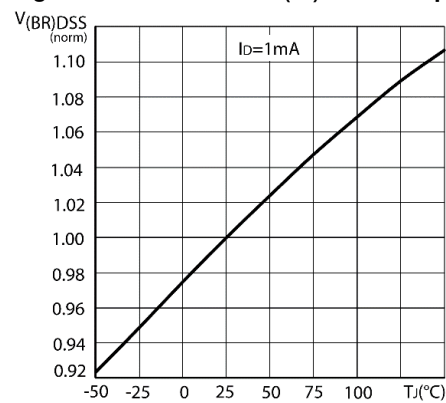


Figure 11: Source-drain diode forward characteristics

Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

3 Test circuit

Figure 13: Test circuit for resistive load switching times

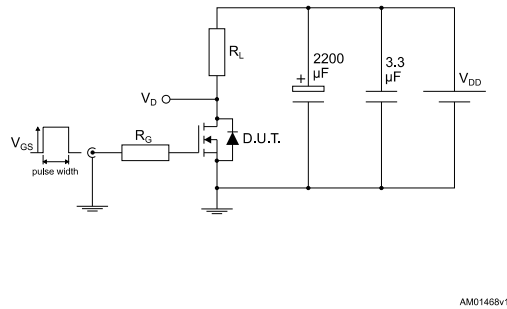


Figure 14: Test circuit for gate charge behavior

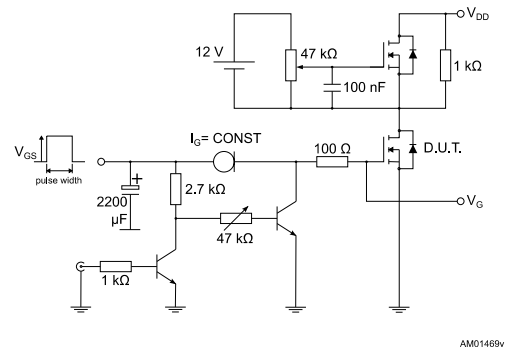


Figure 15: Test circuit for inductive load switching and diode recovery times

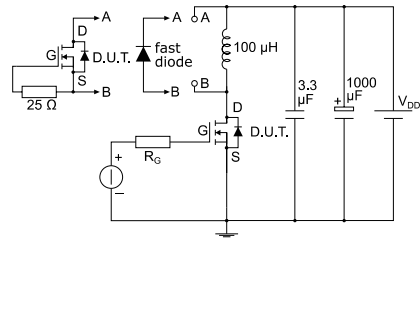


Figure 16: Unclamped inductive load test circuit

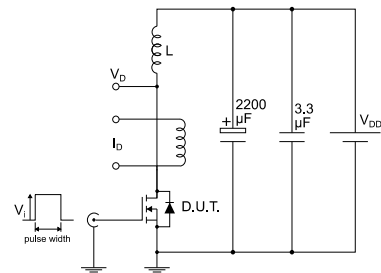


Figure 17: Unclamped inductive waveform

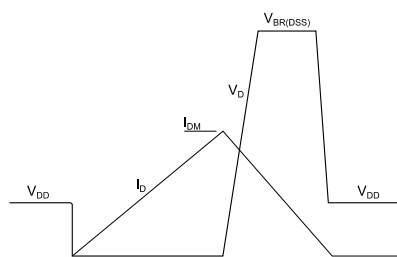
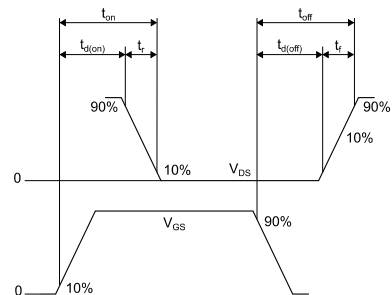


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 19: TO-220FP ultra narrow leads package outline

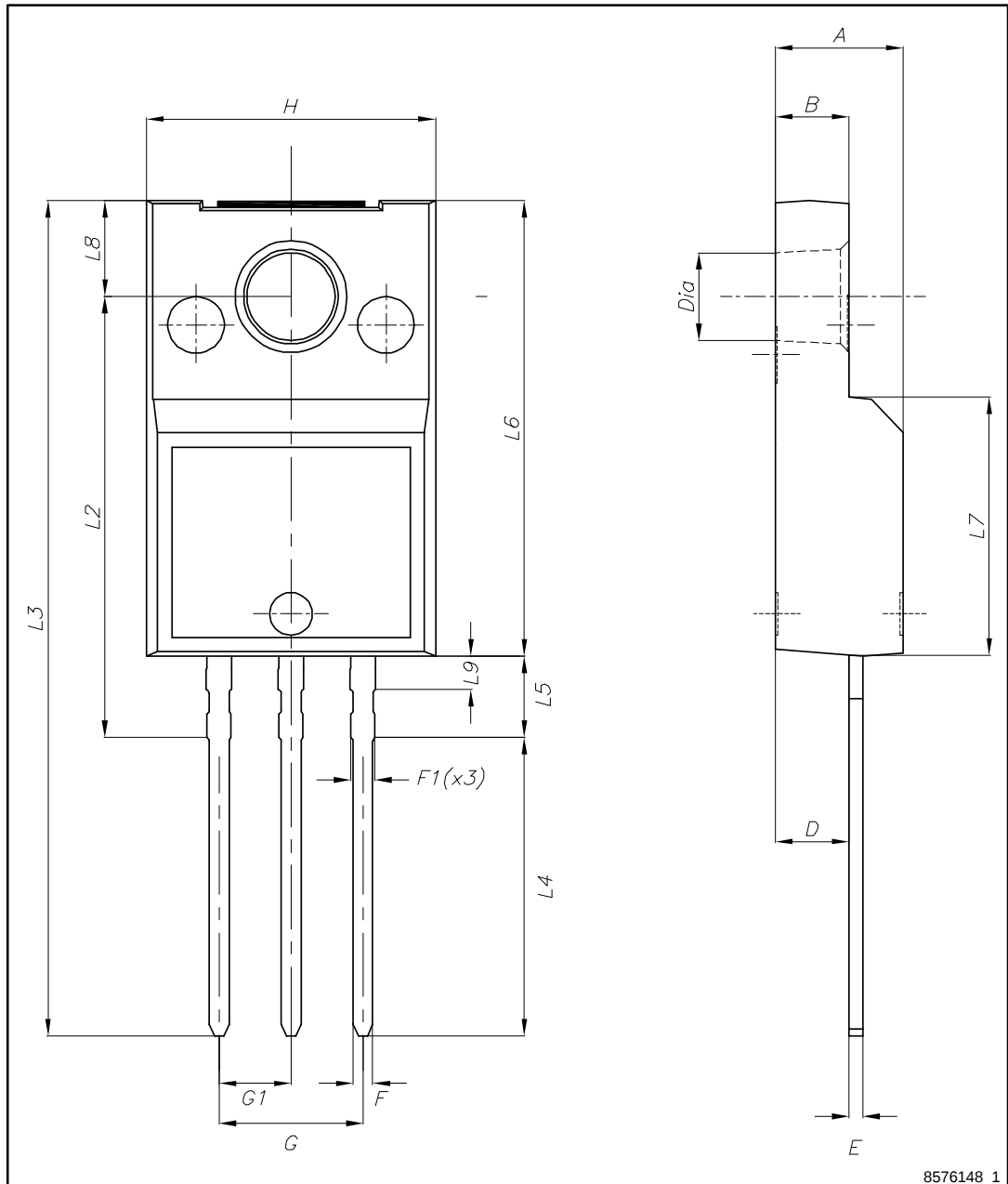


Table 9: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
16-Mar-2015	1	Initial release
09-Sep-2015	2	Datasheet status promoted from preliminary to production data.

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