Bluetooth Class 2 Module MBH7BTZ43 Datasheet

Rev.0.11
Mar 10, 2010

Fujitsu Component Limited

All specifications are preliminary which may be changed without any prior notice

1. Summary

This datasheet applies to the Bluetooth® Module MBH7BTZ43.

2. Features

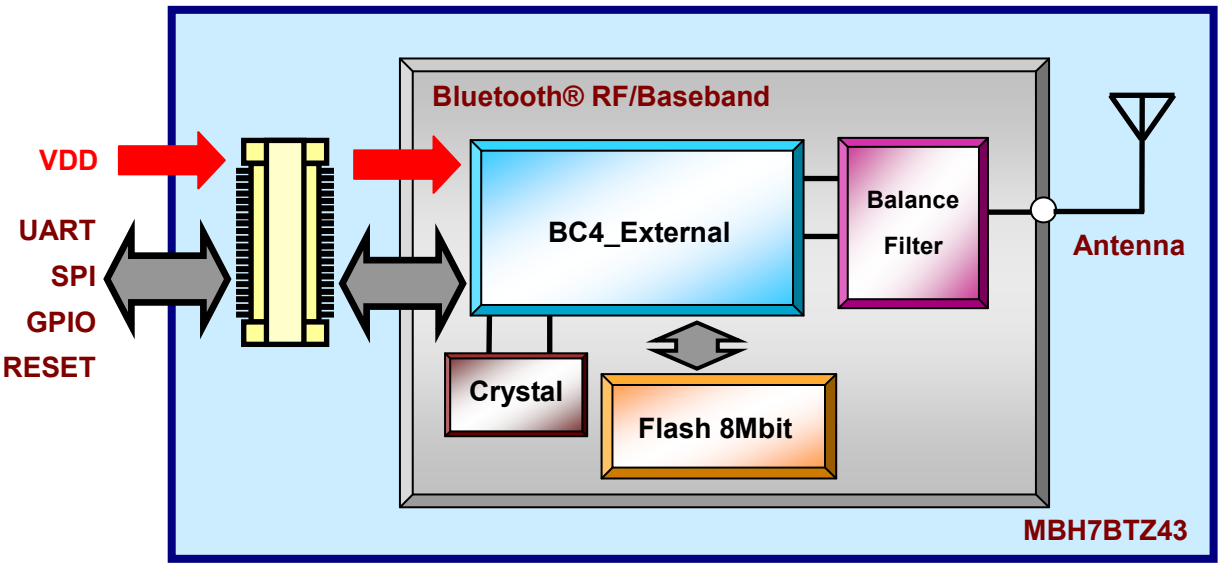
This module is an antenna integrated Board-to-board connector type module with Bluetooth® wireless technology for embedded applications. This module is compliant with Bluetooth® Specification Version 2.1 + EDR and supports Power Class 2 (+4 dBm maximum).
Since the upper level protocol stacks and Serial Port Profile (SPP) are incorporated in this module, users can control Bluetooth® through text-based simple commands. Therefore, this module is the most suitable cable replacement solution for electronic devices that are connected via serial cable, and users can reduce development time and cost to develop Bluetooth® enabled applications.
The followings are the detailed features.

- Bluetooth® Specification Version 2.1 + EDR Compliant
- CSR BlueCore4-External based
- Upper layer protocol stack (L2CAP, SDP, RFCOMM) and profiles (GAP, SDAP, SPP) are incorporated in the module
- Output Power: Class 2 (+4 dBm maximum)
- Hardware Interface: UART
- Software Interface: SPP (FCL proprietary commands/events)
- Power Supply: 2.7 ~ 3.6V
  (It is recommended that LDO regulator is used as power supply.)
- I/O Power supply: 1.7 ~ 3.6V
- RoHS compliant
- Board-to-board connector system
- Small footprint (22.5 mm x 10.6 mm x 2.3 mm)
- Integrated antenna

3. Applicable Standard

- Bluetooth® Specification Version 2.1 + EDR

4. Block Diagram



5. Electrical Characteristics

5-1. General Features

Bluetooth® Specification Version 2.1 + EDR Compliant

Carrier Frequency:	2400 MHz ~ 2483.5 MHz
Modulation:	・0.5BT Gaussian-filtered 2FSK Modulation Index 0.28 ~ 0.35(Basic Rate 1 Mbps) ・π/4-DQPSK (EDR 2 Mbps) ・8DPSK (EDR 3 Mbps)
Symbol Rate:	1 Mbps
Data Rate:	1 Mbps (Basic Rate) 2 Mbps (EDR 2Mbps) 3 Mbps (EDR 3Mbps)
Channel:	79 channels
Channel Spacing:	1 MHz
Output power:	Power Class 2

5-2. Absolute Maximum Rating

Items	Symbol	Min	Max	Unit
VDD	Vdd_reg	-0.3	3.7	V
Input Voltage	Vin	GND-0.4	Vdd+0.4	V
Storage Temperature	Tstg	-40	+85	°C

5-3. Recommendable Operating Condition

Items	Symbol	Min	Typ	Max	Unit
VDD	Vdd_reg	2.7	3.0	3.6	V
Operating Temperature	Topr	-20	-	+70	°C

5-4. I/O Terminal Characteristics

Items	Symbol	Min	Typ	Max	Unit
Input Logic Level Low (Vdd = 2.7 ~ 3.0V)	V_{IL}	-0.4	-	0.8	V
Input Logic Level Low (Vdd = 1.7 ~ 1.9V)	V_{IL}	-0.4	-	0.4	V
Input Logic Level High	V_{IH}	0.7Vdd	-	Vdd+0.4	V
Output Logic Level Low (Vdd = 2.7 ~ 3.0V) I_O = 4.0mA	V_{OL}	-	-	0.2	V
Output Logic Level Low (Vdd = 1.7 ~ 1.9V) I_O = 4.0mA	V_{OL}	-	-	0.4	V
Output Logic Level High (Vdd = 2.7 ~ 3.0V) I_O = -4.0mA	V_{OH}	Vdd-0.2	-	-	V
Output Logic Level High (Vdd = 1.7 ~ 1.9V) I_O = -4.0mA	V_{OH}	Vdd-0.4	-	-	V
I/O pad leakage current	I_{OZL}	-1	0	1	µA
Input Capacitance	C_I	1.0	-	5.0	pF

5-5. Power Consumption

Vdd = 3.0V, Ta = 25±2°C

Mode	Condition	Typ	Max *2	Unit
Deep sleep		30	80	uA
Basic Rate transmitting *1	packet type DH5	44	60	mA
Basic Rate receiving *1	packet type DH5	47	60	mA
Enhanced Data Rate transmitting *1	packet type 3DH5	54	70	mA
Enhanced Data Rate receiving *1	packet type 3DH5	57	70	mA

*1) Measured in the condition connected to Bluetooth Tester Anritsu MT8852B.

*2) Inrush current is not included in the maximum rating.

5-6. Transmitter Specification

Basic Data Rate *1

Items	Condition	Min	Typ	Max	Unit
Maximum RF Transmit Power		-6	2	4	dBm
Step Size of RF Power Control		2	-	8	dB
20dB Bandwidth for Modulated Carrier		-	-	1	MHz
Initial Carrier Frequency Tolerance	DH1mode	-75	-	+75	kHz
Carrier Frequency Drift	1 Slot 3 Slot 5 Slot	-25 -40 -40	- - -	+25 +40 +40	kHz kHz kHz
Modulation	8 bit sequence 01010101	±115	-	-	kHz
	8 bit sequence 00001111 (average)	±140	-	±175	kHz
Adjacent Channel Power	|M-N|=2 |M-N|>=3	- -	- -	-20 -40	dBm dBm
Out-of-Band Spurious Emissions	30 MHz --- 1 GHz 1 GHz --- 12.75 GHz 1.8 GHz --- 1.9 GHz 5.15 GHz --- 5.3 GHz	- - - -	- - - -	-36 -30 -47 -47	dBm dBm dBm dBm

*1) Measured according to Bluetooth specification

Enhanced Data Rate [*1]

Items		Condition	Min	Typ	Max	Unit
EDR Relative Transmit Power (GFSK-DPSK)			-4	-	1	dB
EDR Carrier Frequency Stability [π/4-DQPSK and 8DPSK]	Wi		-75	-	75	kHz
	Wi+Wo		-75	-	75	kHz
	Wo		-10		10	kHz
Modulation [π/4-DQPSK]		RMS DEVM	-	-	20	%
		Peak DEVM	-	-	35	%
		99% DEVM	-	-	30	%
Modulation [8DPSK]		RMS DEVM	-	-	13	%
		Peak DEVM	-	-	25	%
		99% DEVM	-	-	20	%

*1) Measured according to Bluetooth specification

5-7. Receiver Specification

Basic Data Rate [*1]

Items	Condition	Min	Typ	Max	Unit
Receiver Sensitivity Level	0.1% BER		-87	-70	dBm
Sensitivity (Single slot packets)	Input level = -70 dBm DH1 mode	-	-	0.1	%
Sensitivity (multi-slot packets)	Input level= -70 dBm DH5 mode	-	-	0.1	%
C/I Performance		-	-	0.1	%
Blocking Performance	30 MHz ~ 12.75 GHz Interference signal	-	-	0.1	%
Intermodulation Performance	5th order intermodulation	-	-	0.1	%
Maximum Input Level	Input level = -20 dBm	-	-	0.1	%

*1) Measured according to Bluetooth specification

Enhanced Data Rate [*1]

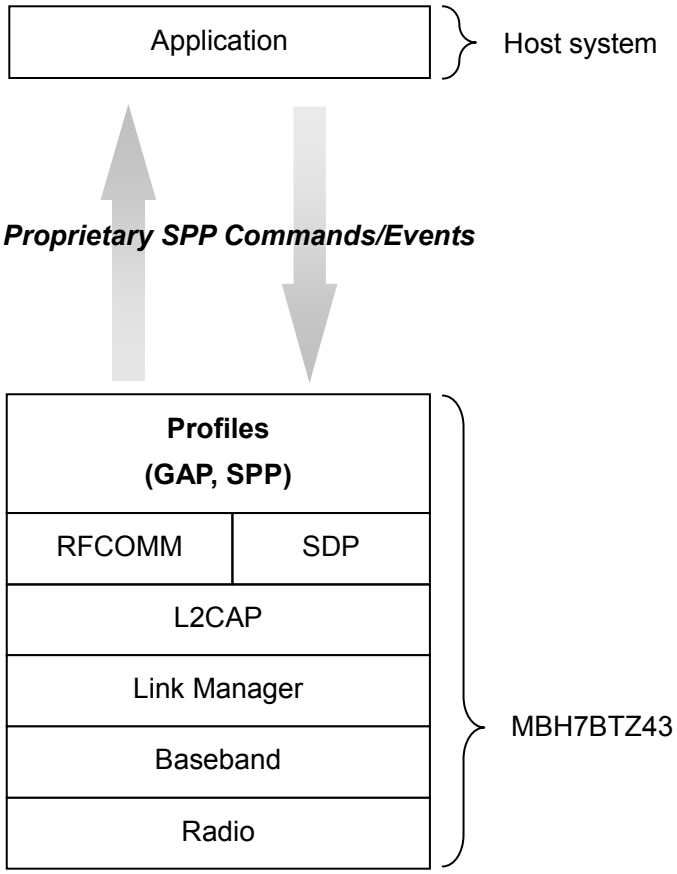
Items	Condition	Min	Typ	Max	Unit
Receiver Sensitivity Level at 0.01% BER	π/4 DQPSK		-88	-70	dBm
	8DPSK		-81	-70	dBm
Maximum Receiver Input Level (Input Level = -20 dBm)	π/4 DQPSK	-	-	0.1	%
	8DPSK	-	-	0.1	%

*1) Measured according to Bluetooth specification

6. Interface Specification

6-1. Host Connection

This module connects to Host via UART, and it is operated with our proprietary SPP commands and events.



6-2. UART Interface

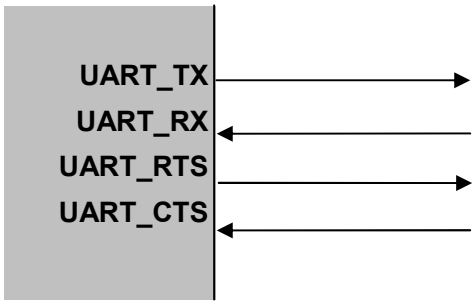


Figure 6-2-1: UART Interface

Four signals are used to implement the UART (Universal Asynchronous Receiver Transmitter) function, as shown in Figure 6-2-1. When this module is connected to Host, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement hardware flow control where both are active low indicators.

1) When this module cannot receive data anymore, it outputs “High” to UART_RTS (Request To Send).
2) This module transmits data only when the input from UART_CTS is ”Low”.

All UART connections are CMOS level and have signaling levels of 0V and VDD_USB.
UART configuration parameters, such as baud rate, can be changed.
Possible UART settings are listed in Table 6-2-1

Table 6-2-1: UART Setting

Item	Possible Values
Baud Rate	9.6k, 19.2k, 38.4k, 57.6k, 115.2k, 230.4k, 460.8k, 921.6k, 1,382.4k
Flow Control	Hardware flow control (RTS/CTS)
Parity bit	None
Number of Stop Bits	1

The UART interface is capable of resetting this module upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX signal. A break signal can be used to wake up this module from Deep Sleep mode.

Note: When the baud rate is set to 19.2kbps or less, Deep Sleep must be disabled. If Deep Sleep is enabled, there is a possibility that the output data from this module is corrupted.

6-3. Deep Sleep

This module enters into deep sleep mode as much as possible to save power consumption when it is in disconnected state or power saving mode (sniff, park, hold).
As at least 10 msec is required to wake up from deep sleep mode, some data may be dropped if the data is sent to UART of this module when deep sleep mode.
To prevent data dropping, user can send break signal by keeping UART_RX low for more than 10 msec.
This module enters into deep sleep mode again if no data is received for 20 msec.
Therefore user must transmit data within 20 msec after sending last data or the break signal.
In addition, it is possible to configure this module not to enter into the deep sleep mode.

The followings are conditions for this module to be able to enter into deep sleep mode.

1. This module is in disconnected state or low power consumption mode (sniff, park, hold).
2. “High” level is not inputted to UART_CTS at boot-up.
3. SPI_CSB shall not be “Low” level.

* In the default setting, Deep Sleep is configured to be disabled.

When normal operation, SPI_CSB must be “High” level to prevent the firmware being damaged.

6-4. Transmission delay

There is longish transmission delay compared to wired link.
Therefore, if user adopts the protocol which needs returning ACK frequently, the delay will accumulate, and the throughput may fall remarkably.
If you are planning to replace the existing wired serial communication system by Bluetooth, you should test for compatibility.

6-5. Boot sequence

Until the initialization is completed, please never turn off the power supply nor reset to avoid the firmware corruption after turning on the power or resetting.

The completion of initialization can be detected by the following boot message.

- Reception of boot message "Welcome␣to␣FCL␣SPP␣Module␣!!".

*If your system cannot detect this boot message, you should wait at least 10 seconds for initialization.

When the write operation is not performed on the flash memory.

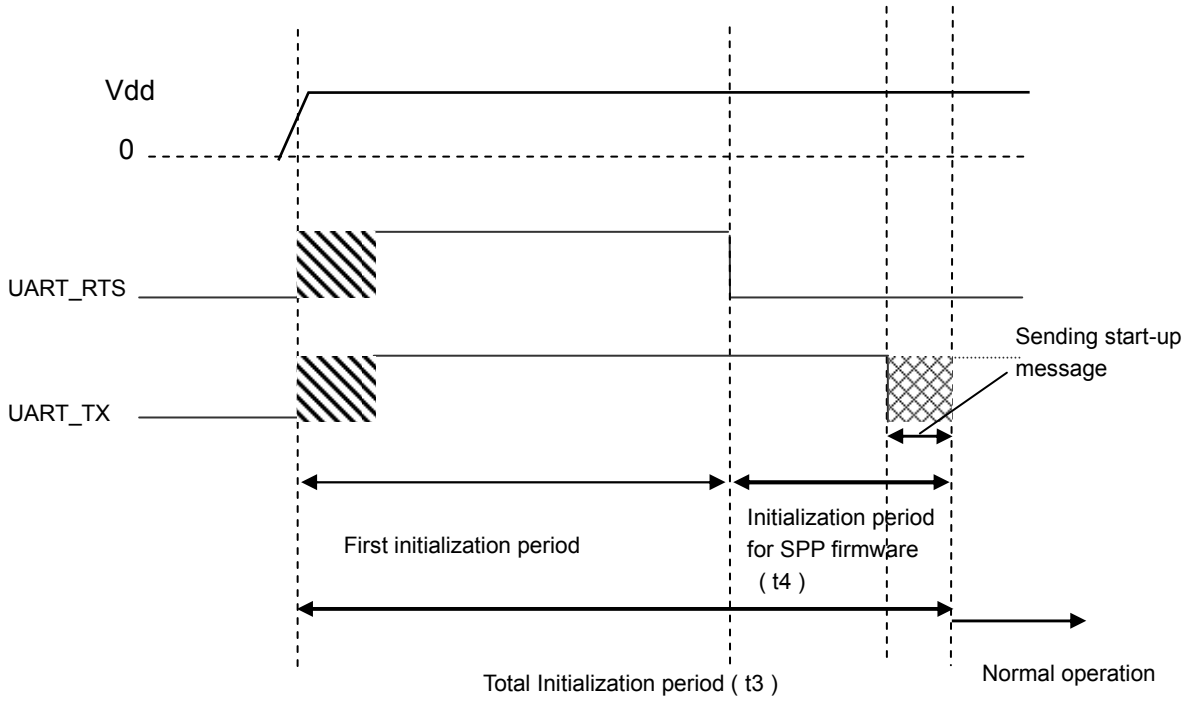


Figure 6-5-1: Boot sequence (When the write operation is not performed on the flash memory.)

	Item	Max
t3	First initialization period	800 ms
t4	Initialization period for SPP firmware	65 ms

*Note: Total initialization period (t3) doesn't include PS (Persistent Store) defragmentation time. PS defragmentation means the function which compactifies the PS (firmware configuration setting) area when there was insufficient free space in the internal flash memory. If there is no writing operation on PS area in the flash memory, this module doesn't perform PS defragmentation.

When the write operation is performed on the flash memory.

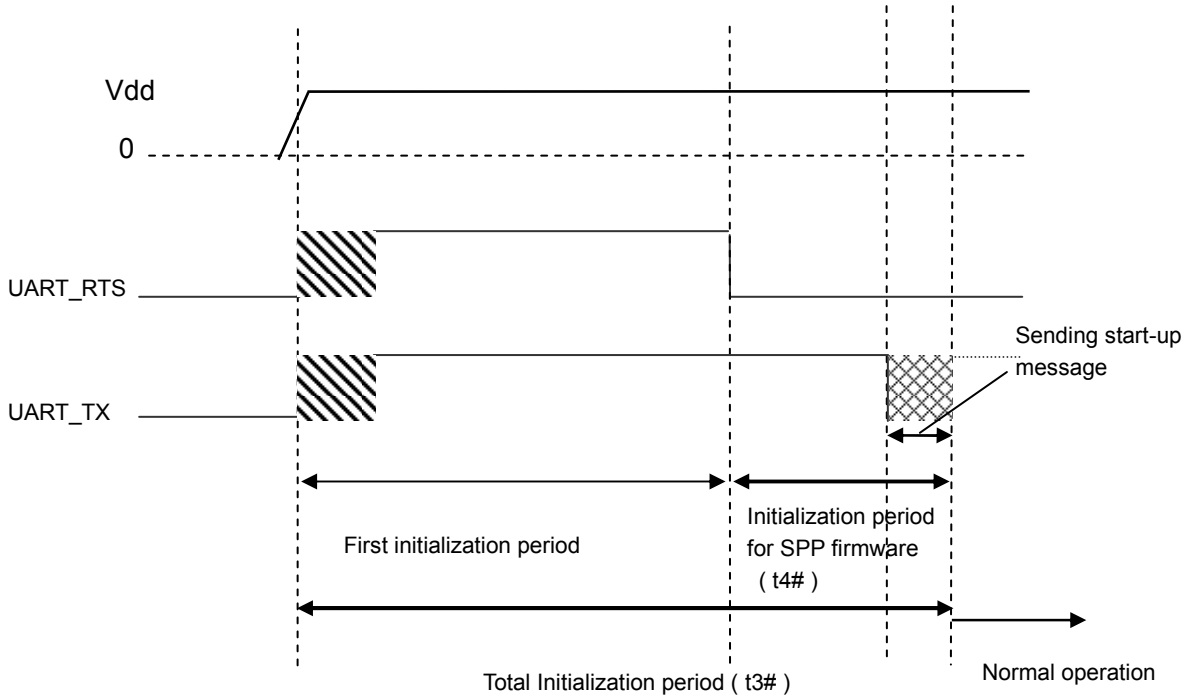


Figure 6-5-2: Boot sequence (When the write operation is performed on the flash memory.)

Item		Max
t3#	First initialization period	3.0s
t4#	Initialization period for SPP firmware	65ms

*Note: Total initialization period (t3#) includes PS (Persistent Store) defragmentation time. If there is writing operation on PS area in the flash memory, this module performs PS defragmentation.
Regarding the commands which are used for writing on PS area, please see "SPP firmware specification".

6-6. Reboot

Once the power supply has been turned off, wait until the voltage drops to zero (0V) before turning it on again.

Please note that the fall time of the power supply voltage varies according to the circuit configuration around this module.

6-7. SPI (Serial Peripheral Interface)

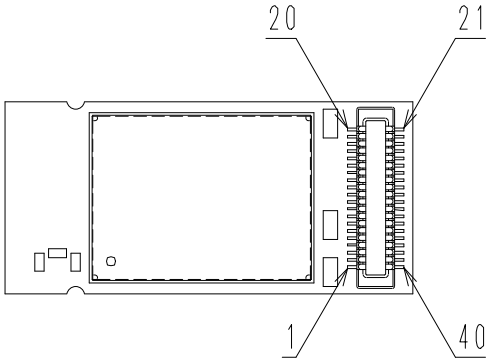
SPI (Serial Peripheral Interface) can be used for the firmware download to the internal flash memory. SPI is controlled by the proprietary utility software with using LPT (parallel) port on Windows PC.

The SPI_CS# pin must be held “High" level in normal operation to prevent the firmware from being erased.

7. SPP Interface Specification

Refer to FCL documentation “SPP firmware specification”.

8. Pin Description



<TOP View>

Pin Name	No.	I/O	Function	External Connection
GND	1	-	Ground	Ground
NC	2	-	Not connect	Leave unconnected
NC	3	-	Not connect	Leave unconnected
NC	4	-	Not connect	Leave unconnected
NC	5	-	Not connect	Leave unconnected
NC	6	-	Not connect	Leave unconnected
NC	7	-	Not connect	Leave unconnected
VDD	8	-	Power Supply	DC power supply
GND	9	-	Ground	Ground
UART_TX	10	O	UART Data output active high with weak internal pull-up	UART RxD
UART_RTS	11	O	UART Request To Send active low with weak internal pull-up	UART CTS
UART_RX	12	I	UART Data input active high with weak internal pull-down	UART TxD
UART_CTS	13	I	UART Clear To Send active low with weak internal pull-down	UART RTS
GND	14	-	Ground	Ground
NC	15	-	Not connect	Leave unconnected
NC	16	-	Not connect	Leave unconnected
NC	17	-	Not connect	Leave unconnected
NC	18	-	Not connect	Leave unconnected
NC	19	-	Not connect	Leave unconnected
NC	20	-	Not connect	Leave unconnected
PIO_11	21	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
PIO_10	22	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
GND	23	-	Ground	Ground
NC	24	-	Not connect	Leave unconnected
PIO_9	25	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
RESET#	26	I	Reset Input active low with weak internal pull-up	RESET (Input must be low for >5ms.)
SPI_CS#	27	I	SPI chip select active low with weak internal pull-up	SPI chip select or NC
SPI_MOSI	28	I	SPI data input with weak internal pull-down	SPI data output or NC
SPI_MISO	29	O	SPI data output with weak internal pull-down	SPI data input or NC
SPI_CLK	30	I	SPI clock with weak internal pull-down	SPI Clock output or NC

Pin Name	No.	I/O	Function	External Connection
PIO_8	31	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
PIO_4	32	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
PIO_3	33	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
PIO_2	34	I/O	Programmable Input/Output line with programmable strength internal pull-up/down	
GND	35	-	Ground	Ground
GND	36	-	Ground	Ground
GND	37	-	Ground	Ground
GND	38	-	Ground	Ground
GND	39	-	Ground	Ground
GND	40	-	Ground	Ground

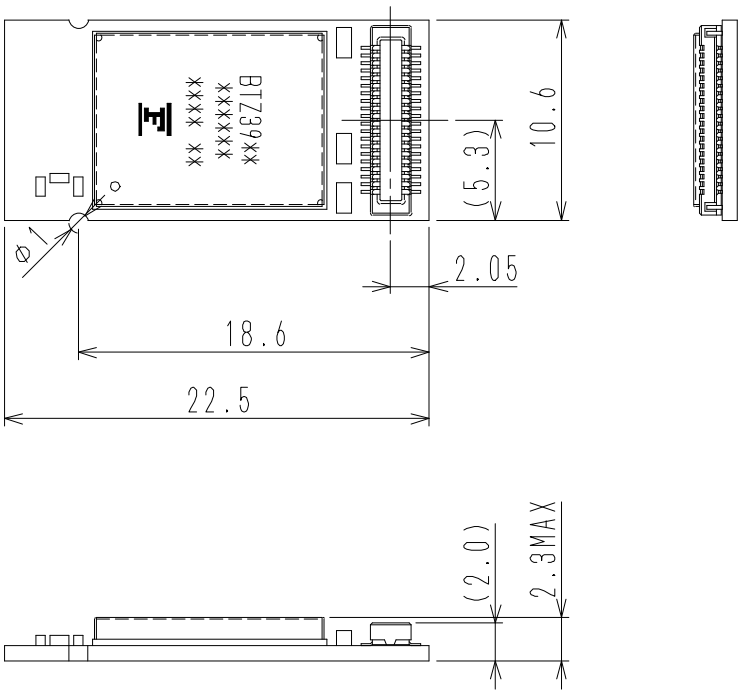
Note) The SPI_CS# pin must be held “High” level in normal operation.
Firmware might be deleted accidentally if the SPI_CS # pin is set to “Low” level.

8-1. Pin State on Reset

Pin Name	Pin No	State
UART_TX	10	Output tri-stated with weak pull-up
UART_RX	12	Input with weak pull-down
UART_CTS	13	Input with weak pull-down
UART_RTS	11	Output tri-stated with weak pull-up
SPI_CS#	27	Input with weak pull-up
SPI_MISO	29	Output tri-stated with weak pull-down
SPI_CLK	30	Input with weak pull-down
SPI_MOSI	28	Input with weak pull-down
RESET#	26	Input with weak pull-up
PIO_2	34	Input with weak pull-down
PIO_3	33	Input with weak pull-down
PIO_4	32	Input with weak pull-down
PIO_8	31	Input with weak pull-down
PIO_9	25	Input with weak pull-down
PIO_10	22	Input with weak pull-down
PIO_11	21	Input with weak pull-down

9. Mechanical Characteristics

9-1. Appearance and Dimensions

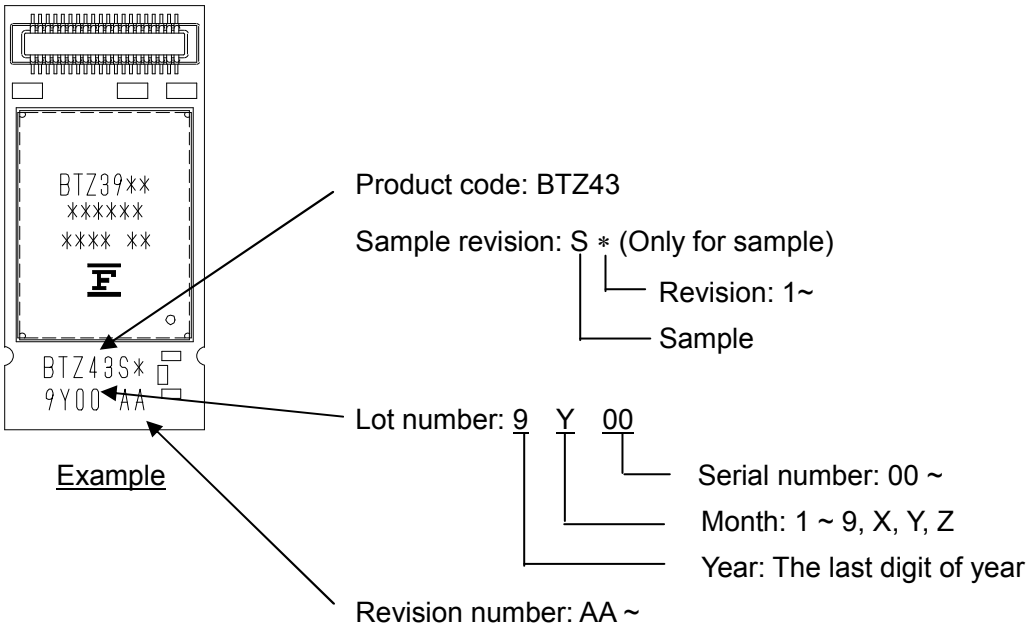


Connector: Molex 55909-0474

*The connector mounted on the host equipment is Molex 500913-0402.

Unit: mm

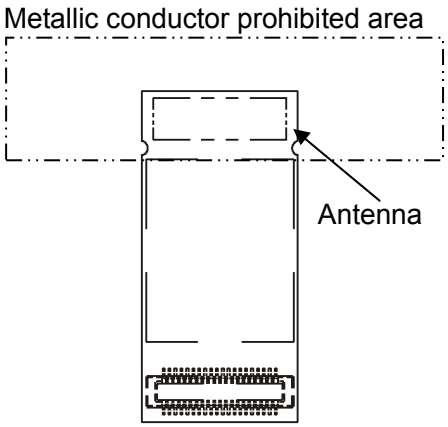
9-2. Marking (TBD)



9-3. Notes for antenna layout

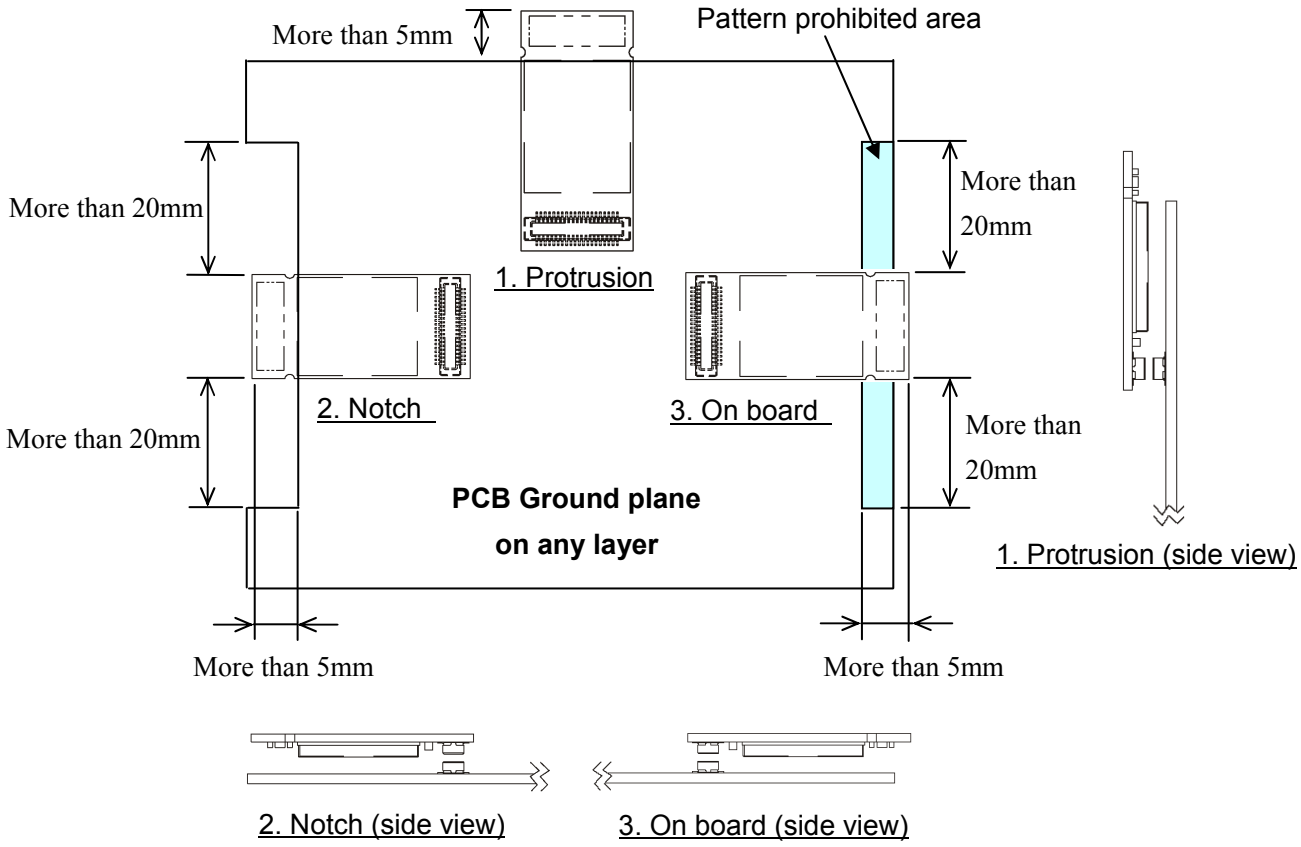
You should avoid to put metals or conductive materials close to the antenna.

It interferes with the radio emission from the antenna, and the communication distance might be decreased remarkably.



9-4. Module layout guideline

The module layout on your PCB should be designed according to the following guidelines.

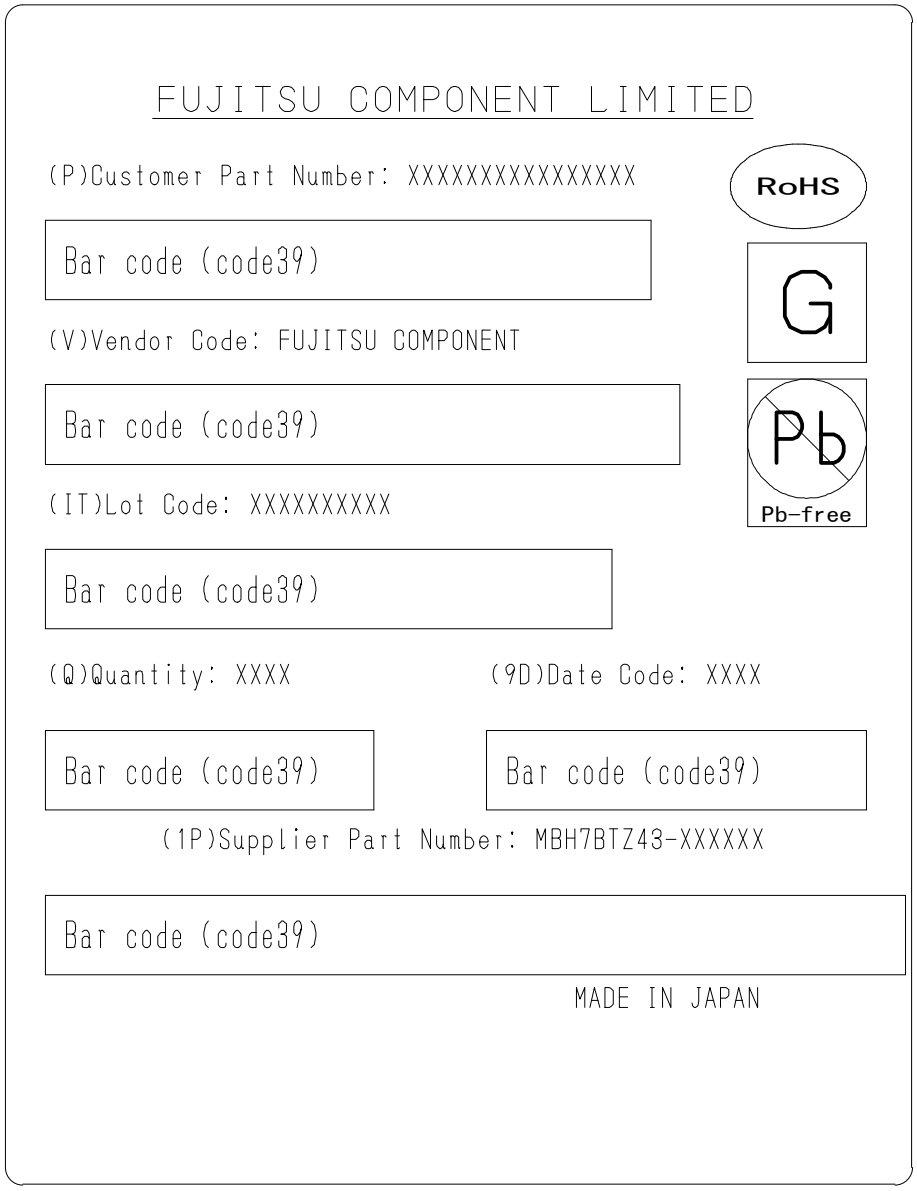


10. Storage Conditions

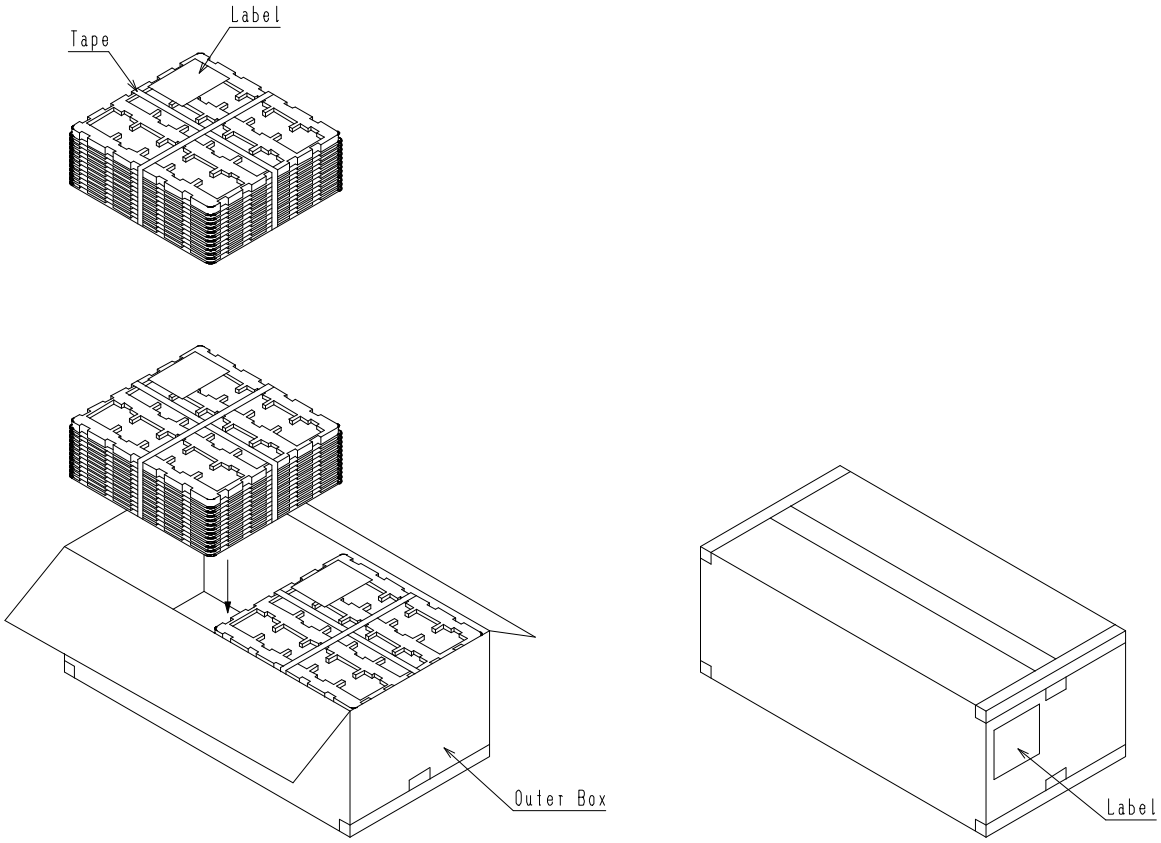
It is recommended that the moisture proof bag is placed in a storage cabinet at 30°C and < 60% RH, and be used within 6 months from the delivery date.

11. Shipment Packing Specification

11-1. Bar code label



11-2. Package (TBD)



12. Revision History

Revision	Marking Rev (Product Marking)	Contents change	Date
Rev. 1.0	AA	Created first edition.	FEB 10 2010
Rev. 0.11	AA	Section 6-6 was added.	MAR 10 2010