2.5 V to 5.5 V, 500 µA, Quad Voltage Output 12-Bit DAC in 10-Lead Package

Enhanced Product

AD5324-EP

FEATURES

Enhanced product features
- **Supports defense and aerospace applications (AQEC)**
- **Military temperature range (−55°C to +125°C)**
- **Controlled manufacturing baseline**
- **One assembly/test site**
- **One fabrication site**
- **Enhanced product change notification**
- **Qualification data available on request**

Four buffered 12-Bit DACs in 10-lead MSOP
- **S Version: ±10 LSB INL**

Low power operation: 500 µA at 3 V, 600 µA at 5 V
2.5 V to 5.5 V power supply
Guaranteed monotonic by design over all codes
Power-down to 80 nA at 3 V, 200 nA at 5 V
Double-buffered input logic
Output range: 0 V to V_{REF}
Power-on reset to 0 V
Simultaneous update of outputs ($\overline{LDAC}$ function)
On-chip, rail-to-rail output buffer amplifiers
Temperature range −55°C to +125°C

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators
Industrial process control

GENERAL DESCRIPTION

The AD5324-EP[1] is a quad 12-bit buffered voltage output digital-to-analog converter (DAC) in a 10-lead MSOP package that operates from a single 2.5 V to 5.5 V supply, consuming 500 µA at 3 V. The on-chip output amplifiers allows rail-to-rail output swing to be achieved with a slew rate of 0.7 V/µs. A 3-wire serial interface is used; it operates at clock rates up to 30 MHz and is compatible with standard serial peripheral interface (SPI), QSPI™, MICROWIRE™, and DSP interface standards.

The references for the four DACs are derived from one reference pin. The outputs of all DACs can be updated simultaneously using the software $\overline{LDAC}$ function. The part incorporates a power-on reset circuit and ensures that the DAC outputs power up to 0 V and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to 200 nA at 5 V (80 nA at 3 V).

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 3 mW at 5 V, and 1.5 mW at 3 V, reducing to 1 µW in power-down mode.

Full details about this enhanced product are available in the AD5324 data sheet, which must be consulted in conjunction with this data sheet.

[1] Protected by U.S. Patent No. 5,969,657.

FUNCTIONAL BLOCK DIAGRAM

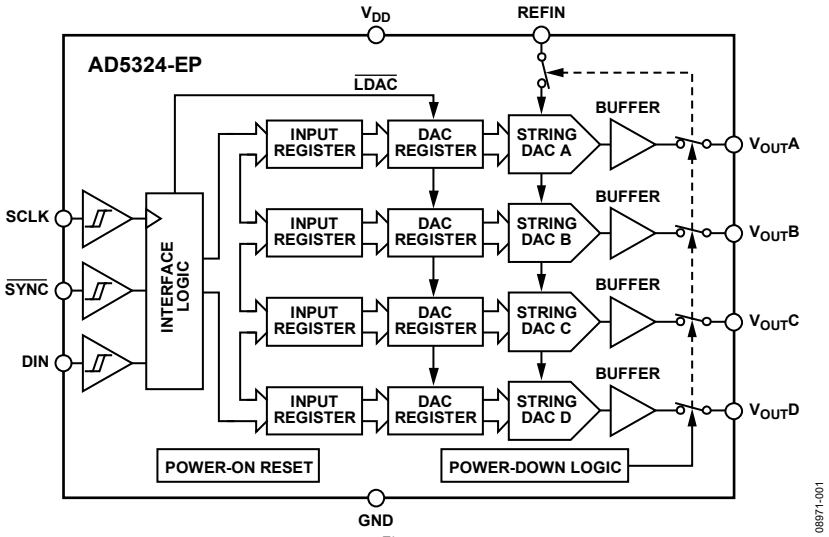

Figure 1.

Rev. A Document Feedback

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Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/2019—Rev. 0 to Rev. A

Changes to Patent Information 1
Changes to Offset Error Parameter, Table 1 and Gain Error Parameter, Table 1 3
Changes to Peak Temperature Parameter, Table 4 6
Updated Outline Dimensions 11

4/2010—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	S Version				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[1]					
Resolution		12		Bits	
Relative Accuracy		±2	±10	LSB	
Differential Nonlinearity[2]		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	See Figure 6 and Figure 8
Gain Error		±0.15	±1	% of FSR	See Figure 6 and Figure 8
Lower Dead Band		20	60	mV	Lower dead band exists only if offset error is negative
Offset Error Drift[3]		−12		ppm of FSR/°C	
Gain Error Drift[3]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[3]		−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[3]		200		µV	R_L = 2 kΩ to GND or V_{DD}
DAC REFERENCE INPUTS[3]					
V_{REF} Input Range	0.25		V_{DD}	V	
V_{REF} Input Impedance	37	45		kΩ	Normal operation
		>10		MΩ	Power-down mode
Reference Feedthrough		−90		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[3]					
Minimum Output Voltage[4]		0.001		V	Measurement of the minimum and maximum
Maximum Output Voltage[4]		V_{DD} − 0.001			V drive capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode V_{DD} = 5 V
		5		µs	Coming out of power-down mode V_{DD} = 3 V
LOGIC INPUTS[3]					
Input Current			±1	µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = 5 V ± 10%
			0.6	V	V_{DD} = 3 V ± 10%
			0.5	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = 5 V ± 10%
	2.1			V	V_{DD} = 3 V ± 10%
	2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)[5]					
V_{DD} = 4.5 V to 5.5 V		600	900	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.5 V to 3.6 V		500	700	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (Power-Down Mode)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.5 V to 3.6 V		0.08	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] DC specifications tested with the outputs unloaded.
[2] Linearity is tested using a reduced code range: Code 115 to Code 3981.
[3] Guaranteed by design and characterization, not production tested.
[4] For the amplifier output to reach the minimum voltage, offset error must be negative. For the amplifier output to reach the maximum voltage, $V_{REF} = V_{DD}$ and offset plus gain error must be positive.
[5] I_{DD} specification is valid for all DAC codes; interface inactive; all DACs active; load currents excluded.

AC CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	S Version[2]				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
		8	10	µs	¼ scale to ¾ scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major Code Transition Glitch Energy		12		nV-sec	1 LSB change around major carry
Digital Feedthrough		1		nV-sec	
Digital Crosstalk		1		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p; frequency = 10 kHz

[1] Guaranteed by design and characterization, not production tested.
[2] Temperature range (S Version): –55°C to +125°C; typical at +25°C.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

	Limit at T_{MIN}, T_{MAX}			
Parameter[1, 2, 3]	**V_{DD} = 2.5 V to 3.6 V**	**V_{DD} = 3.6 V to 5.5 V**	**Unit**	**Conditions/Comments**
t_1	40	33	ns min	SCLK cycle time
t_2	16	13	ns min	SCLK high time
t_3	16	13	ns min	SCLK low time
t_4	16	13	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	80	33	ns min	Minimum $\overline{SYNC}$ high time

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with tr = tf = 5 ns (10% to 90 % of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3] See Figure 2.

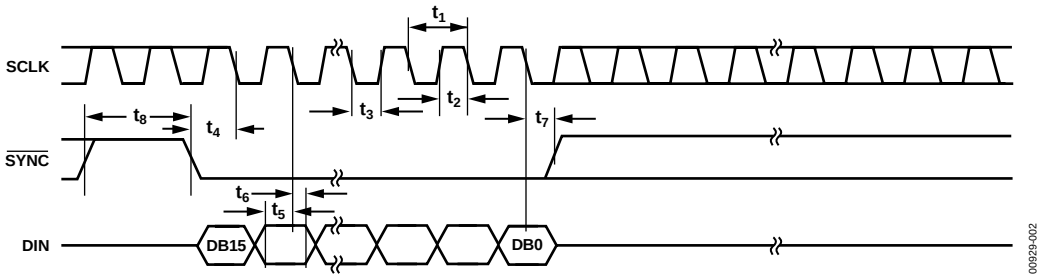


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter[1]	Rating
V_{DD} to GND	–0.3 V to +7 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT}A through V_{OUT}D to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (EP Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	150°C
10-Lead MSOP	
Power Dissipation	(T_J max – T_A)/ θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

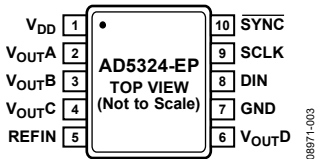


Figure 3. MSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. This part can be operated from 2.5 V to 5.5 V and the supply can be decoupled to GND.
2	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
4	$V_{OUT}C$	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	REFIN	Reference Input Pin for All Four DACs. It has an input range from 0.25 V to V_{DD}.
6	$V_{OUT}D$	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
7	GND	Ground Reference Point for All Circuitry on the Part.
8	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The DIN input buffer is powered down after each write cycle.
9	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30 MHz. The SCLK input buffer is powered down after each write cycle.
10	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following 16 clocks. If $\overline{\text{SYNC}}$ is taken high before the 16th falling edge of SCLK, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.

TYPICAL PERFORMANCE CHARACTERISTICS

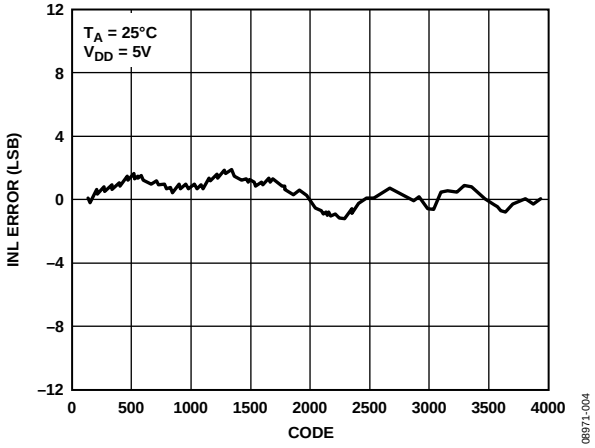


Figure 4. Typical Integral Nonlinearity (INL) Plot

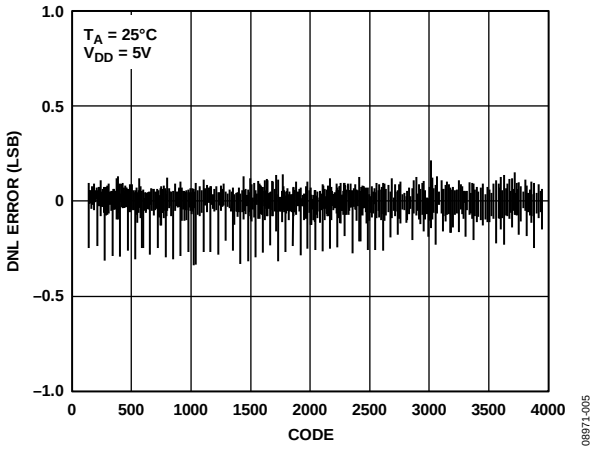


Figure 5. Typical Differential Nonlinearity (DNL) Plot

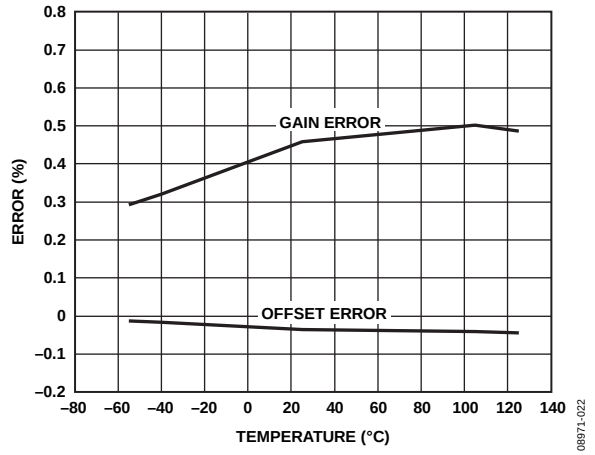


Figure 6. Offset Error and Gain Error vs. Temperature

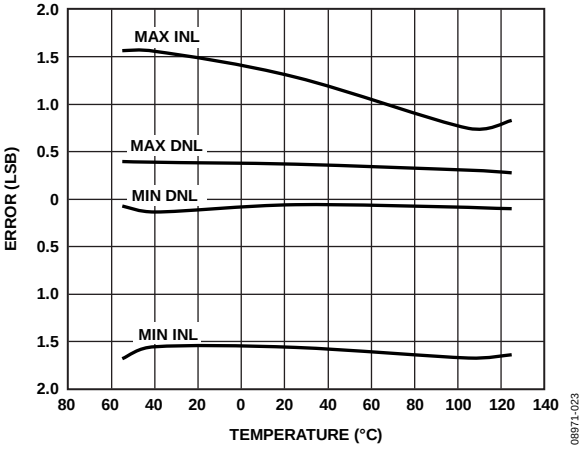


Figure 7. INL and DNL Error vs. Temperature

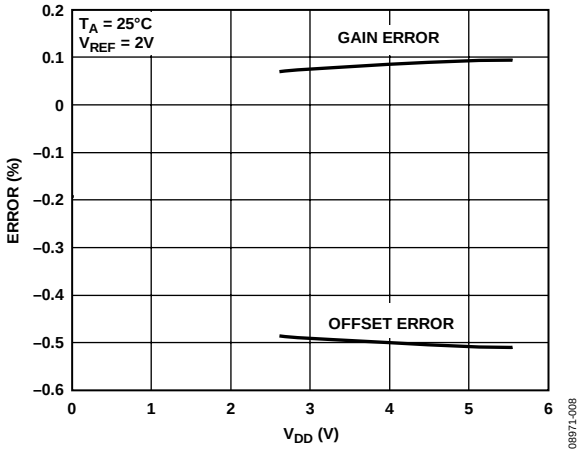


Figure 8. Offset Error and Gain Error vs. V_{DD}

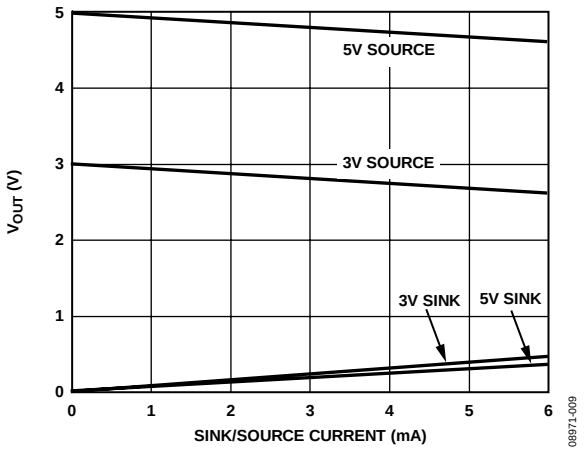


Figure 9. V_{OUT} Source and Sink Current Capability

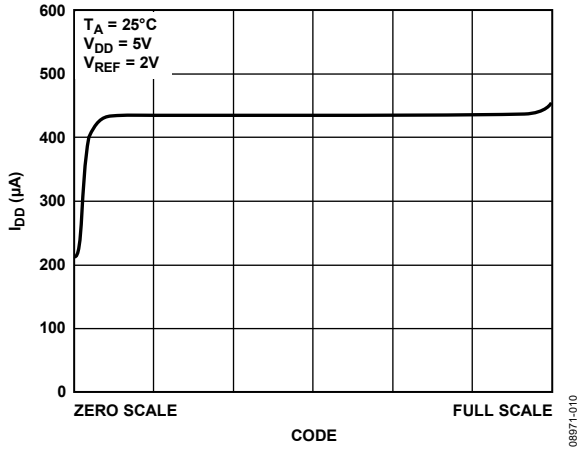


Figure 10. Supply Current vs. DAC Code

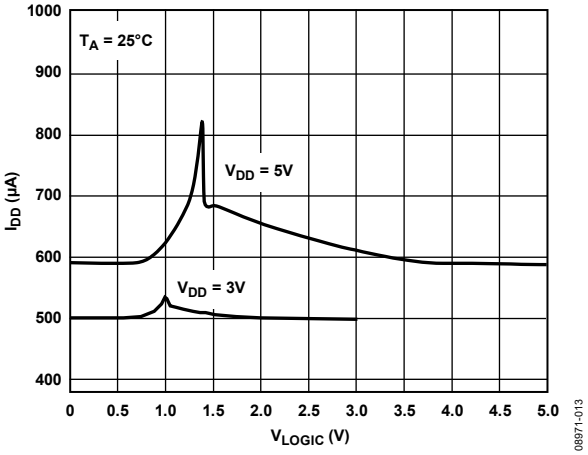


Figure 13. Supply Current vs. Logic Input Voltage

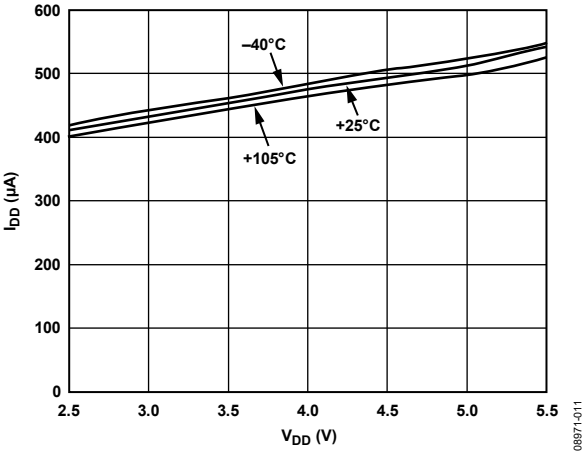


Figure 11. Supply Current vs. Supply Voltage

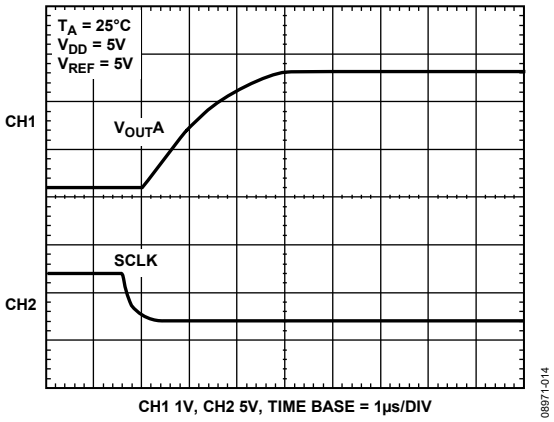


Figure 14. Half-Scale Settling (¼ to ¾ Scale Code Change)

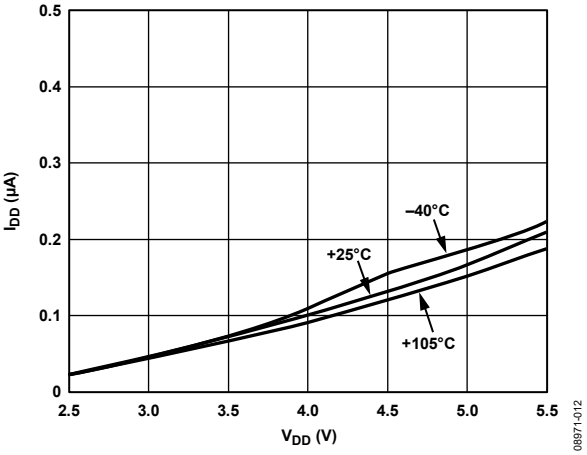


Figure 12. Power-Down Current vs. Supply Voltage

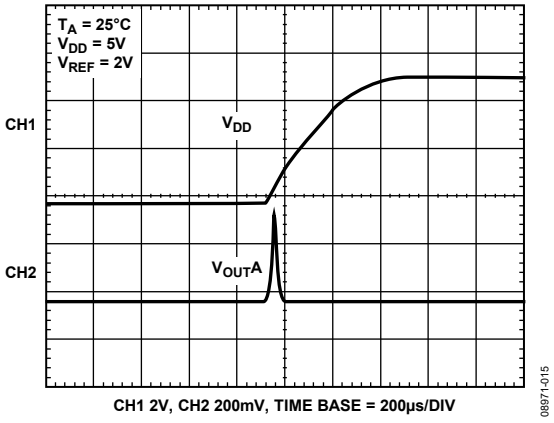


Figure 15. Power-On Reset to 0 V

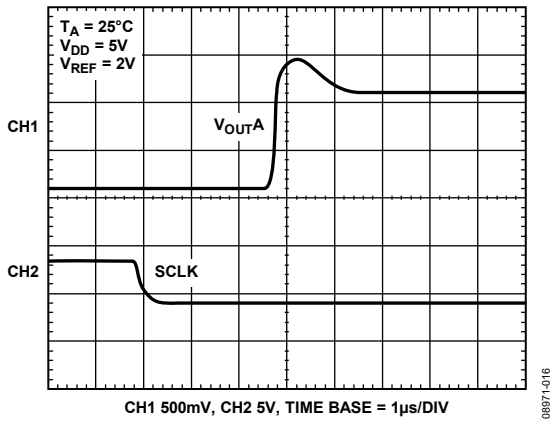


Figure 16. Exiting Power-Down to Midscale

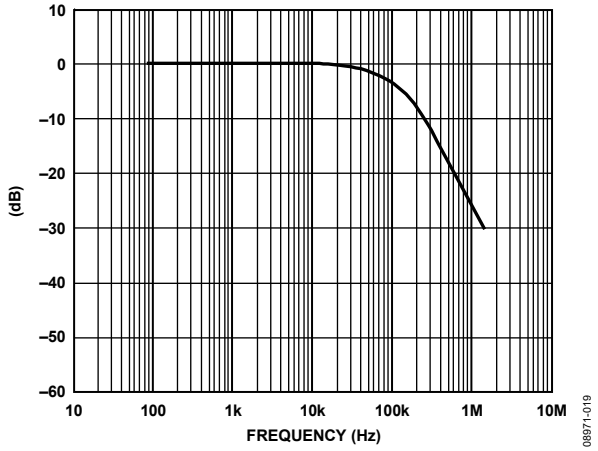


Figure 19. Multiplying Bandwidth (Small-Signal Frequency Response)

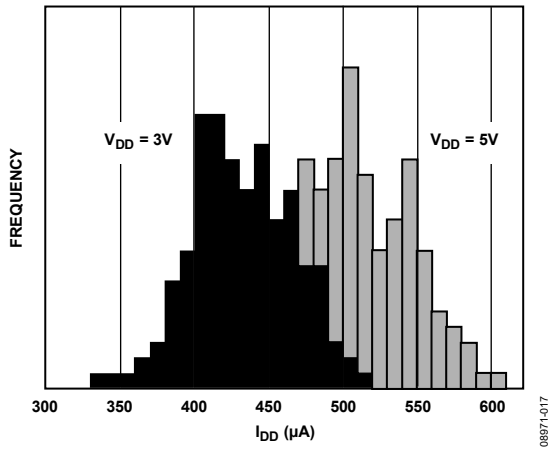


Figure 17. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

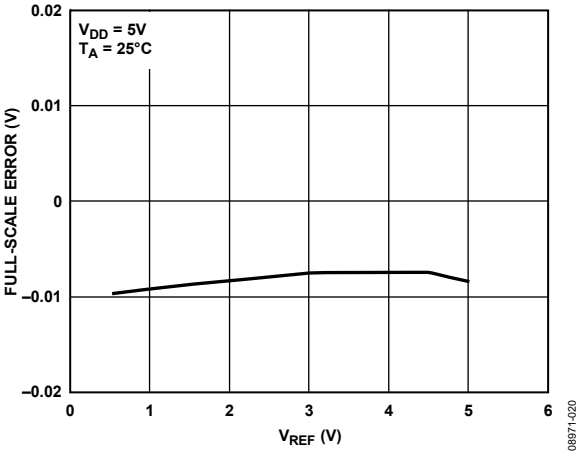


Figure 20. Full-Scale Error vs. V_{REF}

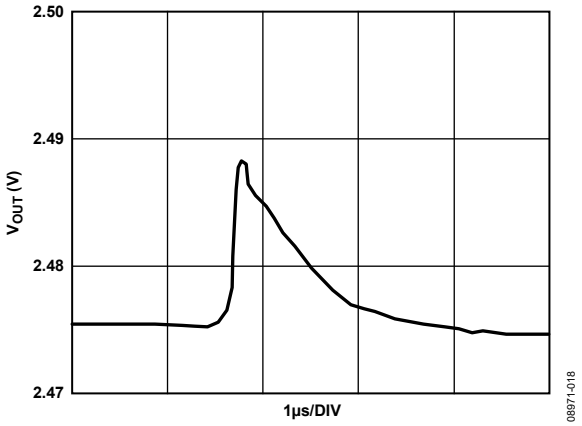


Figure 18. Major-Code Transition Glitch Energy

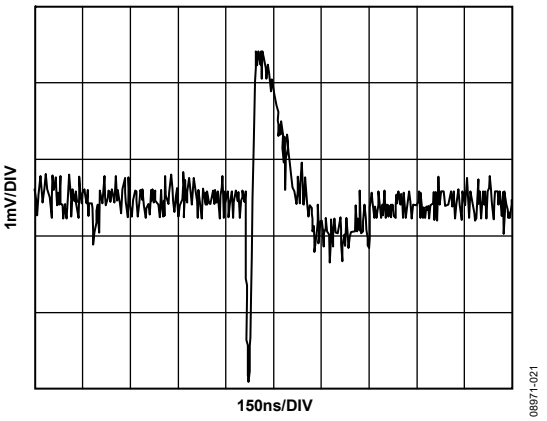
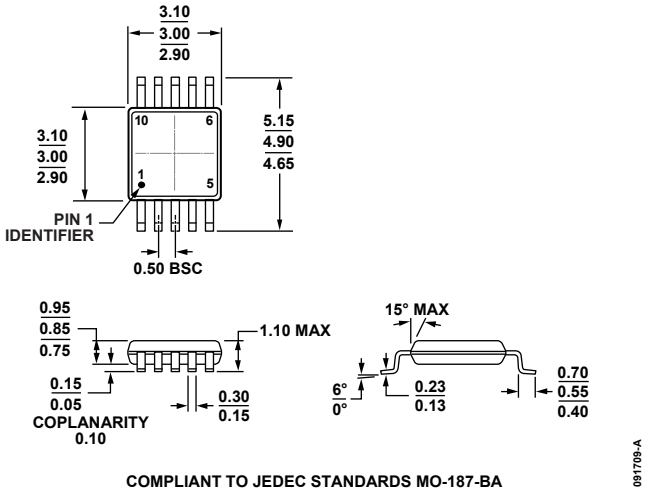


Figure 21. DAC-to-DAC Crosstalk

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 22. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD5324SRMZ-EP-RL7	−55°C to +125°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	DFT

[1] Z = RoHS Compliant Part.

D08971-0-6/19(A)