# 2 OUTPUT PCIE GEN1/2 SYNTHESIZER

IDT5V41065

## Recommended Applications

2 Output synthesizer for PCIe Gen1/2 and Ethernet

## General Description

The IDT5V41065 is a PCIe Gen2 compliant spread spectrum capable clock generator. The device has 2 differential HCSL outputs and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). The spread amount and output frequency are selectable via select pins. The IDT5V41065 can also supply 25 MHz, 125 MHz and 200 MHz outputs for applications such as Ethernet.

## Output Features

- 2 - 0.7V current mode differential HCSL output pairs

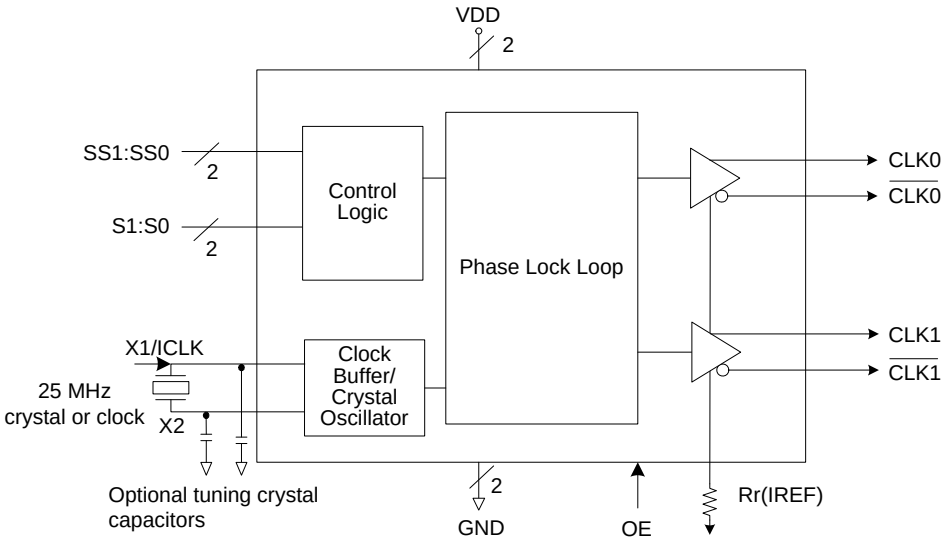
## Features/Benefits

- 16-pin TSSOP and QFN packages; small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- 25 MHz, 125 MHz and 200 MHz output frequencies; TSSOP only
- 100MHz and 200MHz output frequencies; VFQFPN package
- OE control pin; greater system power management
- Spread% and frequency pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications
- **For PCIe Gen3 applications, see the 5V41235**

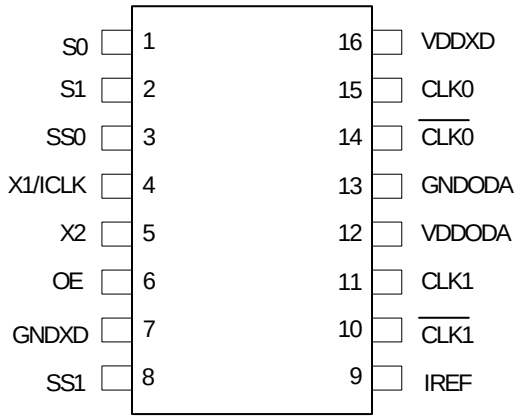
## Key Specifications

- Cycle-to-cycle jitter < 100 ps
- Output-to-output skew < 50 ps
- PCIe Gen2 phase jitter < 3.0ps RMS

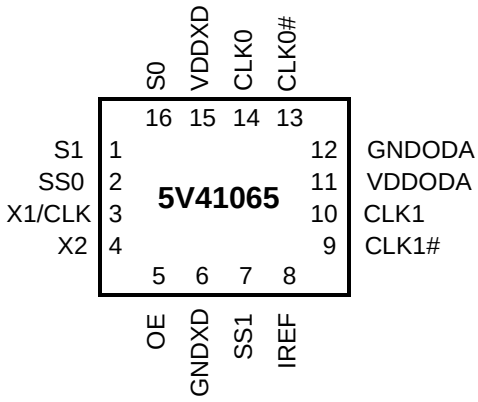
## Block Diagram



## Pin Assignment




16-pin (173 mil) TSSOP




16-pin VFQFPN

### Output Select Table 1 (MHz)–TSSOP only

| S1 | S0 | CLK(1:0), $\overline{\text{CLK(1:0)}}$ |
|---|---|---|
| 0 | 0 | 25M |
| 0 | 1 | 100M |
| 1 | 0 | 125M |
| 1 | 1 | 200M |

### Spread Selection Table 2–TSSOP only

| SS1 | SS0 | Spread% |
|---|---|---|
| 0 | 0 | No Spread |
| 0 | 1 | Down -0.5 |
| 1 | 0 | Down -0.75 |
| 1 | 1 | No Spread |

### Output/Spread Select Table 3 - VFQFPN Only

| S1 | S0 | SS1 | SS0 | Output | Spread% |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 100MHz | -0.5 |
| 0 | 0 | 0 | 1 | 200MHz | -0.5 |
| 0 | 0 | 1 | 0 | 100MHz | No spread |
| 0 | 0 | 1 | 1 | Reserved | |
| 0 | 1 | 0 | 0 | 100MHz | -1 |
| 0 | 1 | 0 | 1 | 200MHz | -1 |
| 0 | 1 | 1 | 0 | Reserved | |
| 0 | 1 | 1 | 1 | Reserved | |
| 1 | 0 | 0 | 0 | 100MHz | -1.5 |
| 1 | 0 | 0 | 1 | 200MHz | -1.5 |
| 1 | 0 | 1 | 0 | Reserved | |
| 1 | 0 | 1 | 1 | Reserved | |
| 1 | 1 | 0 | 0 | Reserved | |
| 1 | 1 | 0 | 1 | 200MHz | No spread |
| 1 | 1 | 1 | 0 | Reserved | |
| 1 | 1 | 1 | 1 | Reserved | |

## Pin Descriptions

| VFQFPN Pin Number | TSSOP Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|---|
| 16 | 1 | S0 | Input | Select pin 0. See Table1. Internal pull-up resistor. |
| 1 | 2 | S1 | Input | Select pin 1. See Table 1. Internal pull-up resistor. |
| 2 | 3 | SS0 | Input | Spread Select pin 0. See Table 2. Internal pull-up resistor. |
| 3 | 4 | X1/ICLK | Input | Crystal or clock input. Connect to a 25 MHz crystal or single ended clock. |
| 4 | 5 | X2 | Output | Crystal connection. Leave unconnected for clock input. |
| 5 | 6 | OE | Input | Output enable. Tri-states outputs and device is not shut down. Internal pull-up resistor. |
| 6 | 7 | GNDXD | Power | Connect to ground. |
| 7 | 8 | SS1 | Input | Spread Select pin 1. See Table 2. Internal pull-up resistor. |
| 8 | 9 | IREF | Output | Precision resistor attached to this pin is connected to the internal current reference. |
| 9 | 10 | CLK1 | Output | HCSL complementary clock output 1. |
| 10 | 11 | CLK1 | Output | HCSL true clock output 1. |
| 11 | 12 | VDDODA | Power | Connect to voltage supply +3.3 V for output driver and analog circuits |
| 12 | 13 | GNDODA | Power | Connect to ground. |
| 13 | 14 | CLK0 | Output | HCSL complementary clock output 0. |
| 14 | 15 | CLK0 | Output | HCSL true clock output 0. |
| 15 | 16 | VDDXD | Power | Connect to voltage supply +3.3 V for crystal oscillator and digital circuit. |

# Applications Information

## External Components

A minimum number of external components are required for proper operation.

## Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

## Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the IDT5V41065 to meet PCI Express specifications.

## Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

$C_L$= Crystal's load capacitance in pF

Crystal Capacitors (pF) = ($C_L$- 8) * 2

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. (16-8)*2=16.

Current Source (Iref) Reference Resistor - $R_R$

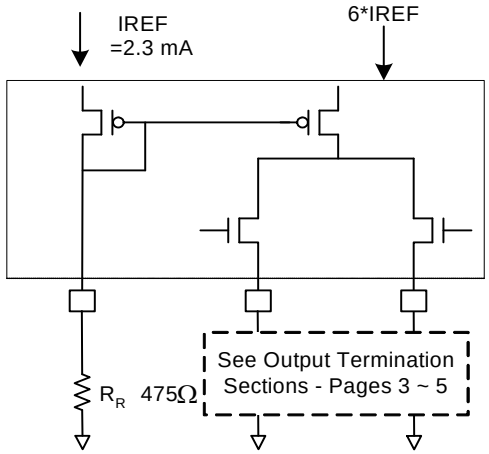
If board target trace impedance (Z) is 50Ω, then $R_R$ = 475Ω (1%), providing IREF of 2.32 mA. The output current ($I_{OH}$) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41065 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41065 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

# Output Structures




## General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41065.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

# Layout Guidelines

| SRC Reference Clock | | | |
|---|---|---|---|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

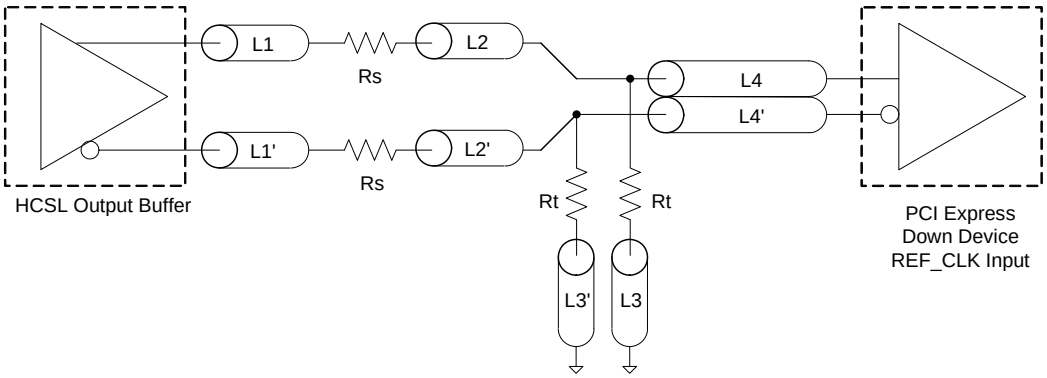
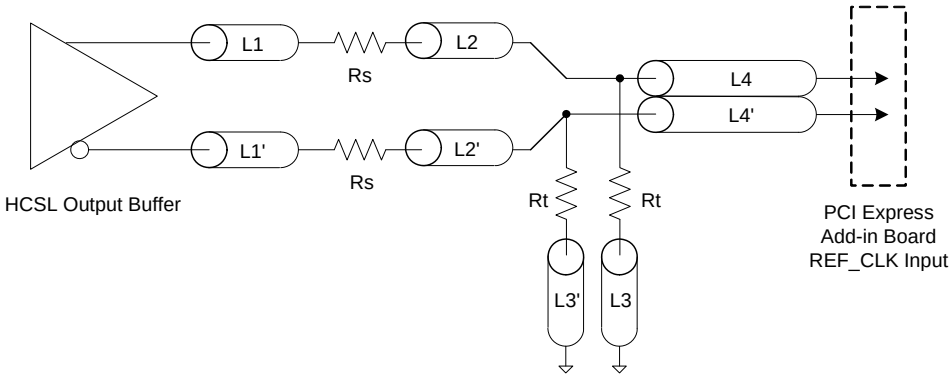


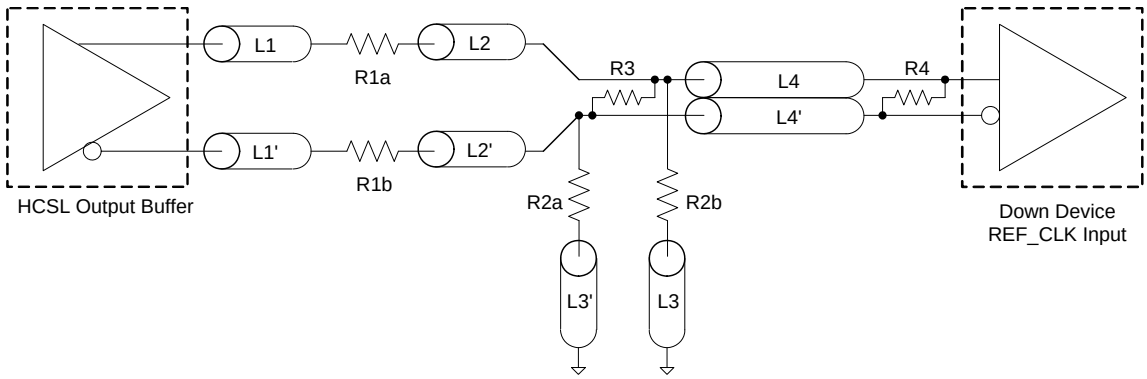

Figure 2: PCI Express Connector Routing



| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

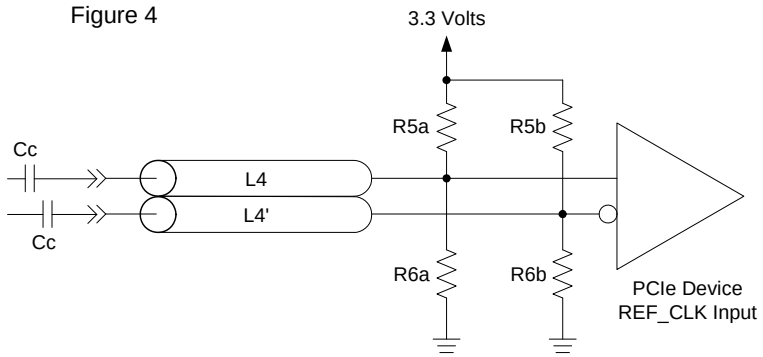
R1a = R1b = R1
R2a = R2b = R2

Figure 3

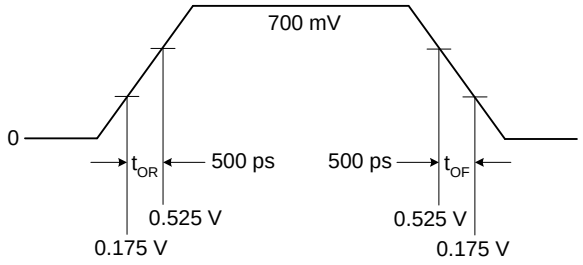



| Cable Connected AC Coupled Application (figure 4) | | |
|---|---|---|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 µF | |
| Vcm | 0.350 volts | |

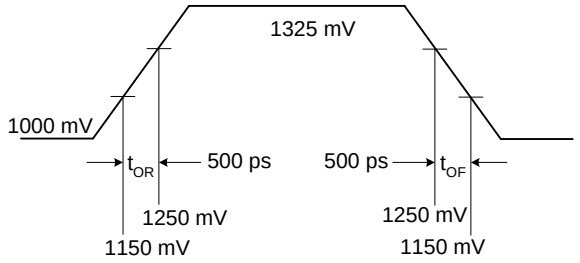
Figure 4



## Typical PCI-Express (HCSL) Waveform




## Typical LVDS Waveform



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41065. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDDXD, VDDODA | 4.6 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70°C |
| Ambient Operating Temperature (industrial) | -40 to +85°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |
| ESD Protection (Input) | 2000 V min. (HBM) |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | V | | 3.135 | 3.3 | 3.465 | V |
| Input High Voltage[1] | $V_{IH}$ | S0, S1, OE, ICLK, SS0, SS1 | 2.2 | | VDD +0.3 | V |
| Input Low Voltage[1] | $V_{IL}$ | S0, S1, OE, ICLK, SS0, SS1 | VSS-0.3 | | 0.8 | V |
| Input Leakage Current[2] | $I_{IL}$ | 0 < Vin < VDD | -5 | | 5 | µA |
| Operating Supply Current @100 MHz | $I_{DD}$ | $R_S$=33Ω, $R_P$=50Ω, $C_L$=2 pF | | 63 | 85 | mA |
| | $I_{DDOE}$ | OE =Low | | 42 | 50 | mA |
| Input Capacitance | $C_{IN}$ | Input pin capacitance | | | 7 | pF |
| Output Capacitance | $C_{OUT}$ | Output pin capacitance | | | 6 | pF |
| X1, X2 Capacitance | $C_{INX}$ | | | | 5 | pF |
| Pin Inductance | $L_{PIN}$ | | | | 5 | nH |
| Output Impedance | $Z_O$ | CLK outputs | 3.0 | | | kΩ |
| Pull-up Resistor | $R_{PU}$ | S0, S1, OE, SS0, SS1 | | 100 | | kΩ |

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

## AC Electrical Characteristics - CLK0/CLK1, $\overline{\text{CLK0/CLK1}}$

Unless stated otherwise, **VDD=3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | | | | 25 | | MHz |
| Output Frequency | | HCSL termination | 25 | | 200 | MHz |
| | | LVDS termination | 25 | | 100 | MHz |
| Output High Voltage[1,2] | $V_{OH}$ | HCSL | | | 850 | mV |
| Output Low Voltage[1,2] | $V_{OL}$ | HCSL | -150 | | | mV |
| Crossing Point Voltage[1,2] | | Absolute | 250 | | 550 | mV |
| Crossing Point Voltage[1,2,4] | | Variation over all edges | | | 140 | mV |
| Jitter, Cycle-to-Cycle[1,3] | | | | | 100 | ps |
| Frequency Synthesis Error | | All outputs | | 0 | | ppm |
| Modulation Frequency | | Spread spectrum | 30 | 32.9 | 33 | kHz |
| Rise Time[1,2] | $t_{OR}$ | From 0.175 V to 0.525 V | 175 | | 700 | ps |
| Fall Time[1,2] | $t_{OF}$ | From 0.525 V to 0.175 V | 175 | | 700 | ps |
| Rise/Fall Time Variation[1,2] | | | | | 125 | ps |
| Output to Output Skew | | | | | 50 | ps |
| Duty Cycle[1,3] | | | 45 | | 55 | % |
| Output Enable Time[5] | | All outputs | | 50 | 100 | ns |
| Output Disable Time[5] | | All outputs | | 50 | 100 | ns |
| Stabilization Time | $t_{STABLE}$ | From power-up VDD=3.3 V | | | 1.8 | ms |
| Spread Spectrum Transition Time | $t_{SPREAD}$ | Stabilization time after spread spectrum changes | 7 | | 30 | ms |

Note 1: Test setup is $R_S$=33Ω, $R_P$=50Ω with $C_L$=2 pF, Rr = 475Ω (1%).

Note 2: Measurement taken from a single-ended waveform.

Note 3: Measurement taken from a differential waveform.

Note 4: Measured at the crossing point where instantaneous voltages of both CLK and $\overline{\text{CLK}}$ are equal.

Note 5: CLK pins are tri-stated when OE is low asserted. CLK is driven differential when OE is high.

## Electrical Characteristics - Differential Phase Jitter

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Jitter, Phase | $t_{jphasePLL}$ | PCIe Gen1 | | 32 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphaseLO}$ | PCIe Gen2, 10 kHz < f < 1.5 MHz | | 0.8 | 3 | ps (RMS) | 1,2,3 |
| | $t_{jphaseHIGH}$ | PCIe Gen2, 1.5 MHz < f < Nyquist (50 MHz) | | 2.3 | 3.1 | ps (RMS) | 1,2,3 |

Note 1. Guaranteed by design and characterization, not 100% tested in production.

Note 2. See http://www.pcisig.com for complete specs.

Note 3: Applies to 100MHz, spread off and 0.5% down spread only.

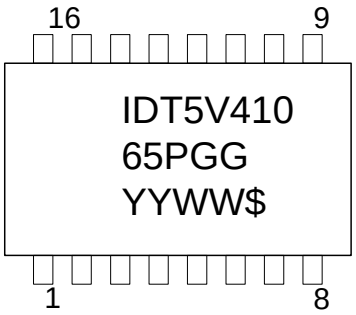
## Thermal Characteristics (16TSSOP)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 78 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 70 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 37 | | °C/W |

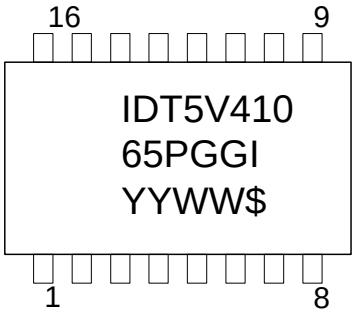
## Thermal Characteristics(16VFQFPN)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 63.2 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 55.9 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 51.4 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 65.8 | | °C/W |

## Marking Diagram (5V41065PGG)



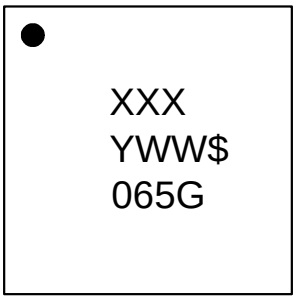

## Marking Diagram (5V41065PGGI)



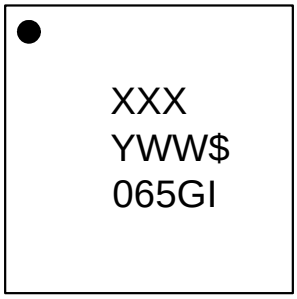

Notes:

1. Line 1 and 2: IDT part number.
2. Line 3: YYWW – Date code; $ – Assembly location.
3. “G” after the two-letter package code designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

## Marking Diagram (5V41065NLGI)




## Marking Diagram (5V41065NLGI)

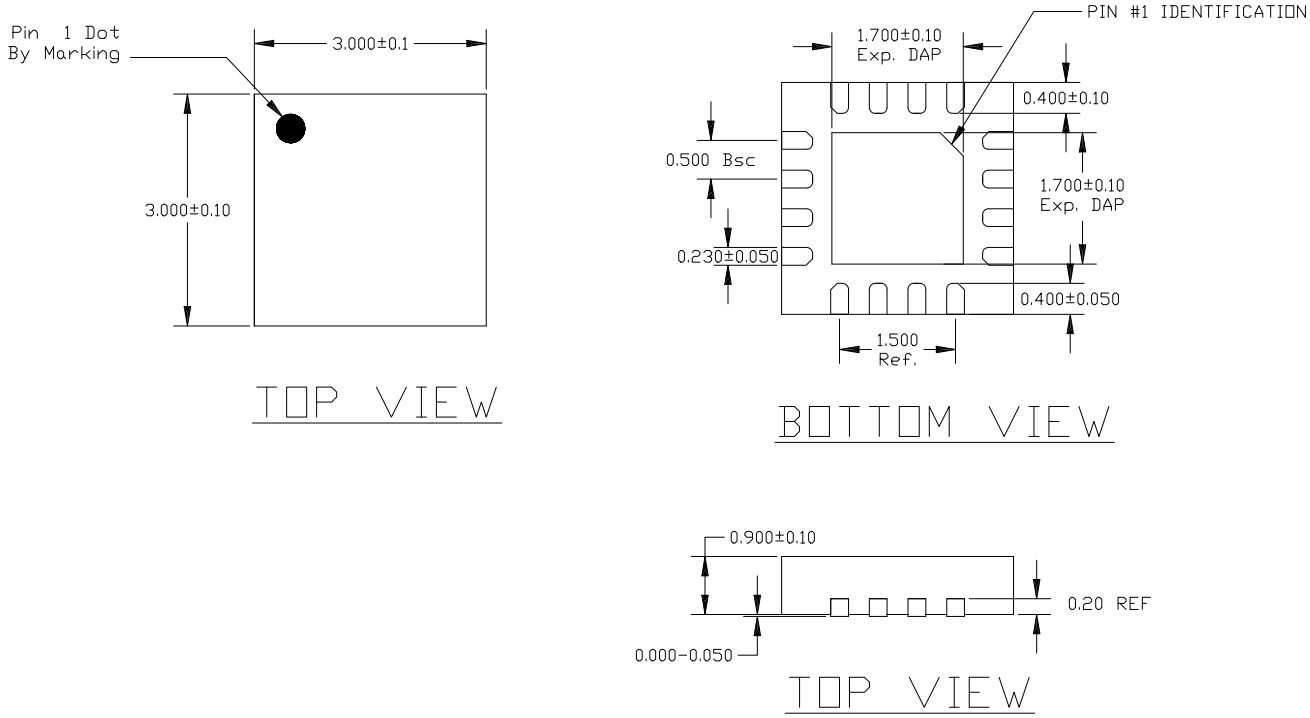



Notes:

1. Line 1: Lot number.
2. Line 2: YWW – Date code; $ – Assembly location.
3. “G” designates RoHS compliant package.
4. “I” at the end of part number indicates industrial temperature range.

# Package Outline and Package Dimensions (16-pin QFN)

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RC |
| 01 | COMBINE POD & LAND PATTERN | 9/17/13 | KS |

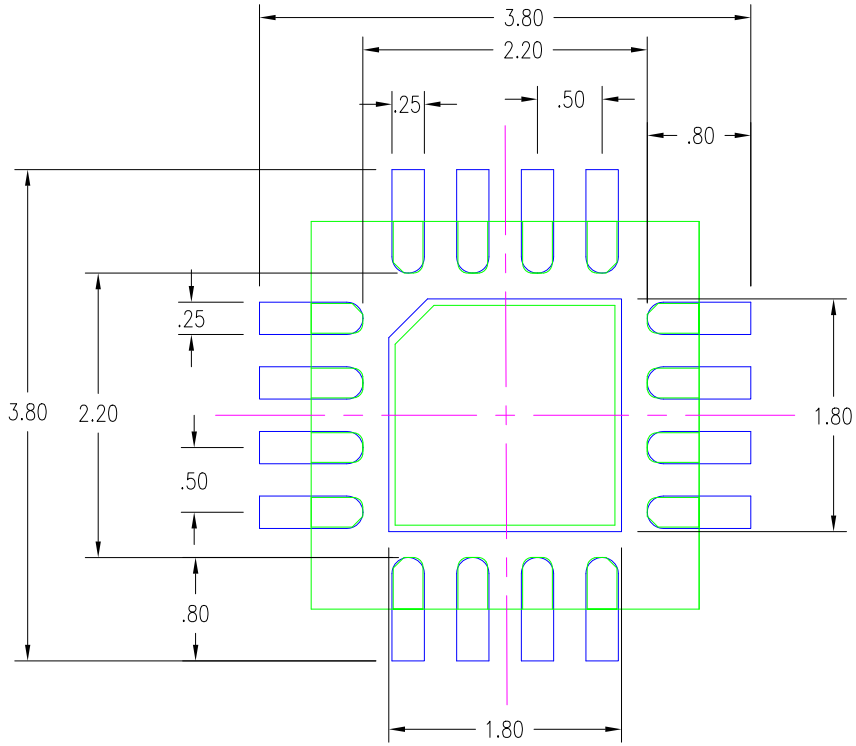



16LD QFN 3X3 (0.5MM PITCH)

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL XX± XXX± XXXX±<br>ANGULAR ± | | IDT www.IDT.com | 6024 Silver Creek Valley Road<br>San Jose, CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-8591 |
| APPROVALS | DATE | TITLE | NL/NLG16 PACKAGE OUTLINE<br>3.0 x 3.0 mm BODY<br>0.5 mm PITCH QFN |
| DRAWN RAC | 10/15/08 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4169 / REV 01 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

# Package Outline and Package Dimensions (16-pin QFN), cont.

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/15/08 | RC |
| 01 | COMBINE POD & LAND PATTERN | 9/17/13 | KS |




NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

APPROVALS | DATE
DRAWN RAC 10/15/08
CHECKED

IDT
www.IDT.com
6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE NL/NLG16 PACKAGE OUTLINE
3.0 x 3.0 mm BODY
0.5 mm PITCH QFN

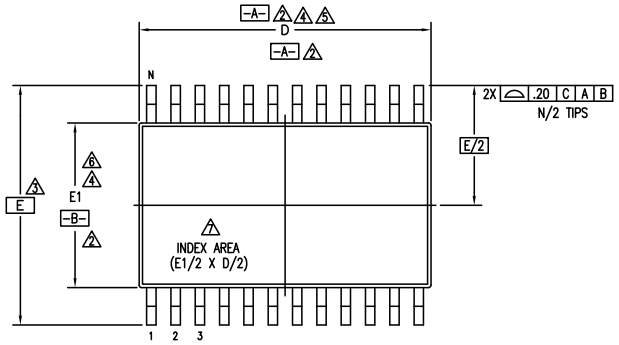
SIZE C | DRAWING No. PSC-4169 | REV 01

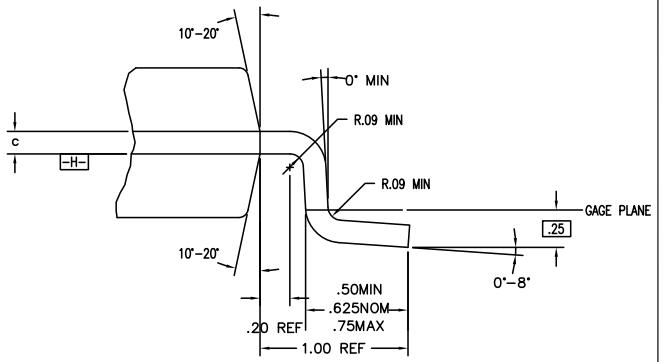
DO NOT SCALE DRAWING | SHEET 2 OF 2

# Package Outline and Package Dimensions (16-pin TSSOP)

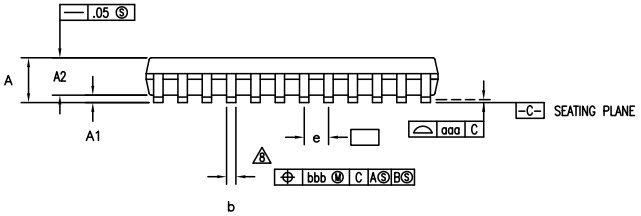
| DATE CREATED | REVISIONS REV | DESCRIPTION | AUTHOR |
|---|---|---|---|
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

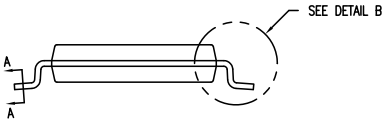
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

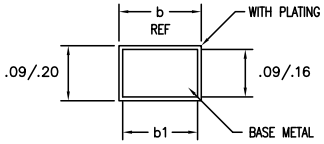



DETAIL B




SECTION A-A
9

| TOLERANCES UNLESS SPECIFIED | |
|---|---|
| DECIMAL | ANGULAR |
| XX± | ± |
| XXX± | |
| XXXX± | |

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TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4056 | 08 |

DO NOT SCALE DRAWING | SHEET 1 OF 3

# Package Outline and Package Dimensions (16-pin TSSOP), cont.

| DATE CREATED | REVISIONS REV | DESCRIPTION | AUTHOR |
|---|---|---|---|
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

| SYMBOL | PG/PGG8 JEDEC VARIATION AA | | | NOTE | PG/PGG14 JEDEC VARIATION AB-1 | | | NOTE | PG/PGG16 JEDEC VARIATION AB | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | |
| A1 | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | |
| A2 | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | |
| D | 2.90 | 3.00 | 3.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 | 4.90 | 5.00 | 5.10 | 4,5 |
| E | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 |
| e | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | |
| b | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | |
| b1 | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | |
| aaa | – | – | .10 | | – | – | .10 | | – | – | .10 | |
| bbb | – | – | .10 | | – | – | .10 | | – | – | .10 | |
| N | 8 | | | | 14 | | | | 16 | | | |

| SYMBOL | PG/PGG20 JEDEC VARIATION AC | | | NOTE | PG/PGG24 JEDEC VARIATION AD | | | NOTE | PG/PGG28 JEDEC VARIATION AE | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | | MIN | NOM | MAX | | MIN | NOM | MAX | |
| A | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | | .85 | 1.10 | 1.20 | |
| A1 | .05 | .10 | .15 | | .05 | .10 | .15 | | .05 | .10 | .15 | |
| A2 | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | | .80 | 1.00 | 1.05 | |
| D | 6.40 | 6.50 | 6.60 | 4,5 | 7.70 | 7.80 | 7.90 | 4,5 | 9.60 | 9.70 | 9.80 | 4,5 |
| E | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 | 6.20 | 6.40 | 6.60 | 3 |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 | 4.30 | 4.40 | 4.50 | 4,6 |
| e | .65 BSC | | | | .65 BSC | | | | .65 BSC | | | |
| b | .19 | .25 | .30 | | .19 | .25 | .30 | | .19 | .25 | .30 | |
| b1 | .19 | .22 | .25 | | .19 | .22 | .25 | | .19 | .22 | .25 | |
| aaa | – | – | .10 | | – | – | .10 | | – | – | .10 | |
| bbb | – | – | .10 | | – | – | .10 | | – | – | .10 | |
| N | 20 | | | | 24 | | | | 28 | | | |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE –C–
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE –H–
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION AA, AB–1, AB, AC, AD & AE

| SYMBOL | OPTION T1 PGG14T1 JEDEC VARIATION AB-1 | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| A | .90 | 1.10 | 1.20 | |
| A1 | .05 | .10 | .15 | |
| A2 | .80 | 1.00 | 1.05 | |
| D | 4.90 | 5.00 | 5.10 | 4,5 |
| E | 6.20 | 6.40 | 6.60 | 3 |
| E1 | 4.30 | 4.40 | 4.50 | 4,6 |
| e | .65 BSC | | | |
| b | .19 | .25 | .30 | |
| b1 | .19 | .22 | .25 | |
| c | .09 | – | .20 | |
| aaa | – | – | .10 | |
| bbb | – | – | .10 | |
| N | 14 | | | |

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

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TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C | DRAWING No. PSC–4056 | REV 08

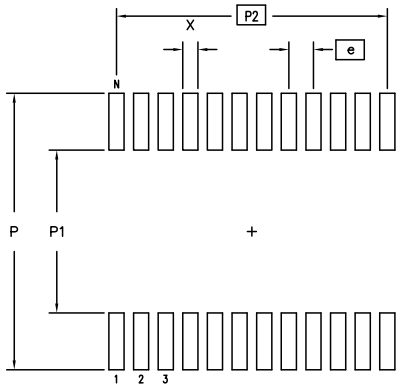
DO NOT SCALE DRAWING | SHEET 2 OF 3

# Package Outline and Package Dimensions (16-pin TSSOP), cont.

| DATE CREATED | REVISIONS REV | DESCRIPTION | AUTHOR |
|---|---|---|---|
| 08/25/98 | 02 | ADD 14 & 16 LD | T. VU |
| 07/10/99 | 03 | ADD 8 LD | T. VU |
| 5/23/01 | 04 | ADDED TOPMARK TO TITLE | |
| 10/14/04 | 05 | ADD "GREEN" PGG NOMENCLATURE | TU VU |
| 3/8/13 | 06 | ADDED PACKAGE CODE | RAC |
| 9/3/14 | 07 | ADD TOLERANCE FOR A, A1, E AND b | CK LEE |
| 3/10/17 | 08 | ADD OPTION T1 | R.TANH |

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

LAND PATTERN DIMENSIONS




| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 | 7.20 | 7.40 |
| P1 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 | 4.20 | 4.40 |
| P2 | 1.95 BSC | | 3.90 BSC | | 4.55 BSC | | 5.85 BSC | | 7.15 BSC | | 8.45 BSC | |
| X | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 | .30 | .50 |
| e | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | | .65 BSC | |
| N | 8 | | 14 | | 16 | | 20 | | 24 | | 28 | |

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DECIMAL XX± XXX± XXXX± ANGULAR ±

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TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C | DRAWING No. PSC-4056 | REV 08

DO NOT SCALE DRAWING | SHEET 3 OF 3

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 5V41065PGG | See Page 11 | Tubes | 16-pin TSSOP | 0 to +70° C |
| 5V41065PGG8 | | Tape and Reel | 16-pin TSSOP | 0 to +70° C |
| 5V41065PGGI | | Tubes | 16-pin TSSOP | -40 to +85° C |
| 5V41065PGGI8 | | Tape and Reel | 16-pin TSSOP | -40 to +85° C |
| 5V41065NLG | See Page 11 | Trays | 16-pin QFN | 0 to +70° C |
| 5V41065NLG8 | | Tape and Reel | 16-pin QFN | 0 to +70° C |
| 5V41065NLGI | | Trays | 16-pin QFN | -40 to +85° C |
| 5V41065NLGI8 | | Tape and Reel | 16-pin QFN | -40 to +85° C |

**"G" after the two-letter package code are the Pb-Free configuration, RoHS compliant.**

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## Revision History

| Rev. | Originator | Date | Description of Change |
|---|---|---|---|
| A | | 07/15/08 | New datasheet; Preliminary initial release. |
| B | RDW | 01/13/10 | Added Gen2 to title; update Electrical tables per char; added Differential Phase Jitter table. |
| C | RDW | 04/27/10 | Updated electrical tables per char; VDD is now 3.3 ±5%; released to final. |
| D | RDW | 07/19/10 | 1. Updated title and general description<br>2. Updated cycle-to-cycle jitter spec from 125 to 100 ps. |
| E | RDW | 11/21/11 | 1. Changed title to "2 Output PCIe GEN1/2 Synthesizer"<br>2. Added note to Features section: "For PCIe Gen3 applications, see 5V41235"<br>3. Updated Differential Phase Jitter table. |
| F | J, Chao | 08/26/13 | 1. Added 16VFQFPN notes in Features section<br>2. Added pinout and "Output/Spread Selection" table for 16VFQFPN.<br>3. Updated Pin Description table to include VFQFPN pin descriptions.<br>4. Added Thermal Characteristics table for 16VFQFPN.<br>5. Added marking diagrams for 16VFQFPN.<br>6. Added Package Dimensions/Drawing for 16VFQFPN.<br>7. Updated Ordering Information to include 16VFQFPN. |
| G | C.P. | 04/17/17 | 1. Replaced package outline drawings with latest NLG16 and PGG16 drawings.<br>2. Updated legal disclaimer. |

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