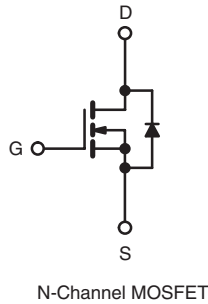
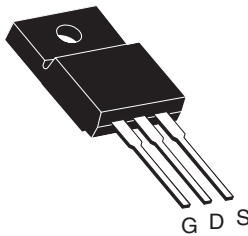


## Power MOSFET

### PRODUCT SUMMARY

|                           |                        |       |
|---------------------------|------------------------|-------|
| $V_{DS}$ (V)              | 60                     |       |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10\text{ V}$ | 0.028 |
| $Q_g$ (Max.) (nC)         | 95                     |       |
| $Q_{gs}$ (nC)             | 27                     |       |
| $Q_{gd}$ (nC)             | 46                     |       |
| Configuration             | Single                 |       |

#### TO-220 FULLPAK



### FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> ( $t = 60\text{ s}$ ;  $f = 60\text{ Hz}$ )
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. The isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

### ORDERING INFORMATION

|                |                             |
|----------------|-----------------------------|
| Package        | TO-220 FULLPAK              |
| Lead (Pb)-free | IRFIZ44GPbF<br>SiHFIZ44G-E3 |
| SnPb           | IRFIZ44G<br>SiHFIZ44G       |

### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ °C}$ , unless otherwise noted

| PARAMETER                                        | SYMBOL           | LIMIT                 | UNIT     |
|--------------------------------------------------|------------------|-----------------------|----------|
| Drain-Source Voltage                             | $V_{DS}$         | 60                    | V        |
| Gate-Source Voltage                              | $V_{GS}$         | $\pm 20$              |          |
| Continuous Drain Current                         | $I_D$            | $T_C = 25\text{ °C}$  | A        |
|                                                  |                  | $T_C = 100\text{ °C}$ |          |
| Pulsed Drain Current <sup>a</sup>                | $I_{DM}$         | 120                   |          |
| Linear Derating Factor                           |                  | 0.32                  | W/°C     |
| Single Pulse Avalanche Energy <sup>b</sup>       | $E_{AS}$         | 100                   | mJ       |
| Maximum Power Dissipation                        | $P_D$            | 48                    | W        |
| Peak Diode Recovery dV/dt <sup>c</sup>           | dV/dt            | 4.5                   | V/ns     |
| Operating Junction and Storage Temperature Range | $T_J, T_{stg}$   | - 55 to + 175         | °C       |
| Soldering Recommendations (Peak Temperature)     | for 10 s         | 300 <sup>d</sup>      |          |
| Mounting Torque                                  | 6-32 or M3 screw | 10                    | lbf · in |
|                                                  |                  | 1.1                   | N · m    |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ °C}$ ,  $L = 129\text{ }\mu\text{H}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 30\text{ A}$  (see fig. 12).
- $I_{SD} \leq 52\text{ A}$ ,  $dI/dt \leq 250\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ °C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

| PARAMETER                        | SYMBOL     | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient      | $R_{thJA}$ | -    | 65   | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | -    | 3.1  |      |

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

| PARAMETER                                 | SYMBOL                           | TEST CONDITIONS                                                                                                                |                                                                                  | MIN. | TYP.  | MAX.  | UNIT |
|-------------------------------------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------|-------|-------|------|
| Static                                    |                                  |                                                                                                                                |                                                                                  |      |       |       |      |
| Drain-Source Breakdown Voltage            | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA                                                                                 |                                                                                  | 60   | -     | -     | V    |
| V <sub>DS</sub> Temperature Coefficient   | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA                                                                                      |                                                                                  | -    | 0.060 | -     | V/°C |
| Gate-Source Threshold Voltage             | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                                                                    |                                                                                  | 2.0  | -     | 4.0   | V    |
| Gate-Source Leakage                       | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V                                                                                                       |                                                                                  | -    | -     | ± 100 | nA   |
| Zero Gate Voltage Drain Current           | I <sub>DSS</sub>                 | V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V                                                                                  |                                                                                  | -    | -     | 25    | μA   |
|                                           |                                  | V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C                                                         |                                                                                  | -    | -     | 250   |      |
| Drain-Source On-State Resistance          | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V                                                                                                         | I <sub>D</sub> = 18 A <sup>b</sup>                                               | -    | -     | 0.028 | Ω    |
| Forward Transconductance                  | g <sub>fs</sub>                  | V <sub>DS</sub> = 25 V, I <sub>D</sub> = 18 A <sup>b</sup>                                                                     |                                                                                  | 15   | -     | -     | S    |
| Dynamic                                   |                                  |                                                                                                                                |                                                                                  |      |       |       |      |
| Input Capacitance                         | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 25 V,<br>f = 1.0 MHz, see fig. 5                                                   |                                                                                  | -    | 2500  | -     | pF   |
| Output Capacitance                        | C <sub>oss</sub>                 |                                                                                                                                |                                                                                  | -    | 1200  | -     |      |
| Reverse Transfer Capacitance              | C <sub>rss</sub>                 |                                                                                                                                |                                                                                  | -    | 200   | -     |      |
| Drain to Sink Capacitance                 | C                                | f = 1.0 MHz                                                                                                                    |                                                                                  | -    | 12    | -     |      |
| Total Gate Charge                         | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V                                                                                                         | I <sub>D</sub> = 52 A, V <sub>DS</sub> = 48 V,<br>see fig. 6 and 13 <sup>b</sup> | -    | -     | 95    | nC   |
| Gate-Source Charge                        | Q <sub>gs</sub>                  |                                                                                                                                |                                                                                  | -    | -     | 27    |      |
| Gate-Drain Charge                         | Q <sub>gd</sub>                  |                                                                                                                                |                                                                                  | -    | -     | 46    |      |
| Turn-On Delay Time                        | t <sub>d(on)</sub>               | V <sub>DD</sub> = 30 V, I <sub>D</sub> = 52 A,<br>R <sub>G</sub> = 9.1 Ω, R <sub>D</sub> = 0.54 Ω,<br>see fig. 10 <sup>b</sup> |                                                                                  | -    | 19    | -     | ns   |
| Rise Time                                 | t <sub>r</sub>                   |                                                                                                                                |                                                                                  | -    | 120   | -     |      |
| Turn-Off Delay Time                       | t <sub>d(off)</sub>              |                                                                                                                                |                                                                                  | -    | 55    | -     |      |
| Fall Time                                 | t <sub>f</sub>                   |                                                                                                                                |                                                                                  | -    | 86    | -     |      |
| Internal Drain Inductance                 | L <sub>D</sub>                   | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact                                                     |                                                                                  | -    | 4.5   | -     | nH   |
| Internal Source Inductance                | L <sub>S</sub>                   |                                                                                                                                |                                                                                  | -    | 7.5   | -     |      |
| Drain-Source Body Diode Characteristics   |                                  |                                                                                                                                |                                                                                  |      |       |       |      |
| Continuous Source-Drain Diode Current     | I <sub>S</sub>                   | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode                                                       |                                                                                  | -    | -     | 30    | A    |
| Pulsed Diode Forward Current <sup>a</sup> | I <sub>SM</sub>                  |                                                                                                                                |                                                                                  | -    | -     | 120   |      |
| Body Diode Voltage                        | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 30 A, V <sub>GS</sub> = 0 V <sup>b</sup>                                              |                                                                                  | -    | -     | 2.5   | V    |
| Body Diode Reverse Recovery Time          | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = 52 A, dI/dt = 100 A/μs <sup>b</sup>                                                   |                                                                                  | -    | 140   | 300   | ns   |
| Body Diode Reverse Recovery Charge        | Q <sub>rr</sub>                  |                                                                                                                                |                                                                                  | -    | 1.2   | 2.8   | μC   |
| Forward Turn-On Time                      | t <sub>on</sub>                  | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )                              |                                                                                  |      |       |       |      |

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

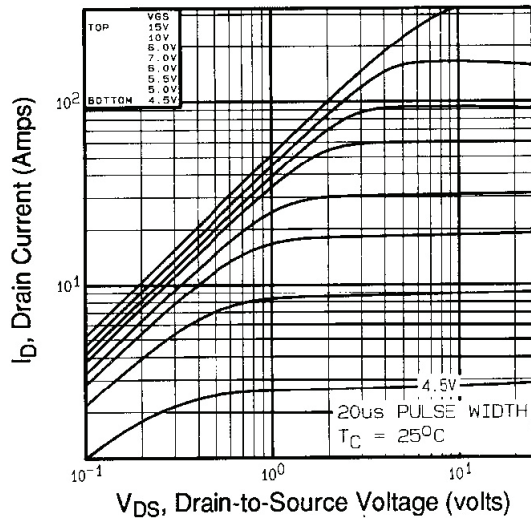


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

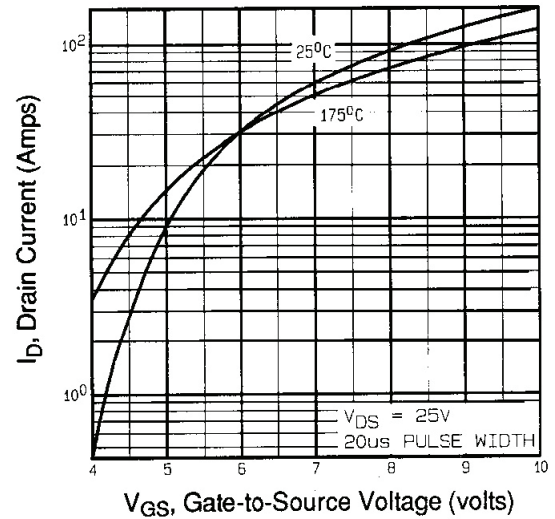


Fig. 3 - Typical Transfer Characteristics

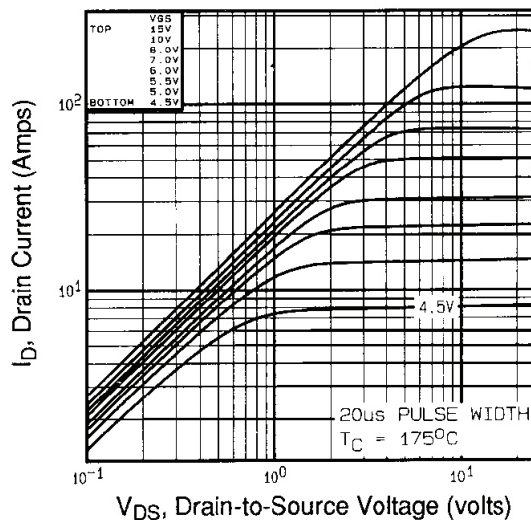


Fig. 2 - Typical Output Characteristics,  $T_C = 175^\circ\text{C}$

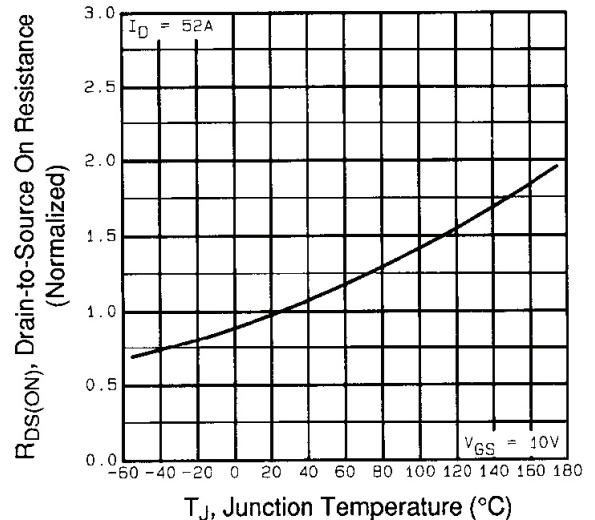


Fig. 4 - Normalized On-Resistance vs. Temperature

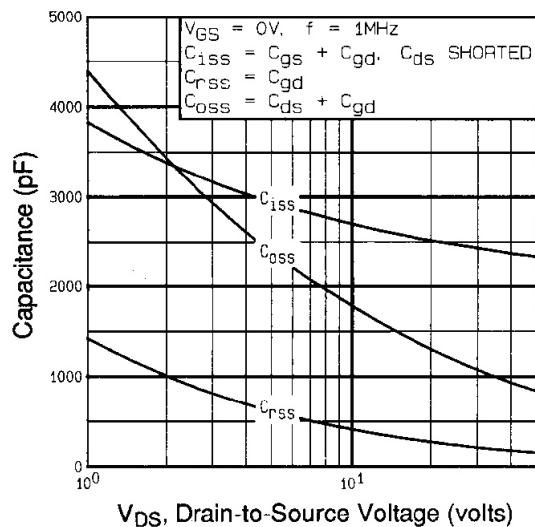


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

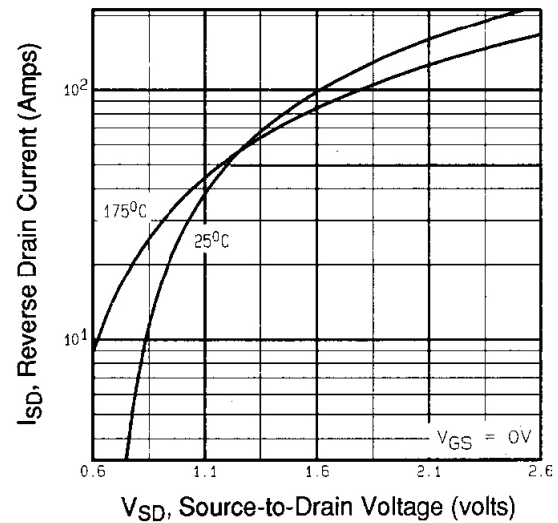


Fig. 7 - Typical Source-Drain Diode Forward Voltage

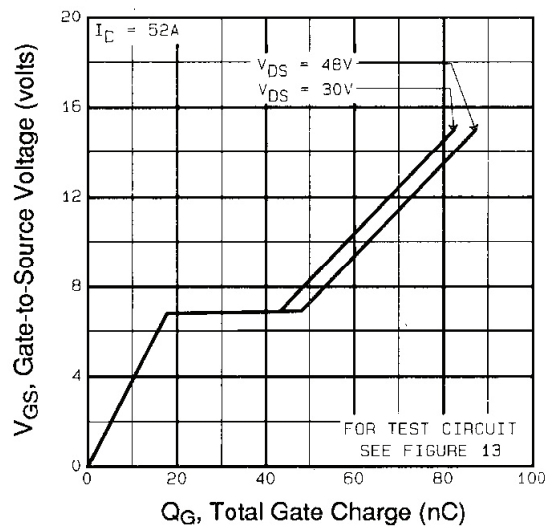


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

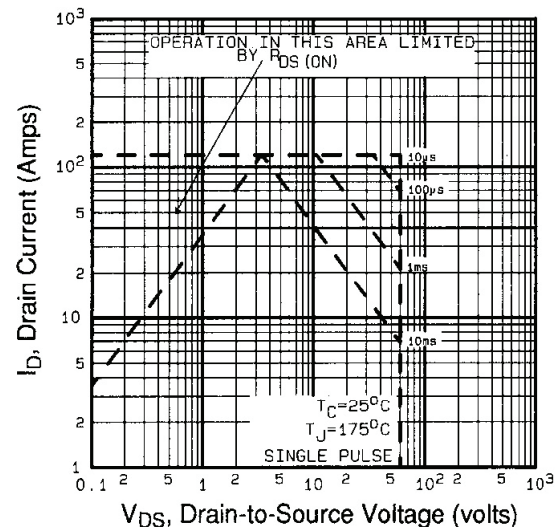


Fig. 8 - Maximum Safe Operating Area

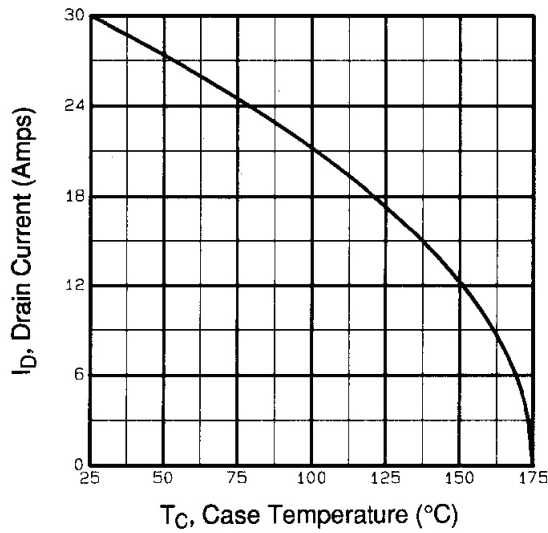


Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

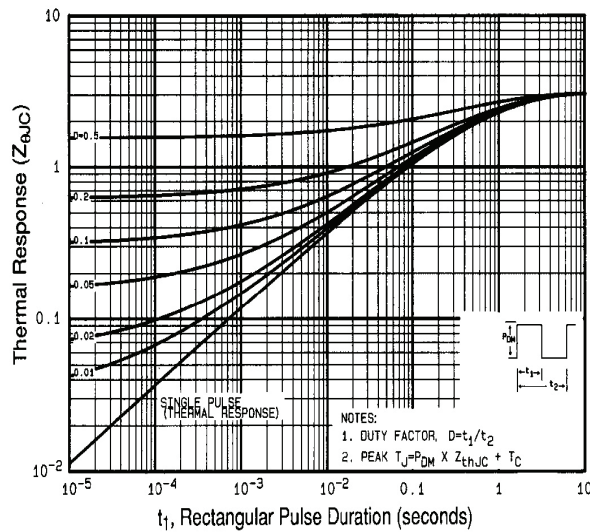


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

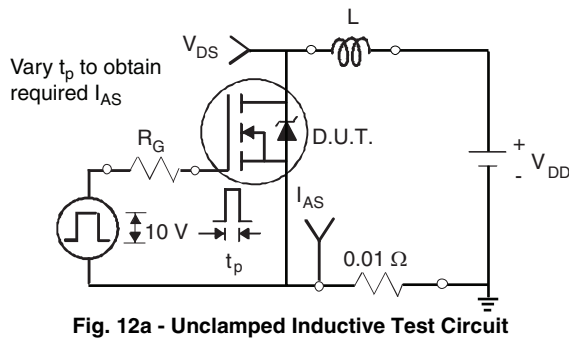


Fig. 12a - Unclamped Inductive Test Circuit

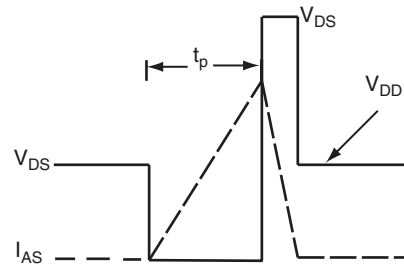


Fig. 12b - Unclamped Inductive Waveforms

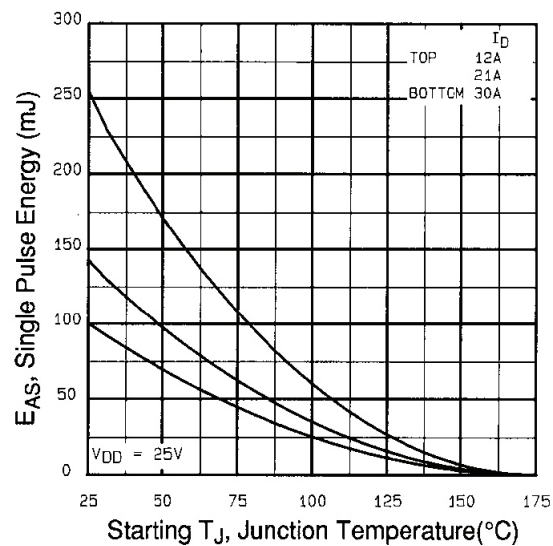


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

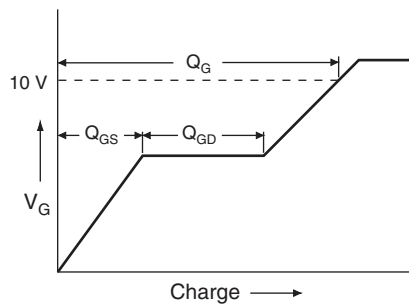


Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit

① Driver gate drive

P.W. Period  $D = \frac{\text{P.W.}}{\text{Period}}$

$V_{GS} = 10 \text{ V}^*$

② D.U.T.  $I_{SD}$  waveform

Reverse recovery current

Body diode forward current

$di/dt$

③ D.U.T.  $V_{DS}$  waveform

Diode recovery  $dV/dt$

$V_{DD}$

Body diode forward drop

④ Inductor current

Ripple  $\leq 5\%$

$I_{SD}$

\*  $V_{GS} = 5 \text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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