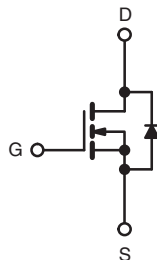
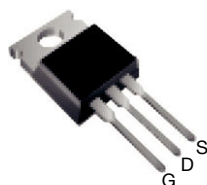


D Series Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	450	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.6
Q_g max. (nC)	30	
Q_{gs} (nC)	4	
Q_{gd} (nC)	7	
Configuration	Single	

TO-220AB


N-Channel MOSFET

FEATURES

- Optimal Design
 - Low Area Specific On-Resistance
 - Low Input Capacitance (C_{iss})
 - Reduced Capacitive Switching Losses
 - High Body Diode Ruggedness
 - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
 - Low Cost
 - Simple Gate Drive Circuitry
 - Low Figure-of-Merit (FOM): $R_{on} \times Q_g$
 - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Note

- * Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics
 - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
 - SMPS
- Industrial
 - Welding
 - Induction Heating
 - Motor Drives
- Battery Chargers



RoHS*
COMPLIANT
HALOGEN
FREE
Available

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	SiHP10N40D-E3
Lead (Pb)-free and Halogen-free	SiHP10N40D-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	400	V
Gate-Source Voltage	V_{GS}	± 30	
Gate-Source Voltage AC ($f > 1$ Hz)		30	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	23	
Linear Derating Factor		1.2	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	194	mJ
Maximum Power Dissipation	P_D	147	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	dV/dt	$T_J = 125$ °C	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak Temperature)		for 10 s	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 2.3$ mH, $R_g = 25$ Ω , $I_{AS} = 13$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, starting $T_J = 25$ °C.

**THERMAL RESISTANCE RATINGS**

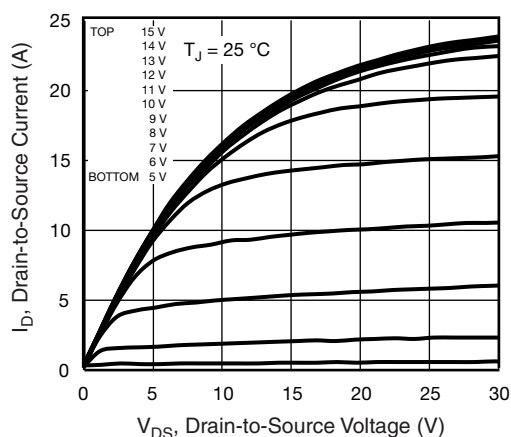
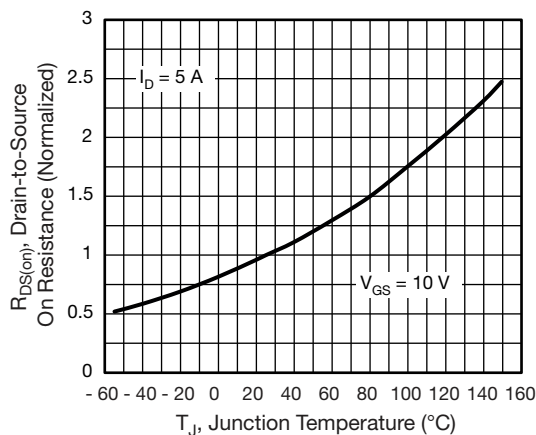
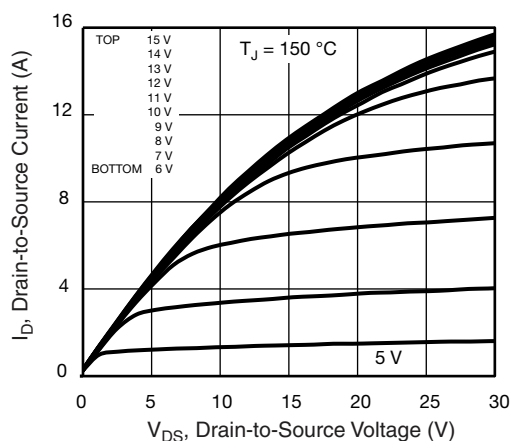
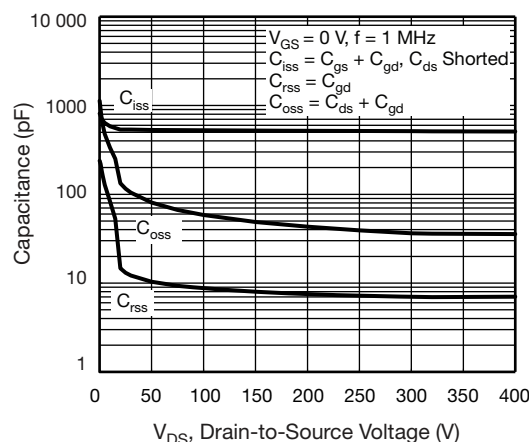
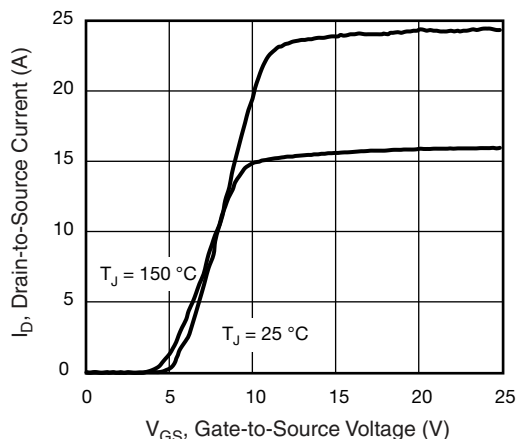
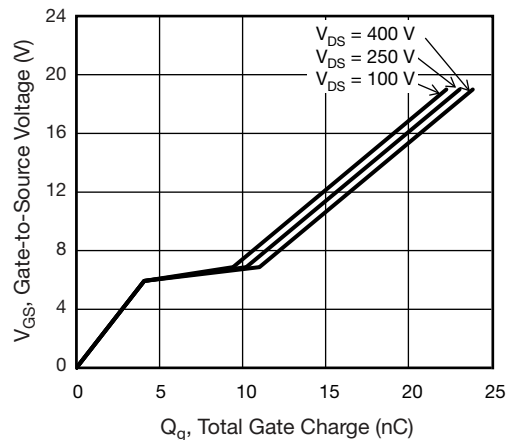
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.85	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		400	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 250 μA		-	0.53	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3	-	5	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5 A	-	0.5	0.6	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 5 A		-	2.7	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	526	-	pF
Output Capacitance	C _{oss}			-	59	-	
Reverse Transfer Capacitance	C _{rss}			-	9	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{GS} = 0 V, V _{DS} = 0 V to 320 V		-	66	-	pF
Effective output capacitance, time related ^b	C _{o(tr)}			-	84	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 5 A, V _{DS} = 320 V	-	15	30	nC
Gate-Source Charge	Q _{gs}			-	4	-	
Gate-Drain Charge	Q _{gd}			-	7	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 10 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	12	24	ns
Rise Time	t _r			-	18	36	
Turn-Off Delay Time	t _{d(off)}			-	18	36	
Fall Time	t _f			-	14	28	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	1.8	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10	A
Pulsed Diode Forward Current	I _{SM}			-	-	40	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 5 A, dI/dt = 100 A/μs, V _R = 25 V		-	230	-	ns
Reverse Recovery Charge	Q _{rr}			-	1.6	-	μC
Reverse Recovery Current	I _{RRM}			-	14	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

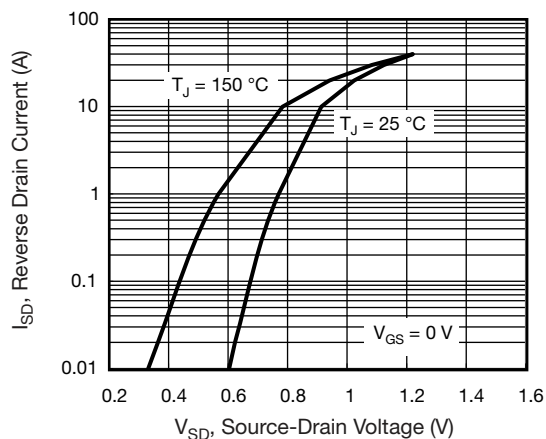
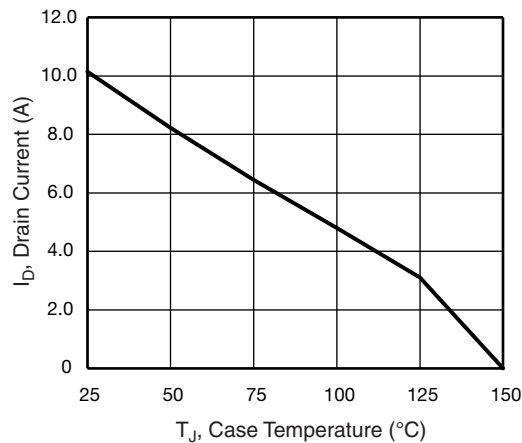
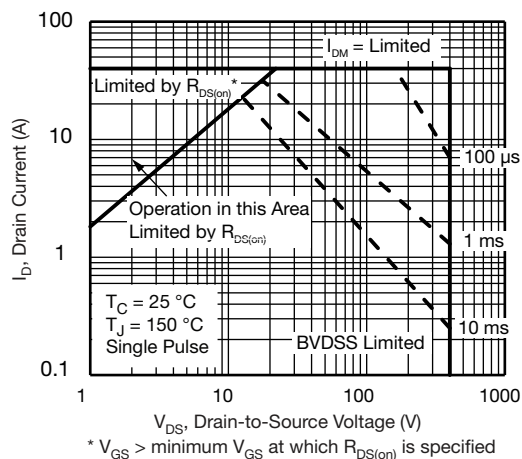
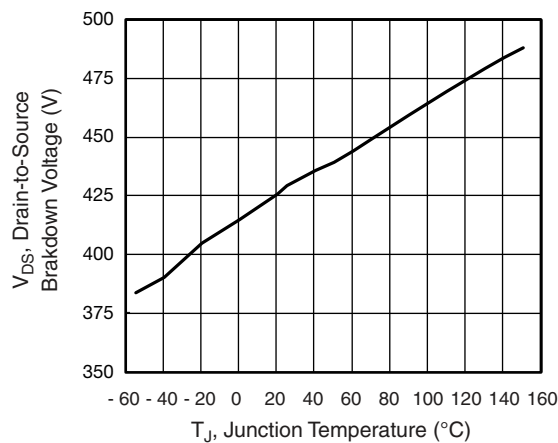
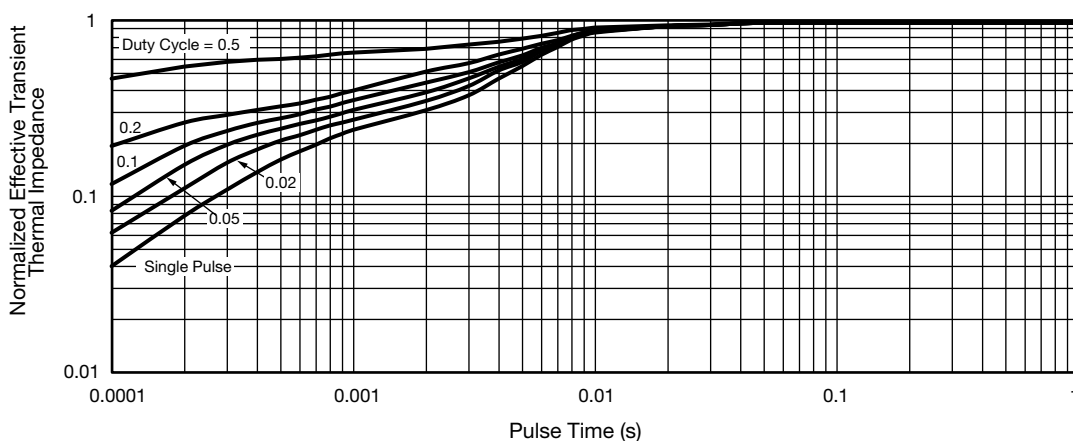
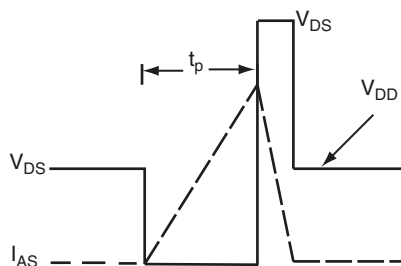

Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Maximum Safe Operating Area

Fig. 10 - Temperature vs. Drain-to-Source Voltage

Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case


Fig. 12 - Switching Time Test Circuit

Fig. 16 - Basic Gate Charge Waveform

Fig. 13 - Switching Time Waveforms

Fig. 17 - Gate Charge Test Circuit

Fig. 14 - Unclamped Inductive Test Circuit

Fig. 15 - Unclamped Inductive Waveforms

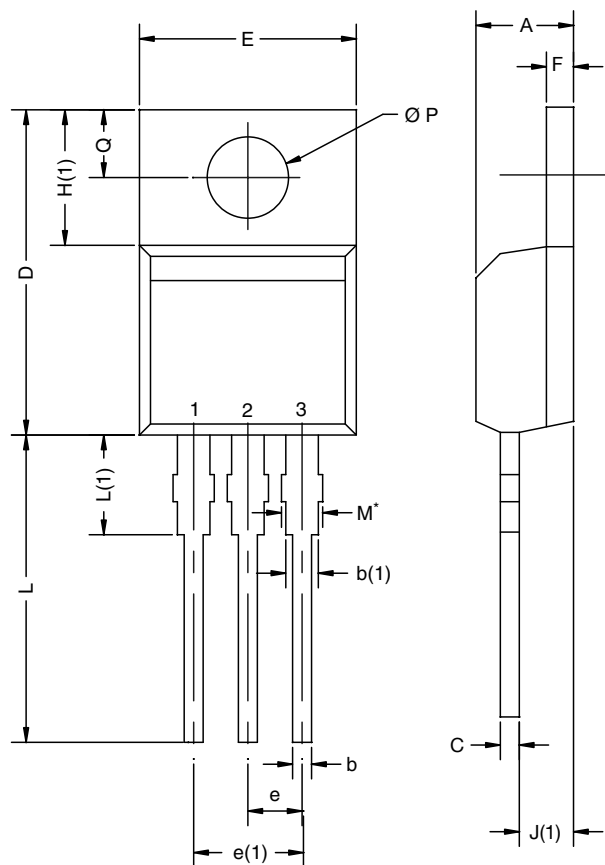

Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

- * $M = 1.32$ mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM
- Xi'an and Mingxin actual photo





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