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DS52096A

# dsPIC33FJ32MC104 Motor Control Plug-in Module

## Overview

The dsPIC33FJ32MC104 Motor Control Plug-in Module (Part No. MA330032) is designed to demonstrate the capabilities of the dsPIC33FJ32MC104 motor control device using the dsPICDEM™ MCLV-2 Development Board (DM330021-2) and dsPICDEM MCHV-2 Development Board (DM330023-2). The PIM is also compatible with the dsPICDEM MCLV Development Board (DM330021) and dsPICDEM MCHV Development Board (DM330023).

The dsPIC33FJ32MC104 device is an ultra low-cost 16-bit Digital Signal Controller (DSC) in a 44-pin 10x10 mm TQFP package. The 44 pins of this device host 14 analog inputs, 35 pins with general I/O function and 26 pins with Peripheral Pin Select (PPS) functionality.

The dsPIC33FJ32MC104 Motor Control Plug-in Module provides test points and zero ohm resistors for easier testing and debugging. In-circuit programming/debugging is accommodated using the PGEC3-PGED3 pin pair. The PIM supports a PWM Fault input on the FLTA pin.

Figure 1 provides the schematics for the dsPIC33FJ32MC104 Motor Control Plug-in Module. Table 1 shows the mapping between the device pins and the PIM pins.

**Note:** For use of this PIM with the dsPICDEM MCLV-2 Development Board (DM330021-2) and dsPICDEM MCHV-2 Development Board (DM330023-2):

Insert the external op amp configuration matrix board into the appropriate jumper before powering up the development board.

**Table 1: 44-Pin Device to 100-Pin PIM Mapping**

| Device Pin # | Device Functional Description | PIM Pin # |
|---|---|---|
| 1 | SDA/RP9/CN21/RB9 | 50 |
| 2 | RP22/CN18/RC6 | 80 |
| 3 | RP23/CN17/RC7 | 47 |
| 4 | RP24/CN20/RC8 | 48 |
| 5 | RP25/CN19/RC9 | 49 |
| 6 | VSS | 15, 45, 65, 75 |
| 7 | VCAP | N/A |
| 8 | PWM1H3/RP10/CN16/RB10 | 3 |
| 9 | PWM1L3/RP11/CN15/RB11 | 100 |
| 10 | PWM1H2/RP12/CN14/RB12 | 99 |
| 11 | PWM1L2/RP13/CN13/RB13 | 98 |
| 12 | RA10 | 60 |
| 13 | RA7 | 1 |
| 14 | PWM1H1/RTCC/RP14/CN12/RB14 | 94 |
| 15 | PWM1L1/RP15/CN11/RB15 | 93 |
| 16 | AVSS | 31 |
| 17 | AVDD | 30 |
| 18 | $\overline{\text{MCLR}}$ | 13 |
| 19 | PGED2/AN0/C3INB/C1INA/CTED1/CN2/RA0 | 25 |
| 20 | PGEC2/AN1/C3INA/C1INB/CTED2/CN3/RA1 | 24 |
| 21 | PGED1/AN2/C2INA/C1INC/CTCMP/RP0/CN4/RB0 | 35 |
| 22 | PGEC1/AN3/CVREFI/CVREFO/C2INB/C1IND/RP1/CN5/RB1 | 41 |
| 23 | AN4/C3INC/C2INC/RP2/CN6/RB2 | 42 |
| 24 | AN5/C3IND/C2IND/RP3/CN7/RB3 | 43 |
| 25 | AN6/RP16/CN8/RC0 | 29 |
| 26 | AN7/RP17/CN9/RC1 | 61 |
| 27 | AN8/RP18/CN10/RC2 | 32, 33 |
| 28 | VDD | 2, 16, 37, 46, 62, 86 |
| 29 | VSS | 15, 45, 65, 75 |
| 30 | OSC1/CLKI/CN30/RA2 | 63 |
| 31 | OSC2/CLKO/CN29/RA3 | 64 |

**Table 1: 44-Pin Device to 100-Pin PIM Mapping (Continued)**

| Device Pin # | Device Functional Description | PIM Pin # |
|---|---|---|
| 32 | RA8 | 83 |
| 33 | PGED3/SOSCI/AN9/RP4/CN1/RB4 | 27 |
| 34 | PGEC3/SOSCO/AN10/T1CK/CN0/RA4 | 26 |
| 35 | RA9 | 84 |
| 36 | AN11/RP19/CN28/RC3 | 21 |
| 37 | AN12/RP20/CN25/RC4 | 22 |
| 38 | AN15/RP21/CN26/RC5 | 23 |
| 39 | VSS | 15, 45, 65, 75 |
| 40 | VDD | 2, 16, 37, 46, 62, 86 |
| 41 | FLTB/ASDA1/RP5/CN27/RB5 | N/A |
| 42 | FLTA/ASCL1/RP6/CN24/RB6 | 18 |
| 43 | INT0/RP7/CN23/RB7 | 68 |
| 44 | SCL1/RP8/CN22/RB8 | 69 |

**Figure 1: Schematics**