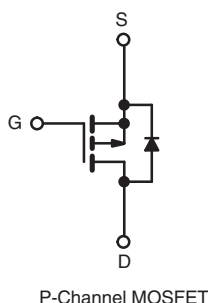
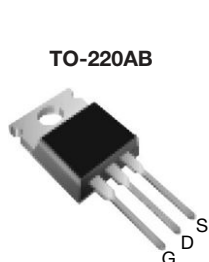


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	1.5
Q_g (Max.) (nC)	22	
Q_{gs} (nC)	12	
Q_{gd} (nC)	10	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9620PbF SiHF9620-E3
SnPb	IRF9620 SiHF9620

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 14	
Linear Derating Factor		0.32	W/ $^\circ\text{C}$
Maximum Power Dissipation	P_D	40	W
Peak Diode Recovery dV/dt^b	dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^c	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $I_{SD} \leq 3.5$ A, $dI/dt \leq 95$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

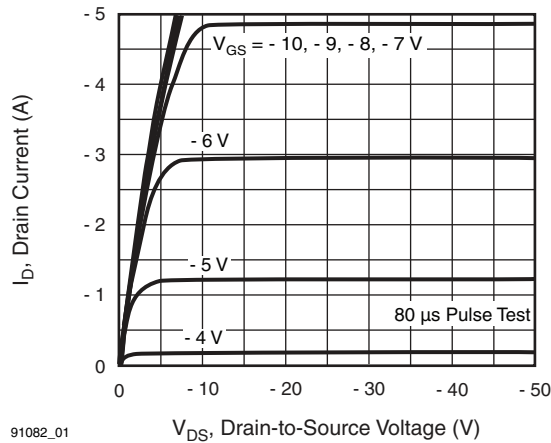
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

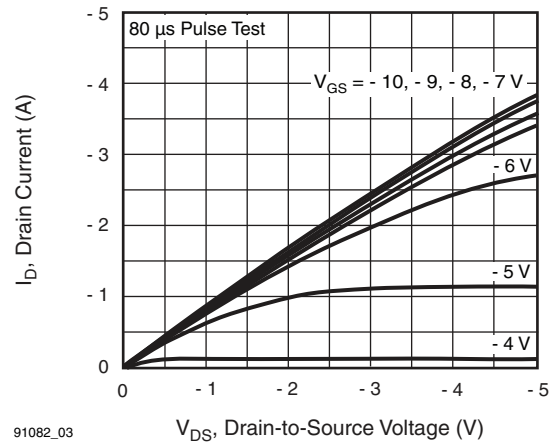
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = - 250\text{ }\mu\text{A}$		- 200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = - 1\text{ mA}$		-	- 0.22	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = - 250\text{ }\mu\text{A}$		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = - 200\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	- 100	μA
		$V_{DS} = - 160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = - 10\text{ V}$	$I_D = - 1.5\text{ A}^b$	-	-	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = - 50\text{ V}$, $I_D = - 1.5\text{ A}^b$		1.0	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = - 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	350	-	pF
Output Capacitance	C_{oss}			-	100	-	
Reverse Transfer Capacitance	C_{rss}			-	30	-	
Total Gate Charge	Q_g	$V_{GS} = - 10\text{ V}$	$I_D = - 4.0\text{ A}$, $V_{DS} = - 160\text{ V}$, see fig. 11 and 18 ^b	-	-	22	nC
Gate-Source Charge	Q_{gs}			-	-	12	
Gate-Drain Charge	Q_{gd}			-	-	10	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = - 100\text{ V}$, $I_D = - 1.5\text{ A}$, $R_g = 50\text{ }\Omega$, $R_D = 67\text{ }\Omega$, see fig. 17 ^b		-	15	-	ns
Rise Time	t_r			-	25	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Fall Time	t_f			-	15	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 3.5	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	- 14	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = - 3.5\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	- 7.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = - 3.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	300	450	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.9	2.9	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

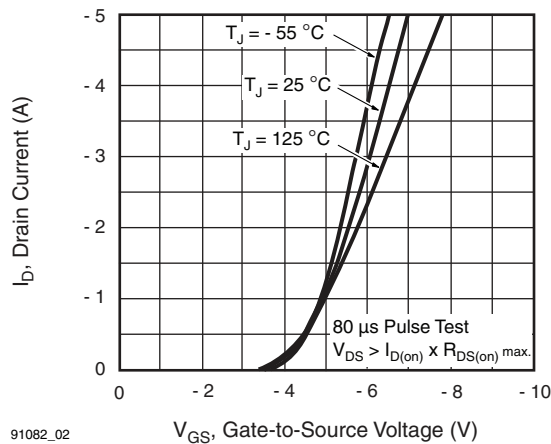
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


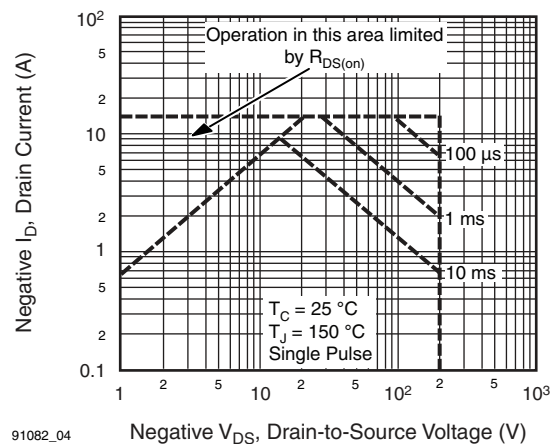
91082_01

Fig. 1 - Typical Output Characteristics


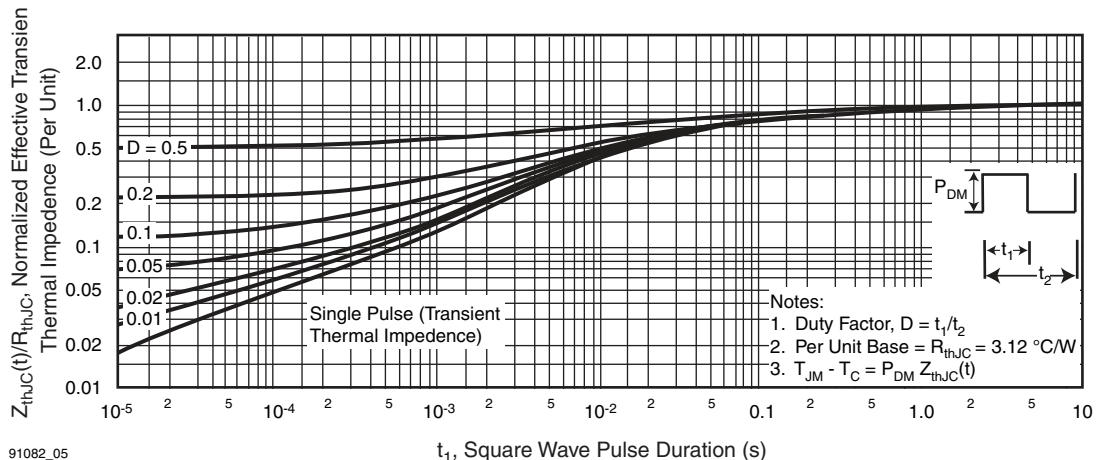
91082_03

Fig. 3 - Typical Saturation Characteristics


91082_02

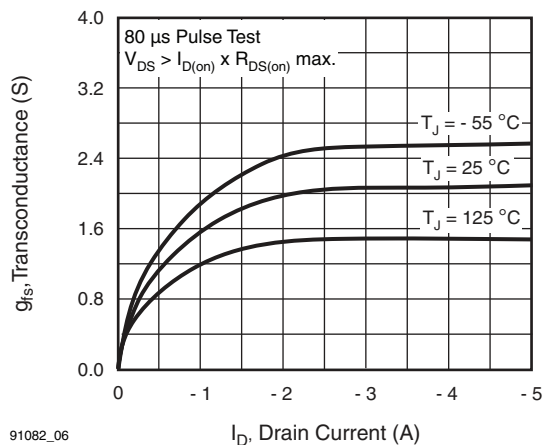
Fig. 2 - Typical Transfer Characteristics


91082_04

Fig. 4 - Maximum Safe Operating Area


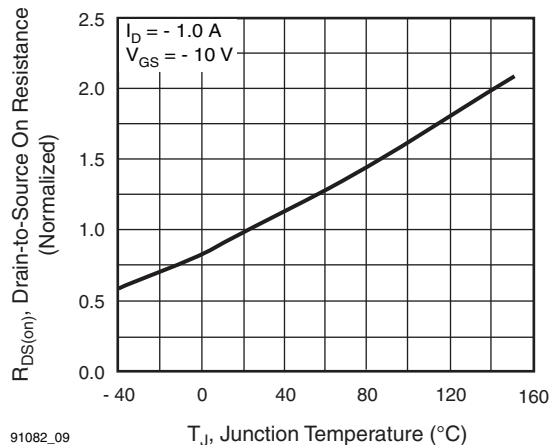
91082_05

Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration



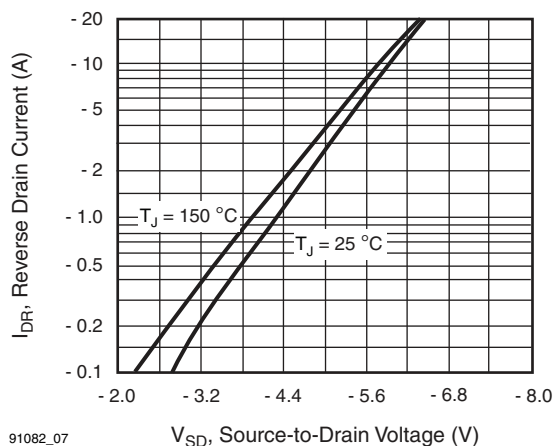
91082_06

Fig. 6 - Typical Transconductance vs. Drain Current



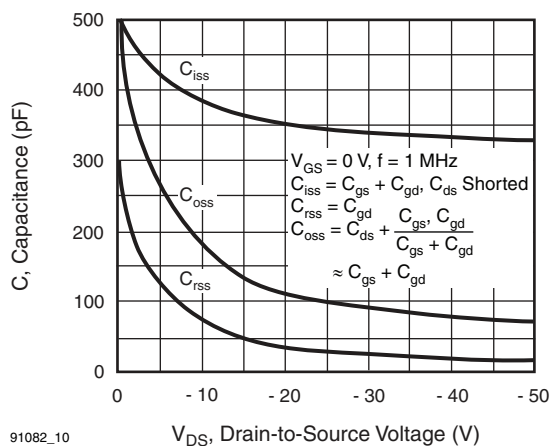
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Fig. 9 - Normalized On-Resistance vs. Temperature



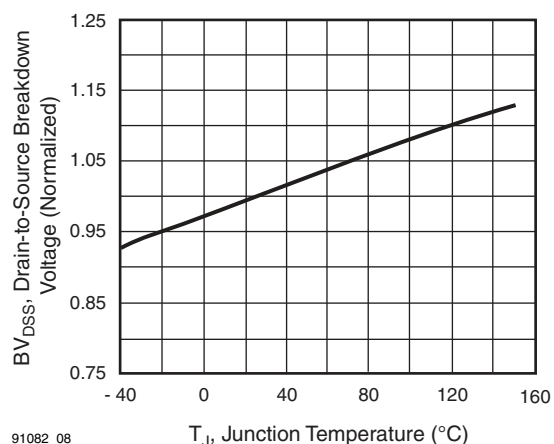
91082_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



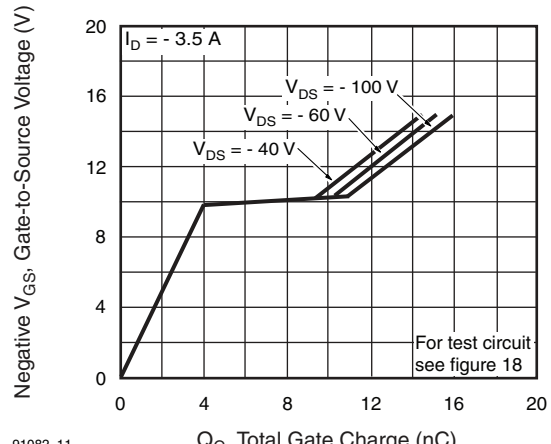
91082_10

Fig. 10 - Typical Capacitance vs. Drain-to-Source Voltage



91082_08

Fig. 8 - Breakdown Voltage vs. Temperature



91082_11

Fig. 11 - Typical Gate Charge vs. Gate-to-Source Voltage

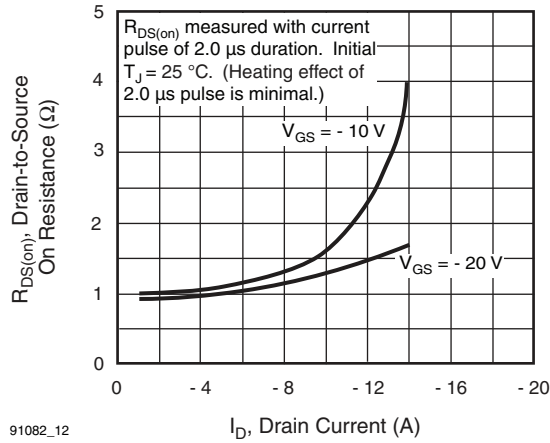


Fig. 12 - Typical On-Resistance vs. Drain Current

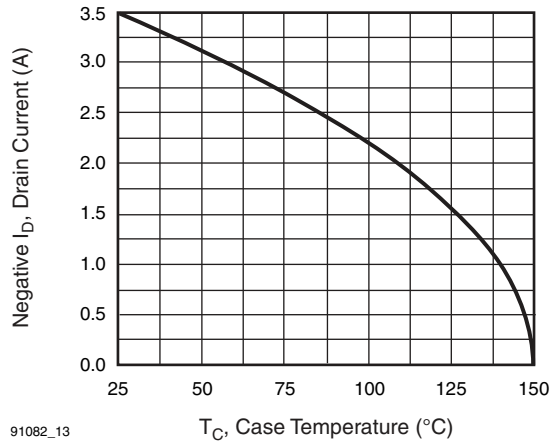


Fig. 13 - Maximum Drain Current vs. Case Temperature

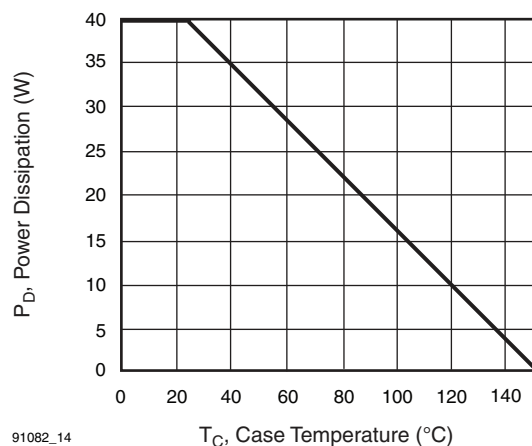


Fig. 14 - Power vs. Temperature Derating Curve

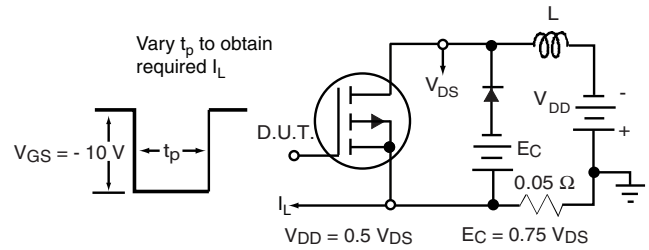


Fig. 15 - Clamped Inductive Test Circuit

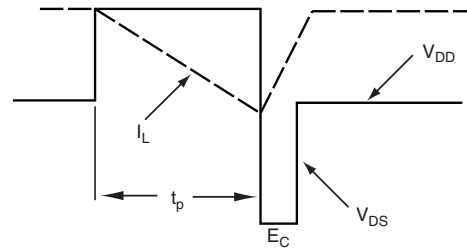


Fig. 16 - Clamped Inductive Waveforms

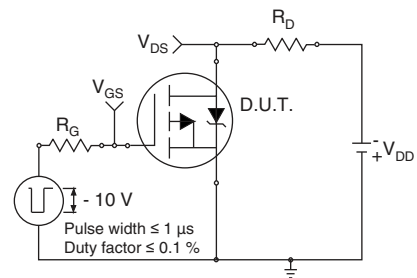


Fig. 17a - Switching Time Test Circuit

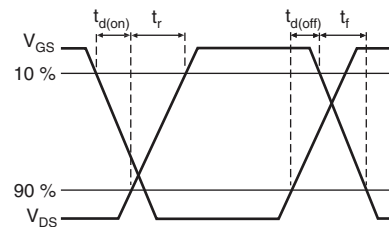


Fig. 17b - Switching Time Waveforms

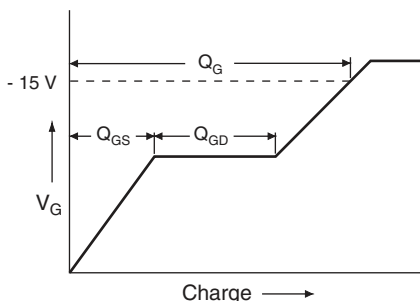


Fig. 18a - Basic Gate Charge Waveform

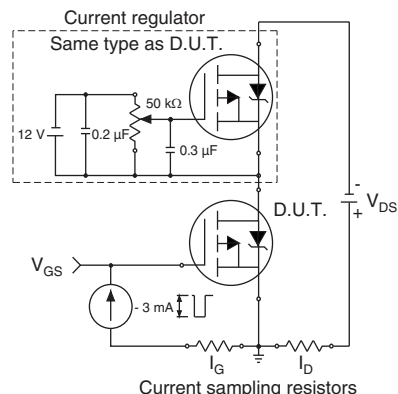


Fig. 18b - Gate Charge Test Circuit

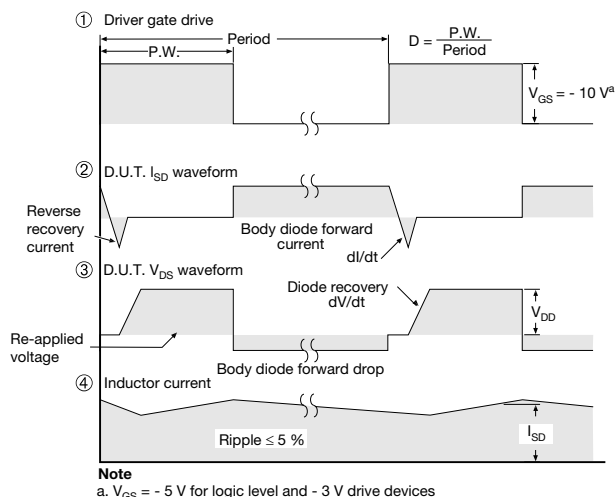
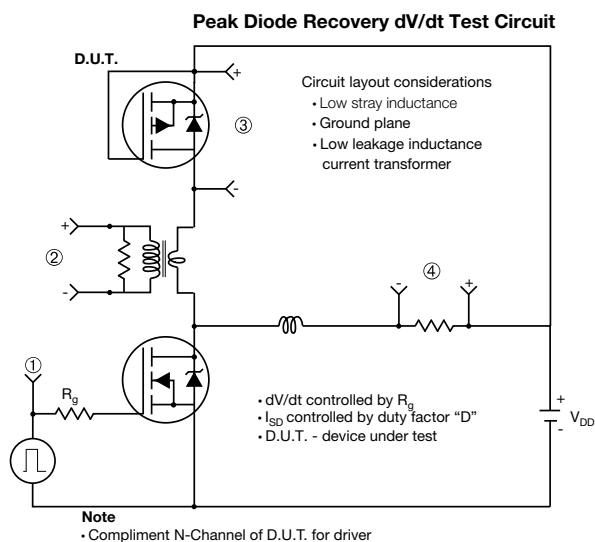
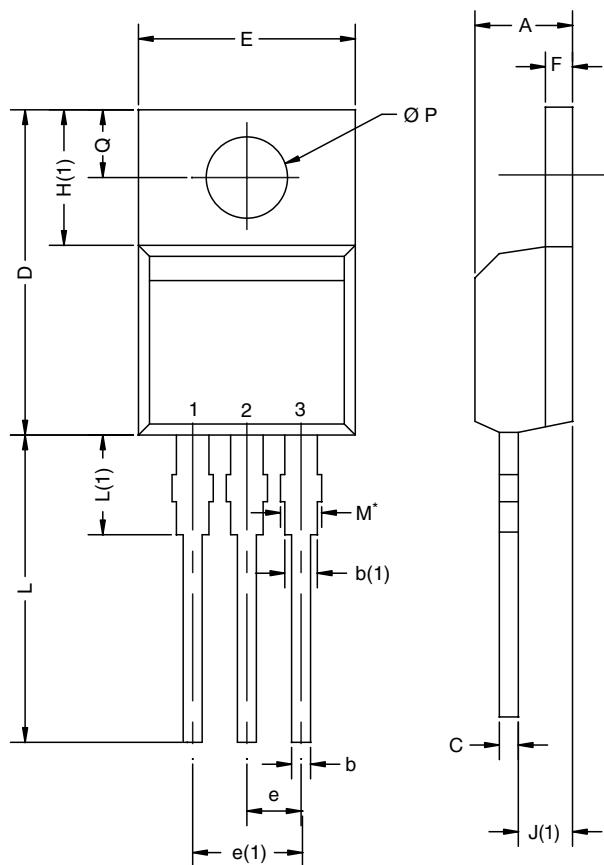


Fig. 19 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91082.

TO-220AB

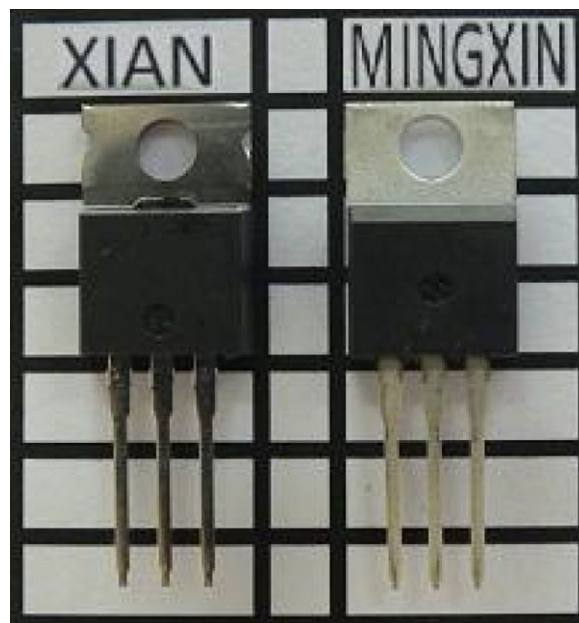


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
$\varnothing P$	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

- * M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM
- Xi'an and Mingxin actual photo





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