

3.2 Ω , Fast Switching Speed, +12 V / +5 V / +3 V / $\pm$ 5 V, 4- / 8-Channel Analog Multiplexers

DESCRIPTION

The DG9408E, DG9409E uses BiCMOS wafer fabrication technology that allows the DG9408E, DG9409E to operate on single and dual supplies. Single supply voltage ranges from 3 V to 16 V while dual supply operation is recommended with $\pm$ 3 V to $\pm$ 8 V.

The DG9408E is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0 , A_1 , A_2). The DG9409E is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0 , A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. The DG9408E, DG9409E are offered in a QFN package that has a nickel-palladium-gold device terminations and is represented by the lead (Pb)-free “-E4” suffix. The nickel-palladium-gold device terminations meet all the JEDEC® standards for reflow and MSL ratings.

FEATURES

- 3 V to 16 V single supply or $\pm$ 3 V to $\pm$ 8 V dual supply operation
- Low on-resistance - R_{ON} : 3.2 Ω typ.
- Fast switching: t_{ON} - 36 ns, t_{OFF} - 24 ns
- Break-before-make guaranteed
- Low leakage
- TTL, CMOS, LV logic (3 V) compatible
- 2500 V ESD protection (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

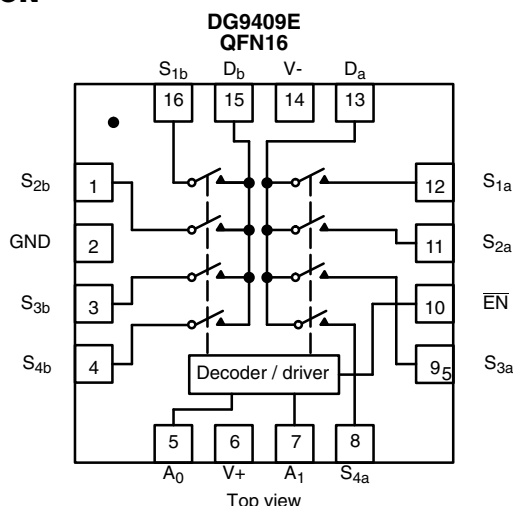
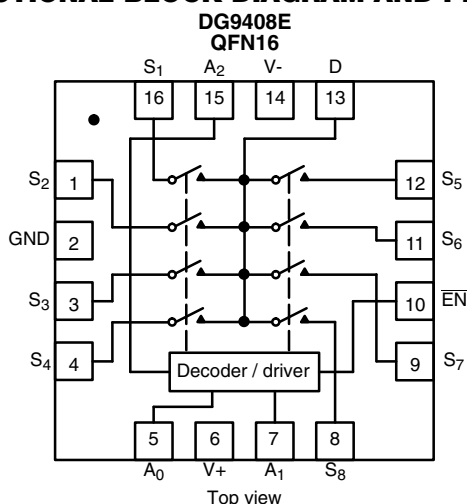
BENEFITS

- Fast switching speed
- Low switch resistance
- Wide operation voltage range
- Simple logic interface

APPLICATIONS

- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Battery powered systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Note

- QFN16 package central exposed pad has no electrical connection inside the chip. It can be connected GND, V+, V-, or left floating.



TRUTH TABLE AND ORDERING INFORMATION

TRUTH TABLE DG9408E				
A ₂	A ₁	A ₀	$\overline{\text{EN}}$	ON SWITCH
X	X	X	1	None
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

TRUTH TABLE DG9409E			
A ₁	A ₀	$\overline{\text{EN}}$	ON SWITCH
X	X	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

X = do not care

For low and high voltage levels for V_{AX} and V_{EN} consult “Digital Control” parameters for specific V+ operation. See specifications tables for:

Single supply 12 V

Dual supply V+ = 5 V, V- = -5 V

Single supply 5 V

Single supply 3 V

ORDERING INFORMATION			
TEMP. RANGE	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY
-40 °C to +85 °C	16-pin QFN (4 mm x 4 mm) (variation 1)	DG9408EDN-T1-GE4	Tape and reel, 2500 units
		DG9409EDN-T1-GE4	Tape and reel, 2500 units

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
PARAMETER		LIMIT	UNIT
Voltage referenced V+ to V-		-0.3 to +18	V
GND to V-		18	
Digital inputs ^a , V _S , V _D		(V-) - 0.3 to (V+) + 0.3	
Current (any terminal except S or D)		30	mA
Continuous current, S or D		100	
Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		200	
Package solder reflow conditions (lead (Pb)-free assembly) ^d	16-pin (4 x 4 mm) QFN	260 +0 / -5	°C
Storage temperature		-65 to +150	
Power dissipation (package) ^b , (T _A = 70 °C)	16-pin (4 x 4 mm) QFN ^c	1880	mW
ESD human body model (HBM), per ANSI / ESDA / JEDEC® JS-001		2500	V
Latch up current, per JESD78		400	mA

Notes

- Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered or welded to PC board.
- Derate 23.5 mW/°C above 70 °C.
- Manual soldering with soldering iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SPECIFICATIONS (Single Supply 12 V)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, ± 10 %, V- = 0 V VA, VEN = 0.8 V or 2.4 V ^f		TEMP. ^b	LIMITS -40 °C to +85 °C			UNIT
					MIN. ^c	TYP. ^d	MAX. ^c	
Analog Switch								
Analog signal range ^e	VANALOG			Full	0	-	12	V
On-resistance	RON	V+ = 10.8 V, VD = 2 V or 9 V, IS = 50 mA sequence each switch on		Room	-	3.2	7	Ω
				Full	-		7.5	
RON match between channels ^g	ΔRON	V+ = 10.8 V, VD = 2 V or 9 V, IS = 50 mA		Room	-	-	3.6	
On-resistance flatness ⁱ	RON flatness			Room	-	-	8	
Switch off leakage current	IS(off)	VEN = 2.4 V, VD = 11 V or 1 V, VS = 1 V or 11 V		Room	-2	-	2	nA
	ID(off)			Full	-15	-	15	
				Room	-2	-	2	
				Full	-15	-	15	
Channel on leakage current	ID(on)	VEN = 0 V, VS = VD = 1 V or 11 V		Room	-2	-	2	
				Full	-15	-	15	
Digital Control								
Logic high input voltage	VINH			Full	2.4	-	-	V
Logic low input voltage	VINL			Full	-	-	0.8	
Input current	IIN	VAX = VEN = 2.4 V or 0.8 V		Full	-1	-	1	μA
Dynamic Characteristics								
Transition time	tTRANS	VS1 = 8 V, VS8 = 0 V, (DG9408E) VS1b = 8 V, VS4b = 0 V, (DG9409E) see fig. 2		Room	-	40	71	ns
				Full	-	-	75	
Break-before-make time	tBBM	VS(all) = VDA = 5 V see fig. 4		Room	2	20	-	
				Full	-	-	-	
Enable turn-on time	tON(EN)	VAX = 0 V, VS1 = 5 V (DG9408E) VAX = 0 V, VS1b = 5 V (DG9409E) see fig. 3		Room	-	36	70	
				Full	-	-	75	
Enable turn-off time	tOFF(EN)			Room	-	24	44	
				Full	-	-	46	
Charge injection ^e	Q	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω		Room	-	4.5	-	pC
Off isolation ^{e, h}	OIRR	f = 100 kHz, RL = 1 kΩ		Room	-	-83	-	dB
Crosstalk ^e	XTALK			Room	-	-89	-	
Source off capacitance ^e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 2.4 V	DG9408E	Room	-	17	-	pF
			DG9409E	Room	-	16	-	
Drain off capacitance ^e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 2.4 V	DG9408E	Room	-	134	-	
			DG9409E	Room	-	67	-	
Drain on capacitance ^e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 0 V	DG9408E	Room	-	154	-	
			DG9409E	Room	-	86	-	
Power Supplies								
Power supply current	I+	VEN = VA = 0 V or V+		Room	-	-	1	μA



SPECIFICATIONS (Dual Supply V ₊ = 5 V, V ₋ = -5 V)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V ₊ = 5 V, V ₋ = -5 V, ± 10 % V _A , V _{EN} = 0.8 V or 2 V ^f		TEMP. ^b	LIMITS -40 °C to +85 °C			UNIT
					MIN. ^c	TYP. ^d	MAX. ^c	
Analog Switch								
Analog signal range ^e	V _{ANALOG}			Full	-5	-	5	V
On-Resistance	R _{ON}	V ₊ = 4.5 V, V ₋ = -4.5 V, V _D = ± 3.5 V, I _S = 50 mA sequence each switch on		Room	-	4	8	Ω
				Full	-	-	8.5	
R _{ON} match between channels ^g	ΔR _{ON}			Room	-	-	3.6	
On-resistance flatness ⁱ	R _{ON} Flatness	V ₊ = 4.5 V, V ₋ = -4.5 V, V _D = ± 3.5 V, I _S = 50 mA		Room	-	-	8.2	
Switch off leakage current ^a	I _{S(off)}	V ₊ = 5.5, V ₋ = -5.5 V V _{EN} = 2.4 V, V _D = ± 4.5 V, V _S = ± 4.5 V		Room	-2	-	2	nA
				Full	-15	-	15	
	I _{D(off)}			Room	-2	-	2	
				Full	-15	-	15	
Channel on leakage current ^a	I _{D(on)}	V ₊ = 5.5 V, V ₋ = -5.5 V V _{EN} = 0 V, V _D = ± 4.5 V, V _S = ± 4.5 V		Room	-2	-	2	
				Full	-15	-	15	
Digital Control								
Logic high input voltage	V _{INH}			Full	2	-	-	V
Logic low input voltage	V _{INL}			Full	-	-	0.8	
Input current ^a	I _{IN}	V _{AX} = V _{EN} = 2 V or 0.8 V		Full	-1	-	1	μA
Dynamic Characteristics								
Transition time ^e	t _{TRANS}	V _{S1} = 3.5 V, V _{S8} = -3.5 V, (DG9408E) V _{S1b} = 3.5 V, V _{S4b} = -3.5 V, (DG9409E) see fig. 2		Room	-	47	65	ns
				Full	-	-	70	
Break-before-make time ^e	t _{BBM}	V _{S(all)} = V _{DA} = 3.5 V see fig. 4		Room	1	13	-	
				Full	-	-	-	
Enable turn-on time ^e	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 3.5 V (DG9408E) V _{AX} = 0 V, V _{S1b} = 3.5 V (DG9409E) see fig. 3		Room	-	54	70	
				Full	-	-	76	
Enable turn-off time ^e	t _{OFF(EN)}			Room	-	28	40	
				Full	-	-	43	
Source off capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 2 V	DG9408E	Room	-	15	-	pF
			DG9409E	Room	-	14	-	
Drain off capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 0 V, V _{EN} = 2 V	DG9408E	Room	-	126	-	
			DG9409E	Room	-	63	-	
Drain on capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 0 V	DG9408E	Room	-	153	-	
			DG9409E	Room	-	89	-	
Power Supplies								
Power supply current	I ₊	V _{EN} = V _A = 0 V or V ₊		Room	-	-	1	μA
	I ₋			Room	-1	-	-	



SPECIFICATIONS (Single Supply 5 V)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 %, V- = 0 V V _A , V _{EN} = 0.8 V or 2 V ^f		TEMP. ^b	LIMITS -40 °C to +85 °C			UNIT
					MIN. ^c	TYP. ^d	MAX. ^c	
Analog Switch								
Analog signal range ^e	V _{ANALOG}			Full	0	-	5	V
On-resistance	R _{ON}	V+ = 4.5 V, V _D or V _S = 1 V or 3.5 V, I _S = 50 mA		Room	-	6.8	10.5	Ω
				Full	-	-	11	
R _{ON} match between channels ^g	ΔR _{ON}	V+ = 4.5 V, V _D = 1 V or 3.5 V, I _S = 50 mA		Room	-	-	3.6	
On-resistance flatness ⁱ	R _{ON} Flatness			Room	-	-	9	
Switch off leakage current ^a	I _{S(off)}	V+ = 5.5 V V _S = 1 V or 4 V, V _D = 4 V or 1 V		Room	-2	-	2	nA
	I _{D(off)}			Full	-15	-	15	
				Room	-2	-	2	
				Full	-15	-	15	
Channel on leakage current ^a	I _{D(on)}	V+ = 5.5 V V _D = V _S = 1 V or 4 V, sequence each switch on		Room	-2	-	2	
				Full	-15	-	15	
Digital Control								
Logic high input voltage	V _{INH}	V+ = 5 V		Full	2	-	-	V
Logic low input voltage	V _{INL}			Full	-	-	0.8	
Input current ^a	I _{IN}	V _{AX} = V _{EN} = 2 V or 0.8 V		Full	-1	-	1	μA
Dynamic Characteristics								
Transition time ^e	t _{TRANS}	V _{S1} = 3.5 V, V _{S8} = 0 V, (DG9408E) V _{S1b} = 3.5 V, V _{S4b} = 0 V, (DG9409E) see fig. 2		Room	-	79	97	ns
				Full	-	-	112	
Break-before-make time ^e	t _{OPEN}	V _{S(all)} = V _{DA} = 3.5 V see fig. 4		Room	2	35	-	
				Full	-	-	-	
Enable turn-on time ^e	t _{ON(EN)}	V _{AX} = 0 V, V _{S1} = 3.5 V (DG9408E) V _{AX} = 0 V, V _{S1b} = 3.5 V (DG9409E) see fig. 3		Room	-	83	95	
				Full	-	-	116	
Enable turn-off time ^e	t _{OFF(EN)}			Room	-	36	57	
				Full	-	-	61	
Charge injection ^e	Q	C _L = 1 nF, R _{GEN} = 0, V _{GEN} = 0 V		Room	-	3.7	-	pC
Off isolation ^{e, h}	OIRR	R _L = 1 kΩ, f = 100 kHz		Room	-	-83	-	dB
Crosstalk ^e	X _{TALK}			Room	-	-90	-	
Source off capacitance ^e	C _{S(off)}	f = 1 MHz, V _S = 0 V, V _{EN} = 0 V	DG9408E	Room	-	19	-	pF
			DG9409E	Room	-	18	-	
Drain off capacitance ^e	C _{D(off)}	f = 1 MHz, V _D = 0 V, V _{EN} = 2 V	DG9408E	Room	-	149	-	
			DG9409E	Room	-	74	-	
Drain on capacitance ^e	C _{D(on)}	f = 1 MHz, V _D = 0 V, V _{EN} = 0 V	DG9408E	Room	-	170	-	
			DG9409E	Room	-	94	-	
Power Supplies								
Power supply current	I+	V _{EN} = V _A = 0 V or V+		Room	-	-	1	μA



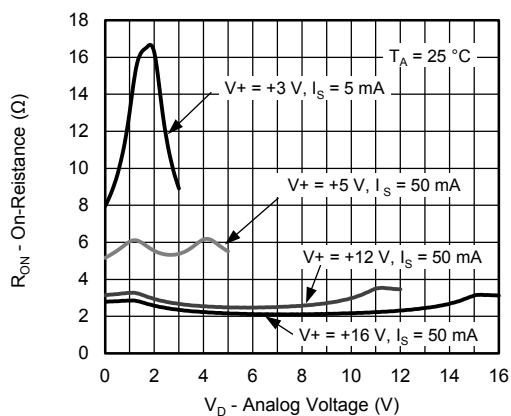
SPECIFICATIONS (Single Supply 3 V)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 %, V- = 0 V VEN = 0.4 V or 1.8 V f		TEMP. b	LIMITS -40 °C to +85 °C			UNIT
					MIN. c	TYP. d	MAX. c	
Analog Switch								
Analog signal range e	VANALOG			Full	0	-	3	V
On-resistance	RON	V+ = 2.7 V, VD = 0.5 V or 2.2 V, IS = 5 mA		Room	-	13	25.5	Ω
RON match between channels g	ΔRON	V+ = 2.7 V, VD = 0.5 V or 2.2 V, IS = 5 mA		Full	-	-	26.5	
On-resistance flatness i	RON Flatness			Room	-	-	13	
Switch off leakage current a	IS(off)	V+ = 3.3 V VS = 2 V or 1 V, VD = 1 or 2 V		Room	-2	-	2	nA
				Full	-15	-	15	
	ID(off)			Room	-2	-	2	
				Full	-15	-	15	
Channel on leakage current a	ID(on)	V+ = 3.3 V VD = VS = 1 V or 2 V, sequence each switch on		Room	-2	-	2	nA
				Full	-15	-	15	
Digital Control								
Logic high input voltage	VINH			Full	1.8	-	-	V
Logic low input voltage	VINL			Full	-	-	0.4	
Input current a	IIN	VAX = VEN = 1.8 V or 0.4 V		Full	-1	-	1	μA
Dynamic Characteristics								
Transition time	tTRANS	VS1 = 1.5 V, VS8 = 0 V, (DG9408E) VS1b = 1.5 V, VS4b = 0 V, (DG9409E) see fig. 2		Room	-	169	245	ns
				Full	-	-	278	
Break-before-make time	tBBM	VS(all) = VDA = 1.5 V see fig. 4		Room	2	96	-	
				Full	-	-	-	
Enable turn-on time	tON(EN)	VAX = 0 V, VS1 = 1.5 V (DG9408E) VAX = 0 V, VS1b = 1.5 V (DG9409E) see fig. 3		Room	-	202	255	
				Full	-	-	272	
Enable turn-off time	tOFF(EN)			Room	-	72	97	
				Full	-	-	104	
Charge injection e	Q	CL = 1 nF, RGEN = 0, VGEN = 0 V		Room	-	2.1	-	pC
Off isolation e, h	OIRR	f = 100 kHz, RL = 1 kΩ		Room	-	-83	-	dB
Crosstalk e	XTALK			Room	-	-90	-	
Source off capacitance e	CS(off)	f = 1 MHz, VS = 0 V, VEN = 1.8 V	DG9408E	Room	-	20	-	pF
			DG9409E	Room	-	19	-	
Drain off capacitance e	CD(off)	f = 1 MHz, VD = 0 V, VEN = 1.8 V	DG9408E	Room	-	159	-	
			DG9409E	Room	-	79	-	
Drain on capacitance e	CD(on)	f = 1 MHz, VD = 0 V, VEN = 0 V	DG9408E	Room	-	179	-	
			DG9409E	Room	-	98	-	
Power Supplies								
Power supply current	I+	VEN = VA = 0 V or V+		Room	-	-	1	μA

Notes

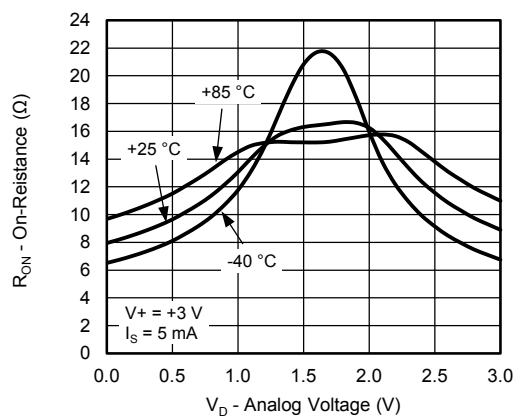
- a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- b. Room = 25 °C, full = as determined by the operating temperature suffix.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.
- g. $\Delta R_{\text{DON}} = R_{\text{DON max.}} - R_{\text{DON min.}}$
- h. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
- i. R_{DON} flatness is measured as the difference between the minimum and maximum measured values across a defined analog signal.



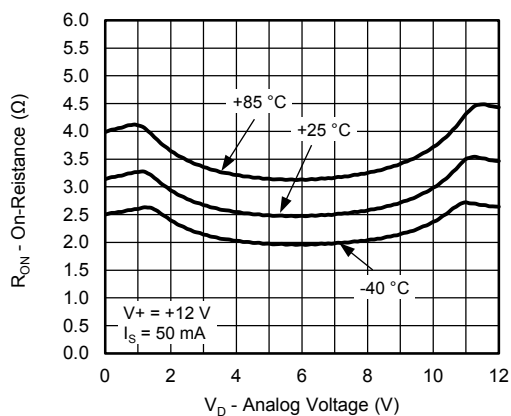
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



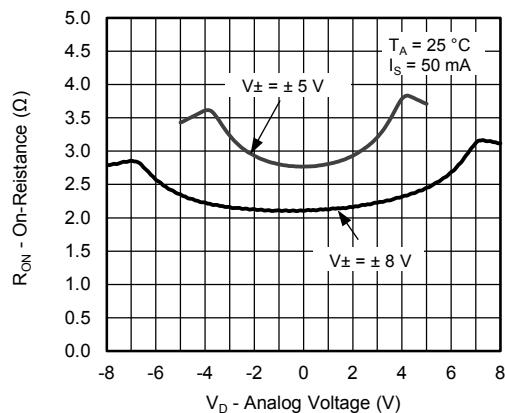
On-Resistance vs. Analog Voltage



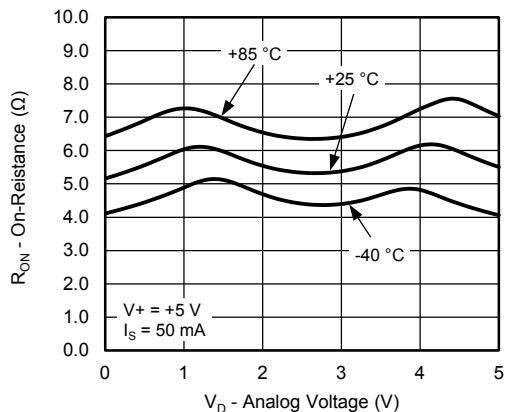
On-Resistance vs. Analog Voltage



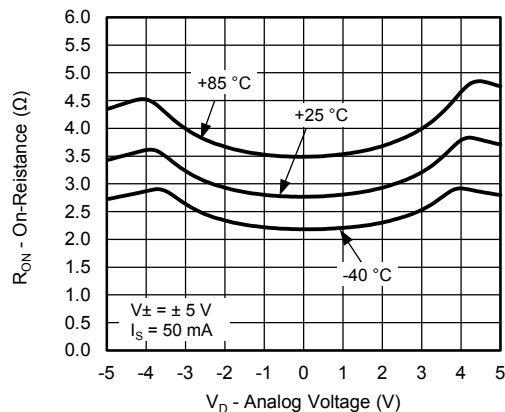
On-Resistance vs. Analog Voltage



On-Resistance vs. Analog Voltage



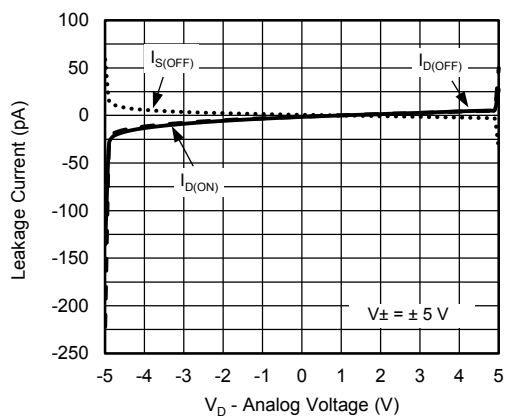
On-Resistance vs. Analog Voltage



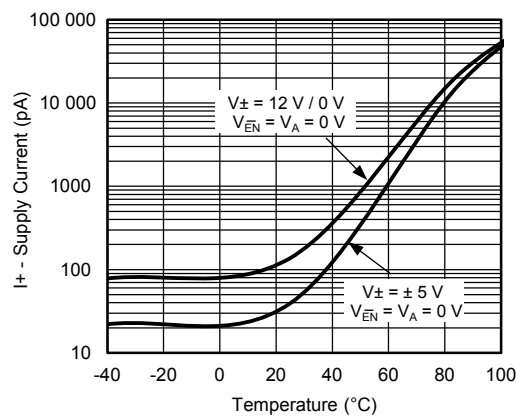
On-Resistance vs. Analog Voltage



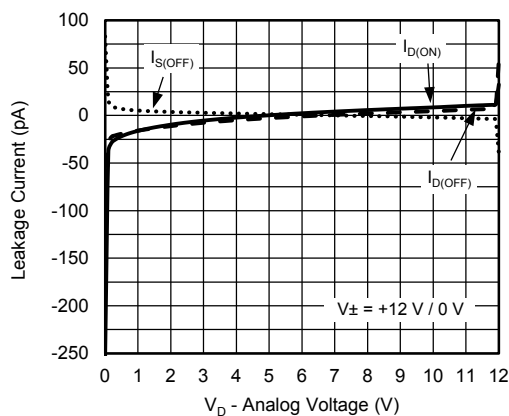
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



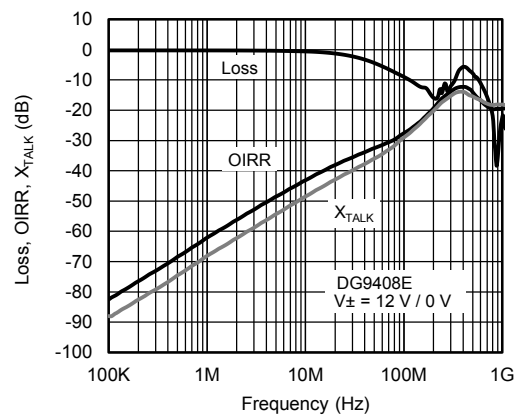
Leakage Current vs. Analog Voltage



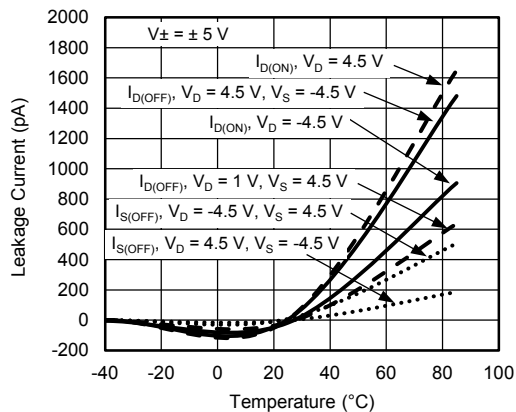
Supply Current vs. Temperature



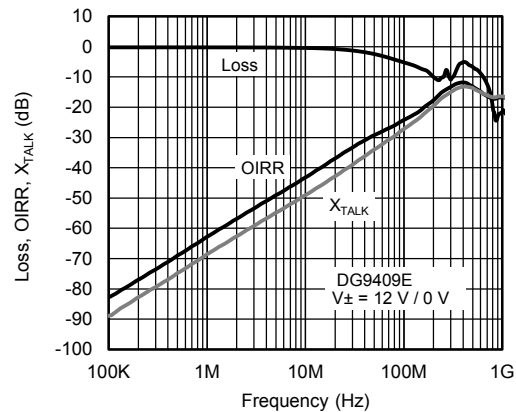
Leakage Current vs. Analog Voltage



Loss, OIRR, X_{TALK} vs. Frequency



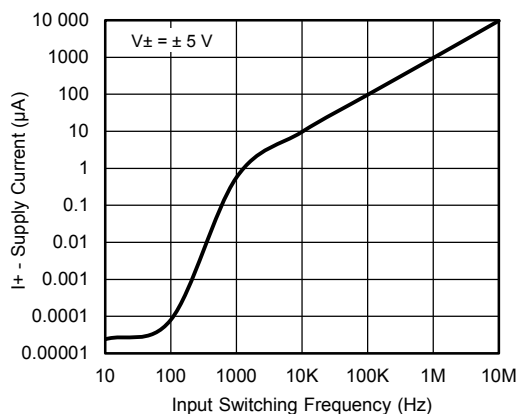
Leakage Current vs. Temperature



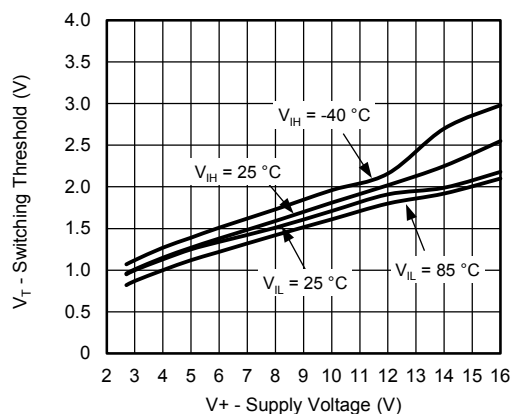
Loss, OIRR, X_{TALK} vs. Frequency



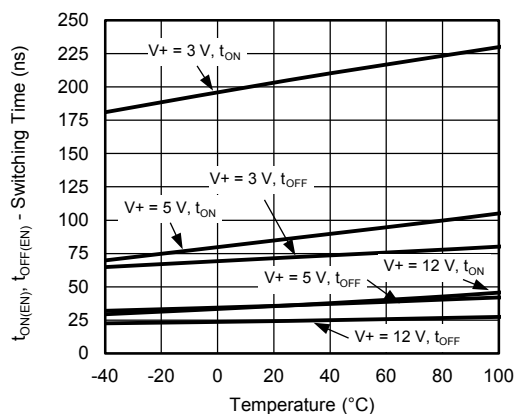
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



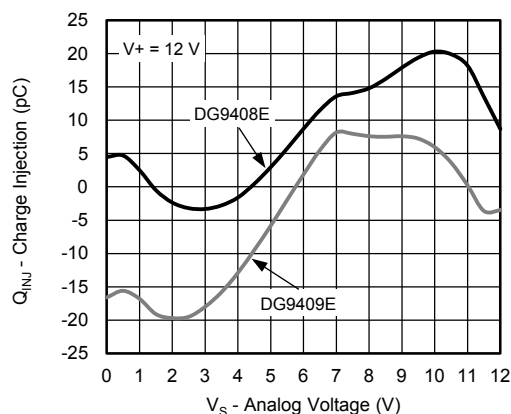
Supply Current vs. Input Switching Frequency



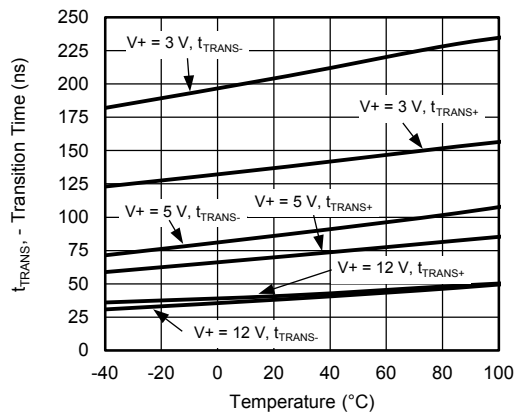
Switching Threshold vs. Supply Voltage



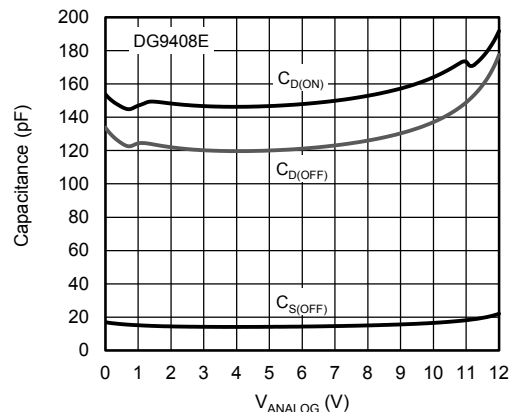
Switching Time vs. Temperature



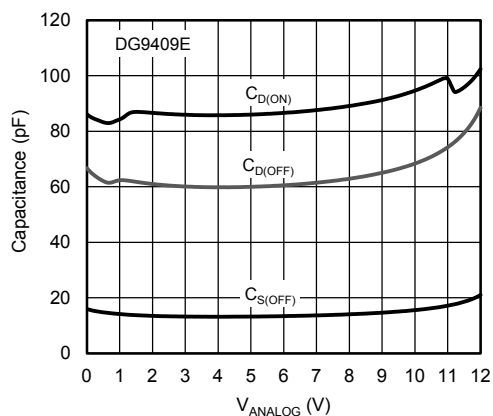
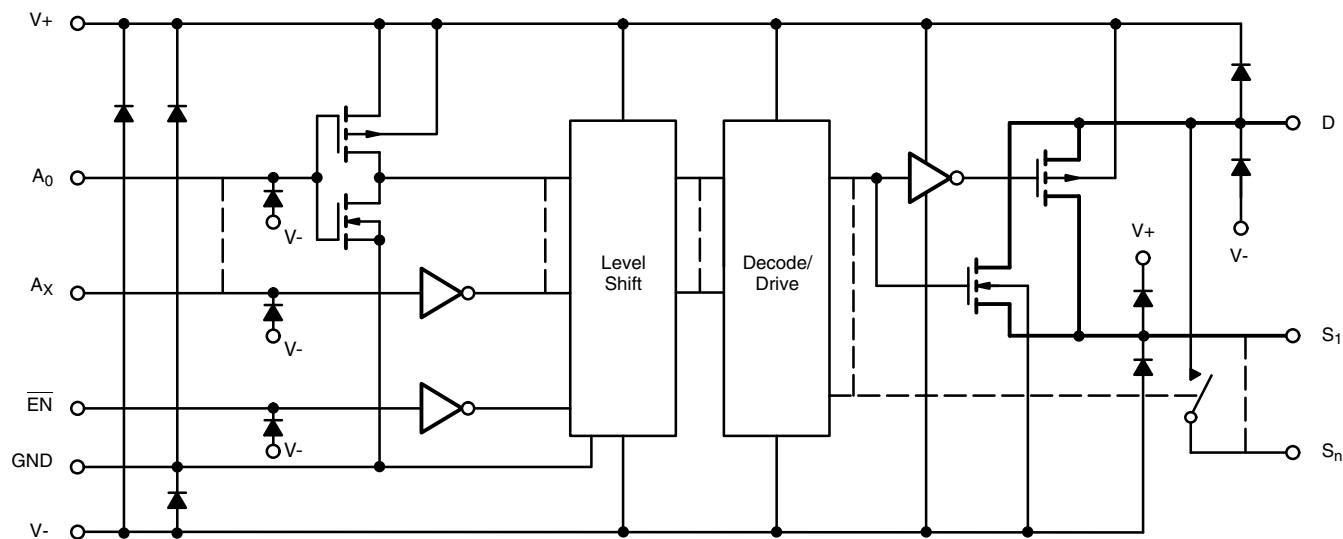
Charge Injection vs. Analog Voltage

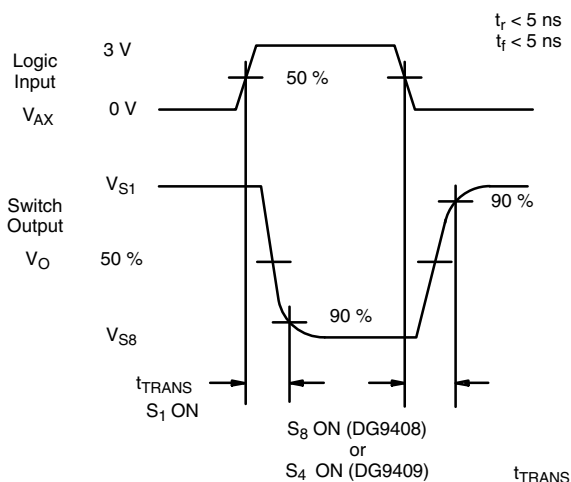
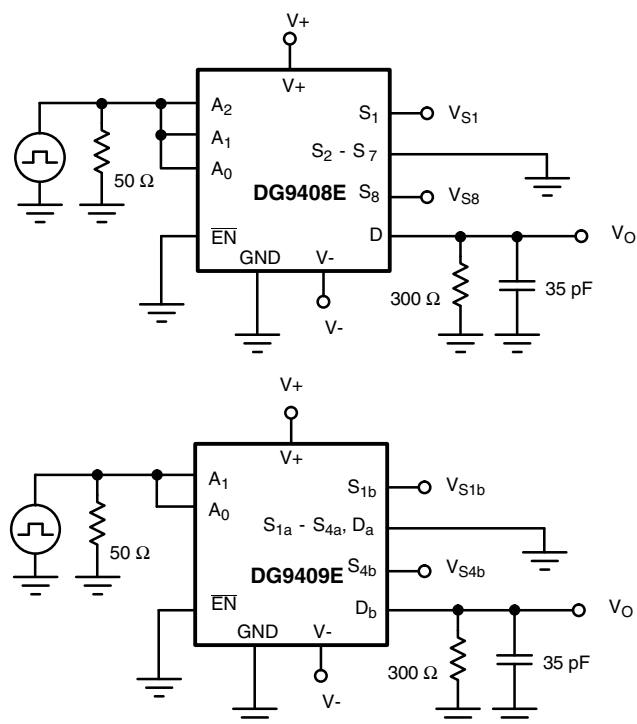


Transition Time vs. Temperature

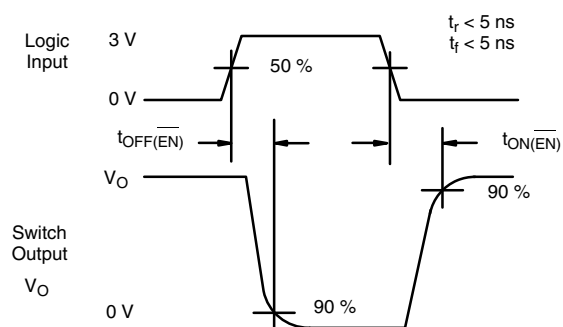
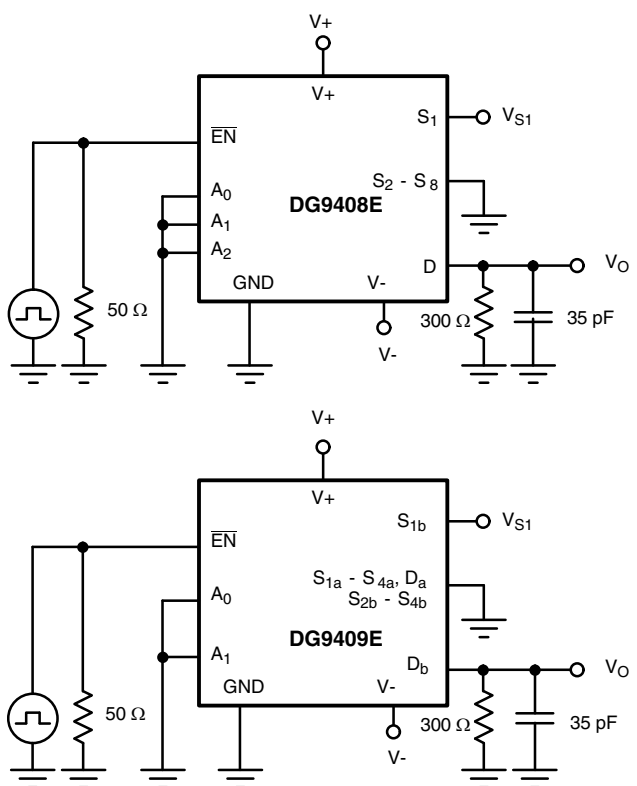


Capacitance vs. Analog Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Capacitance vs. Analog Voltage
SCHEMATIC DIAGRAM (Typical Channel)

Fig. 1 -

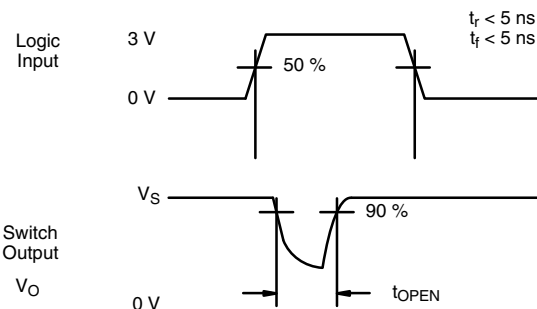
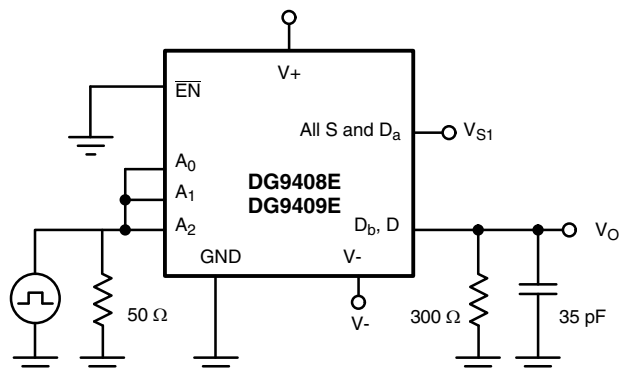
TEST CIRCUITS


Return to Specifications:
 Single Supply 12 V
 Dual Supply V₊ = 5 V, V₋ = -5 V
 Single Supply 5 V
 Single Supply 3 V

Fig. 2 - Transition Time


Return to Specifications:
 Single Supply 12 V
 Dual Supply V₊ = 5 V, V₋ = -5 V
 Single Supply 5 V
 Single Supply 3 V

Fig. 3 - Enable Switching Time

TEST CIRCUITS


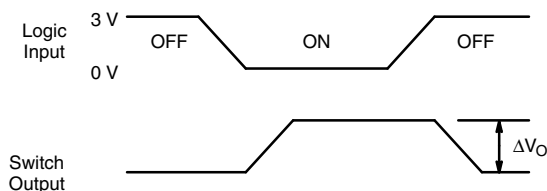
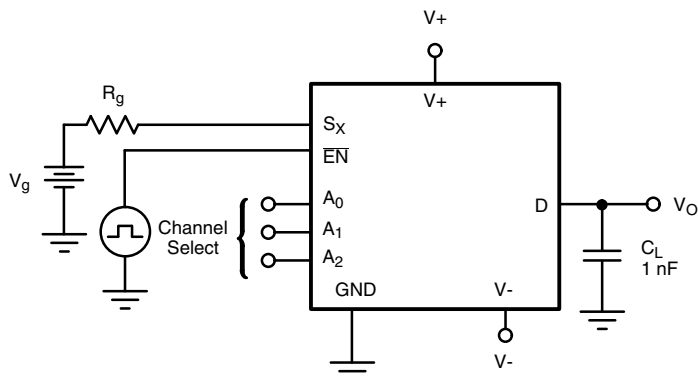
Return to Specifications:

Single Supply 12 V

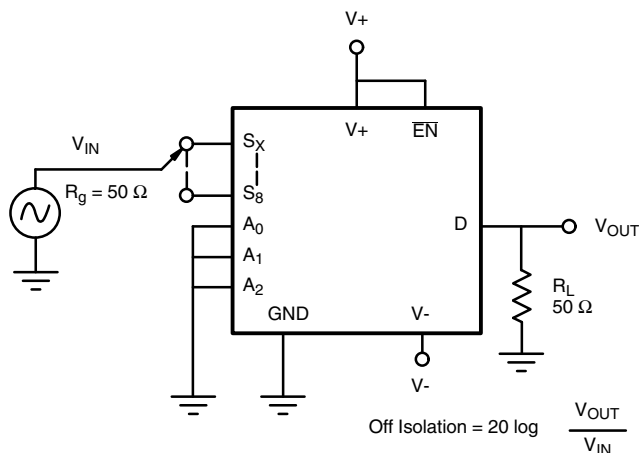
Dual Supply $V_+ = 5\text{ V}$, $V_- = -5\text{ V}$

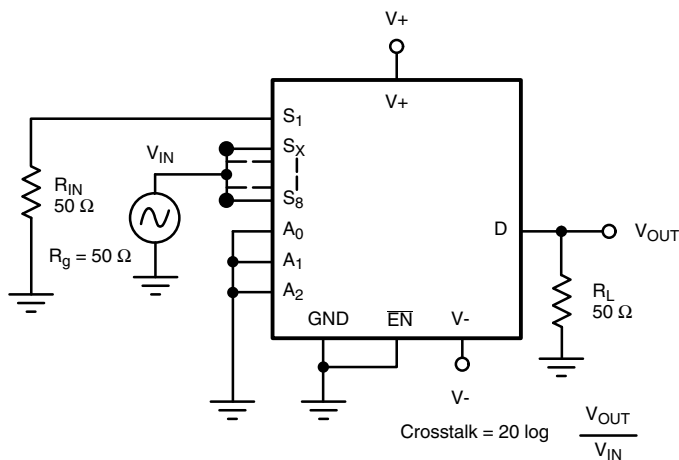
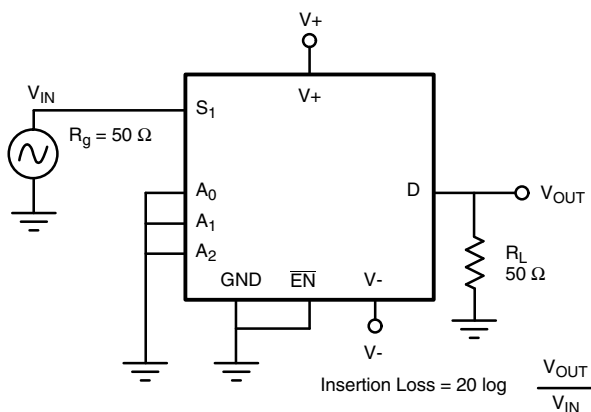
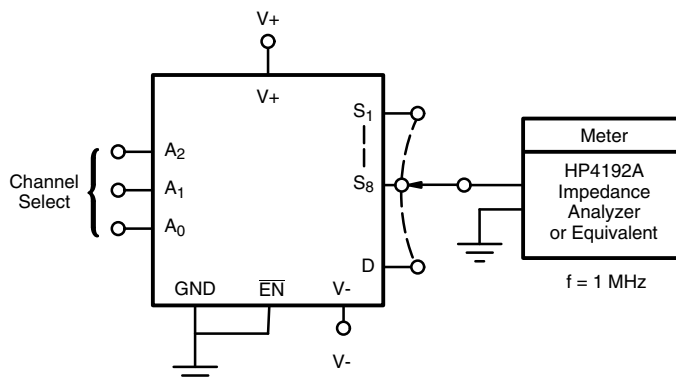
Single Supply 5 V

Single Supply 3 V

Fig. 4 - Break-Before-Make Interval

 ΔV_O is the measured voltage due to charge transfer error Q , when the channel turns off.

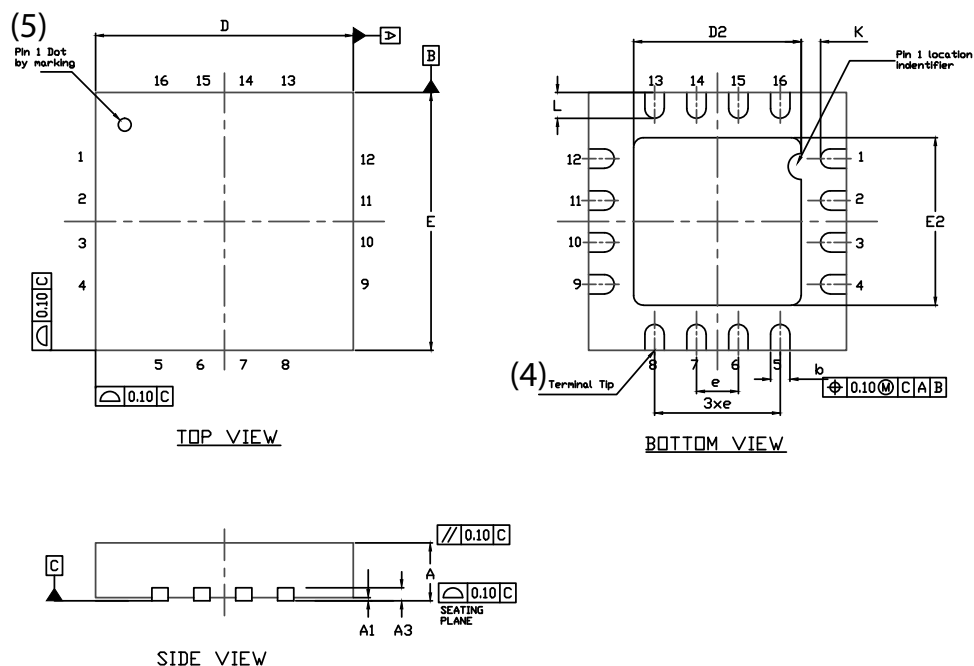
$$Q = C_L \times \Delta V_O$$

Fig. 5 - Charge Injection

Fig. 6 - Off Isolation

TEST CIRCUITS

Fig. 7 - Crosstalk

Fig. 8 - Insertion Loss

Fig. 9 - Source Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75375.

QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS ⁽¹⁾			INCHES			MILLIMETERS ⁽¹⁾			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N ⁽³⁾	16			16			16			16		
Nd ⁽³⁾	4			4			4			4		
Ne ⁽³⁾	4			4			4			4		

Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

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DWG: 5890



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