

### 5GHz Band SPDT Switch + LNA GaAs MMIC

#### **■** GENERAL DESCRIPTION

The NJG1739K51 is a 5GHz band SPDT switch + low noise amplifier GaAs MMIC designed for wireless LAN front-end applications.

The NJG1739K51 features low current consumption, low insertion loss of transmit path and low noise figure of RX LNA mode.

The NJG1739K51 has ESD protection devices to achieve excellent ESD performances.

A small and ultra-thin package of QFN12-51 is adopted.

# NJG1739K51

**■ PACKAGE OUTLINE** 

#### **■** APPLICATIONS

5GHz Band WLAN front-end application

#### **■ FEATURES**

● Operating voltage V<sub>DD</sub>=3.6V typ.

Operating frequency freq=4900 to 5900MHz

#### [RX LNA mode]

● Operating current 8mA typ. @V<sub>DD</sub>=3.6V, V<sub>CTL</sub>1=V<sub>CTL</sub>3=3.3V, V<sub>CTL</sub>2=0V

Small signal gain
Noise figure
Input power 1dB compression
12.0dB typ.
2.5dB typ.
0dBm typ.

#### [RX Bypass mode]

● Operating current
4µA typ. @V<sub>DD</sub>=3.6V, V<sub>CTL</sub>1=3.3V, V<sub>CTL</sub>2=V<sub>CTL</sub>3=0V

Insertion loss
Input power 1dB compression
\*15dBm typ.

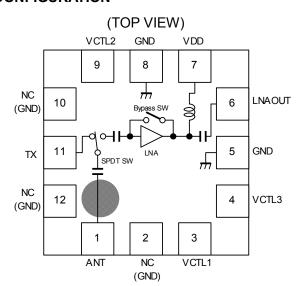
#### [TX mode]

Insertion loss
 Input power 0.1dB compression
 0.5dB typ.
 +29dBm typ.

◆ Package
QFN12-51 (Package size: 2.0mm x 2.0mm x 0.375mm typ.)

RoHS compliant and Halogen Free, MSL1

#### **■ PIN CONFIGURATION**



1: ANT 7. VDD 2: NC(GND) 8. GND 3: VCTL1 9. VCTL2 4: VCTL3 10. NC(GND) 5: GND 11. TX 6: LNAOUT 12: NC(GND)

Exposed pad: GND

Note: Specifications and description listed in this datasheet are subject to change without notice.

#### **■** TRUTH TABLE

"H"=V<sub>CTL</sub>(H), "L"=V<sub>CTL</sub>(L)

mode	VCTL1 VCTL2		VCTL3	STATE				
mode	(SW RX)	(SW TX)	(LNA)	IDD	LNA	Bypass	RX SW	TX SW
RX LNA	Н	L	Н	I <sub>DD</sub> 1	ON	OFF	ON	OFF
RX Bypass	Н	L	L	I <sub>DD</sub> 2	OFF	ON	ON	OFF
TX	L	Н	L	I <sub>DD</sub> 2	OFF	ON	OFF	ON
Sleep	L	L	L	I <sub>DD</sub> 3	OFF	OFF	OFF	OFF

#### ■ ABSOLUTE MAXIMUM RATINGS

T<sub>a</sub>=+25°C

				a-120 C
PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	$V_{DD}$		5.5	V
Control voltage	V <sub>CTL</sub>		5.5	V
Input power 1	P <sub>IN1</sub>	ANT terminal, $V_{DD}$ =3.6V, $V_{CTL}$ 1= $V_{CTL}$ 3=3.3V, $V_{CTL}$ 2=0V	+15	dBm
Input power 2	P <sub>IN2</sub>	TX terminal, $V_{DD}$ =3.6V, $V_{CTL}$ 1= $V_{CTL}$ 3=0V, $V_{CTL}$ 2=3.3V	+25	dBm
Power dissipation	P <sub>D</sub>	Four-layer FR4 PCB with through-hole (101.5x114.5mm), T <sub>i</sub> =150°C	1190	mW
Operation temperature	$T_{opr}$		-40 to +85	°C
Storage temperature T <sub>stg</sub>			-55 to +150	°C

#### ■ ELECTRICAL CHARACTERISTICS 1 (DC Characteristics)

		$V_{DD}$ =3.6V, $V_{CTL}(H)$ =3.3V, $V_{CTL}(L)$ =0V, $T_a$ =+25°C, $Z_s$ = $Z_l$ =500				
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	$V_{DD}$		3.0	3.6	5.0	V
Control voltage 1(High)	V <sub>CTL</sub> 1(H)		2.8	3.3	5.0	V
Control voltage 2(High)	V <sub>CTL</sub> 2(H)		2.8	3.3	5.0	V
Control voltage 3(High)	V <sub>CTL</sub> 3(H)		2.8	3.3	5.0	V
Control voltage 1(Low)	V <sub>CTL</sub> 1(L)		0.0	-	0.4	V
Control voltage 2(Low)	V <sub>CTL</sub> 2(L)		0.0	-	0.4	V
Control voltage 3(Low)	V <sub>CTL</sub> 3(L)		0.0	-	0.4	V
LNA operating current 1 (RX LNA mode)	I <sub>DD</sub> 1	RF OFF, V <sub>CTL</sub> 1=V <sub>CTL</sub> 3=3.3V, V <sub>CTL</sub> 2=0V	-	8	13	mA
LNA operating current 2 (RX Bypass mode)	I <sub>DD</sub> 2	RF OFF, V <sub>CTL</sub> 1=3.3V, V <sub>CTL</sub> 2=V <sub>CTL</sub> 3=0V	-	4	12	μΑ
LNA operating current 3 (Sleep mode)	I <sub>DD</sub> 3	RF OFF, V <sub>CTL</sub> 1=V <sub>CTL</sub> 2=V <sub>CTL</sub> 3=0.4V	-	4	12	μΑ
LNA operating current 4 (VCTL OPEN)	I <sub>DD</sub> 4	RF OFF, V <sub>CTL</sub> 1=V <sub>CTL</sub> 2=V <sub>CTL</sub> 3=open	1	4	12	μΑ
Control current 1	I <sub>CTL</sub> 1	RF OFF, V <sub>CTL</sub> 1=3.3V, V <sub>CTL</sub> 2=V <sub>CTL</sub> 3=0V	-	5	20	μΑ
Control current 2	I <sub>CTL</sub> 2	RF OFF, V <sub>CTL</sub> 2=3.3V, V <sub>CTL</sub> 1=V <sub>CTL</sub> 3=0V	-	5	20	μΑ
Control current 3	I <sub>CTL</sub> 3	RF OFF, V <sub>CTL</sub> 3=3.3V, V <sub>CTL</sub> 1=V <sub>CTL</sub> 2=0V	-	5	20	μΑ

#### ■ ELECTRICAL CHARACTERISTICS 2 (RF Characteristics: RX LNA mode, LNA+SPDT SW)

 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=3.3V,  $V_{CTL}$ 2=0V, freq=4900 to 5900MHz,

 $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit

$r_a = r_2 = 0$ , $c_s = c_1 = 0$ , $c_s = c_1 = 0$ , with application circ					orr circuit	
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 1	Gain1	Exclude PCB and connector losses*1	9.0	12.0	14.0	dB
Gain flatness 1	Gflat1	f=4900 to 4980MHz, f=5400 to 5480MHz, f=5820 to 5900MHz	-	-	0.3	dB
Isolation 1	ISL1		-	30	-	dB
Noise figure 1	NF1	Exclude PCB and connector losses*2	-	2.5	3.0	dB
Input power at 1dB compression 1	P <sub>-1dB(IN)</sub> 1		-	0	-	dBm
Input 3rd order Intercept point 1	IIP3_1	f1=freq, f2=freq+100kHz, P <sub>IN</sub> =-18dBm	-	+9	-	dBm
Outband input 3rd order Intercept point 1	IIP3_OB1	f1=2450MHz, f2=f1+100kHz, P <sub>IN</sub> =-18dBm	-	+2	-	dBm
ANT port return loss 1	RLi1		-	8.0	-	dB
LNAOUT port return loss 1	RLo1		-	9.0	-	dB
LNA switching time	Tsw1_1	10% V <sub>CTL</sub> to 90% RF	-	250	400	ns
Other switching time	Tsw2_1	10% V <sub>CTL</sub> to 90% RF	-	200	500	ns

<sup>\*1) 0.64</sup>dB(4900MHz), 0.71dB(5400MHz), 0.79dB(5900MHz)

#### ■ ELECTRICAL CHARACTERISTICS 3 (RF Characteristics: RX Bypass mode, Bypass SW+SPDT SW) $V_{DD}$ =3.6V, $V_{CTL}$ 1=3.3V, $V_{CTL}$ 2= $V_{CTL}$ 3=0V, freq=4900 to 5900MHz,

 $T_a=+25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ , with application circuit

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PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 2	LOSS2	Exclude PCB and connector losses*3	6.0	8.5	10.5	dB
Input power at 1dB compression 2	P <sub>-1dB(IN)</sub> 2		-	+15	-	dBm
Input 3rd order Intercept point 2	IIP3_2	f1=freq, f2=freq+100kHz, P <sub>IN</sub> =-10dBm	-	+14	-	dBm
ANT port return loss 2	RLi2		-	7.0	1	dB
LNAOUT port return loss 2	RLo2		-	12.0	-	dB

<sup>\*3) 0.64</sup>dB(4900MHz), 0.71dB(5400MHz), 0.79dB(5900MHz)

<sup>\*2) 0.32</sup>dB(4900MHz), 0.35dB(5400MHz), 0.39dB(5900MHz)

#### ■ ELECTRICAL CHARACTERISTICS 4 (RF Characteristics: TX mode, SPDT SW)

 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=0V,  $V_{CTL}$ 2=3.3V, freq=4900 to 5900MHz,  $T_a$ =+25°C,  $Z_s$ = $Z_l$ =50 $\Omega$ , with application circuit

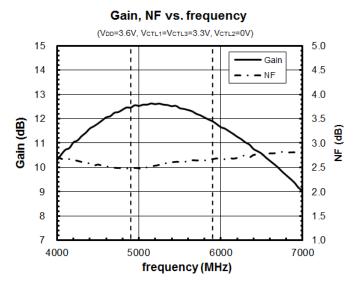
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 3	LOSS3	P <sub>IN</sub> =+23dBm, Exclude PCB and connector losses*4	1	0.5	0.8	dB
Input power at 0.1dB compression 3	P <sub>-0.1dB(IN)</sub> 3		1	+29	-	dBm
ANT port return loss 3	RLi3		1	16	-	dB
TX port return loss 3	RLo3		-	20	-	dB

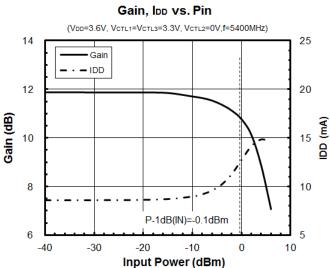
<sup>\*4) 0.65</sup>dB(4900MHz), 0.73dB(5400MHz), 0.81dB(5900MHz)

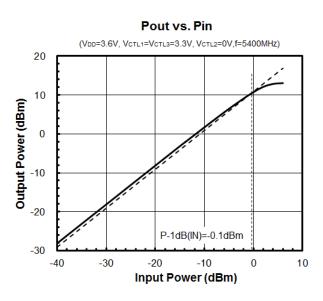
#### **■ TERMINAL INFORMATION**

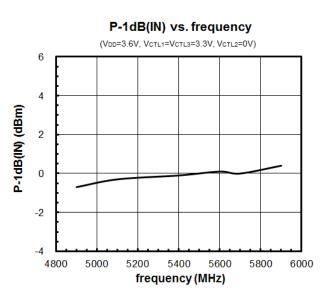
Pin No.	SYMBOL	DESCRIPTION			
1	ANT	RF transmitting/receiving terminal. No DC blocking capacitor is required for this port because of internal capacitor.			
2	NC(GND)	lo connected terminal. This terminal is not connected with internal circuit. Pleas onnect to the PCB ground plane.			
3	VCTL1	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).			
4	VCTL3	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).			
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.			
6	LNAOUT	RF receiving signal output terminal. No DC blocking capacitor is required for this port because of internal output matching circuit including DC blocking capacitor.			
7	VDD	Positive voltage supply terminal. The positive voltage (+3.0 to +5.0V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.			
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.			
9	VCTL2	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).			
10	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.			
11	TX	RF transmitting signal input terminal. DC blocking capacitor is required for this port.			
12	NC(GND)	No connected terminal. This terminal is not connected with internal circuit. Please connect to the PCB ground plane.			
Exposed Pad	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance, and through holes for GND should be placed near by the pin connection			

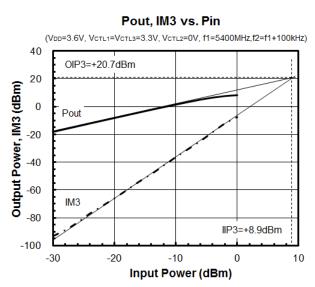
 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=3.3V,  $V_{CTL}$ 2=0V,  $T_a$ =+25°C,  $Z_s$ = $Z_l$ =50 $\Omega$ 

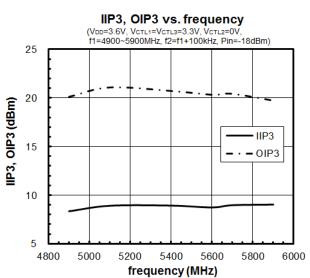




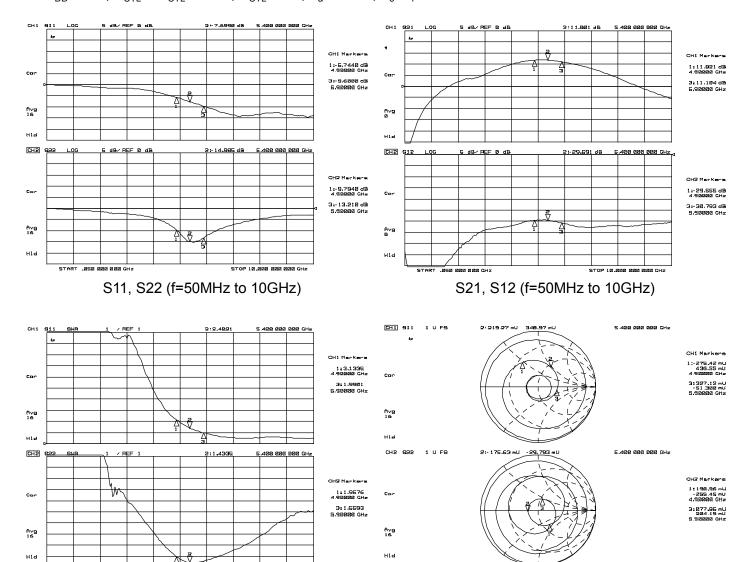








 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=3.3V,  $V_{CTL}$ 2=0V,  $T_a$ =+25°C,  $Z_s$ = $Z_i$ =50 $\Omega$ 

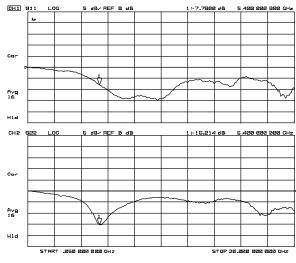


VSWRi, VSWRo (f=50MHz to 10GHz)

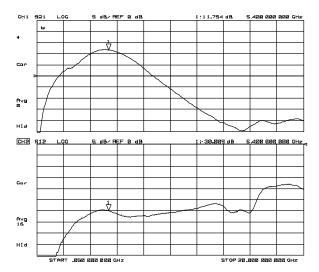
Zin, Zout (f=50MHz to 10GHz)

CENTER 5.025 000 000 CHz

 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=3.3V,  $V_{CTL}$ 2=0V,  $T_a$ =+25°C,  $Z_s$ = $Z_i$ =50 $\Omega$ 



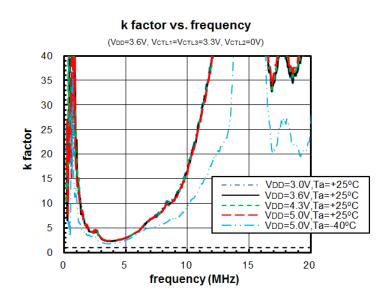
S11, S22 (f=50MHz to 20GHz)



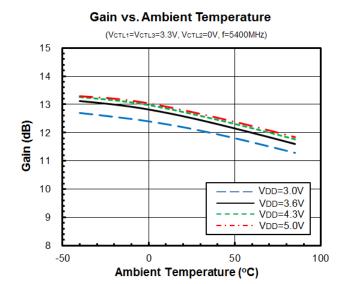
S21, S12 (f=50MHz to 20GHz)

#### **■ ELECTRICAL CHARACTERISTICS** (RX LNA mode)

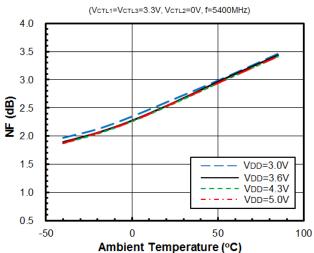
 $V_{CTL}1=V_{CTL}3=3.3V$ ,  $V_{CTL}2=0V$ ,  $Z_{s}=Z_{l}=50\Omega$ 



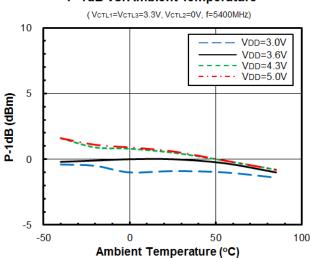
 $V_{CTL}1=V_{CTL}3=3.3V$ ,  $V_{CTL}2=0V$ ,  $Z_s=Z_l=50\Omega$ 



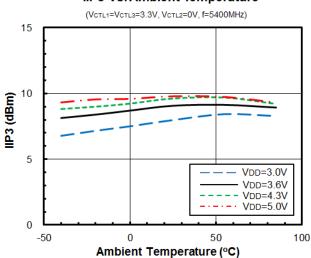
# NF vs. Ambient Temperature (Vctl=Vctl3=3.3V, Vctl2=0V, f=5400MHz)



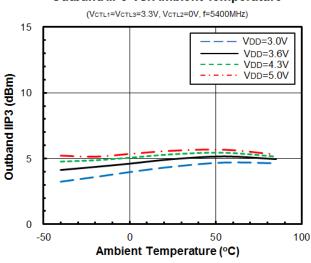
#### P-1dB vs. Ambient Temperature



#### IIP3 vs. Ambient Temperature

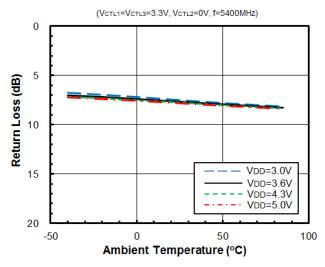


#### Outband IIP3 vs. Ambient Temperature

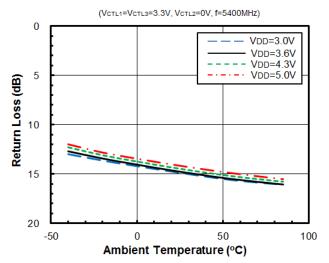


 $V_{CTL}1=V_{CTL}3=3.3V$ ,  $V_{CTL}2=0V$ ,  $Z_s=Z_l=50\Omega$ 

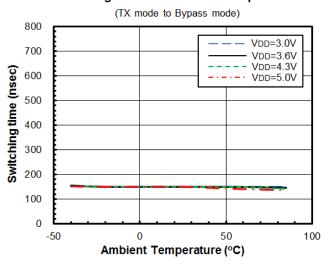
#### ANT Port Return Loss vs. Ambient Temperature



#### LNAOUT Port Return Loss vs. Ambient Temperature

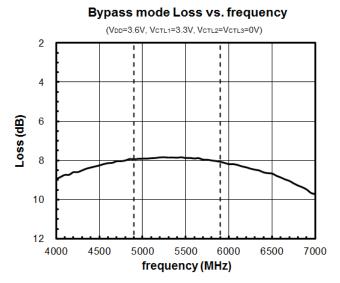


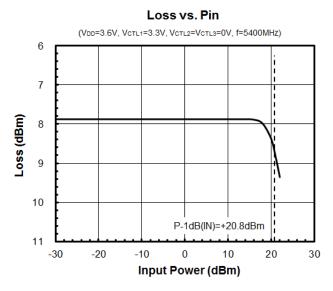
#### Switching Time vs. Ambient Temperature

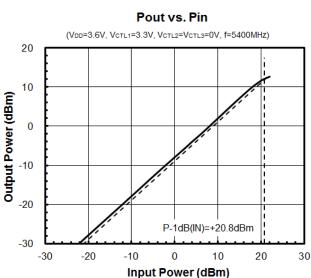


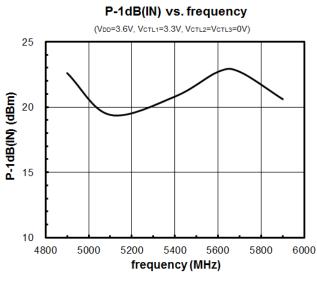
#### **■ ELECTRICAL CHARACTERISTICS** (RX Bypass mode)

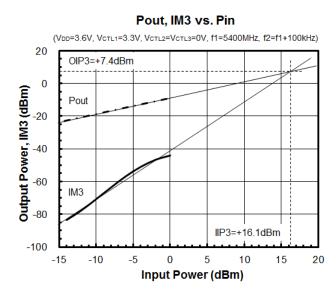
 $V_{DD}$ =3.6V,  $V_{CTL}$ 1=3.3V,  $V_{CTL}$ 2= $V_{CTL}$ 3=0V,  $T_a$ =+25°C,  $Z_s$ = $Z_i$ =50 $\Omega$ 

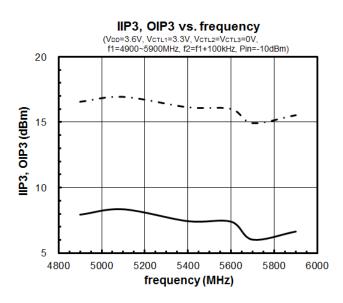






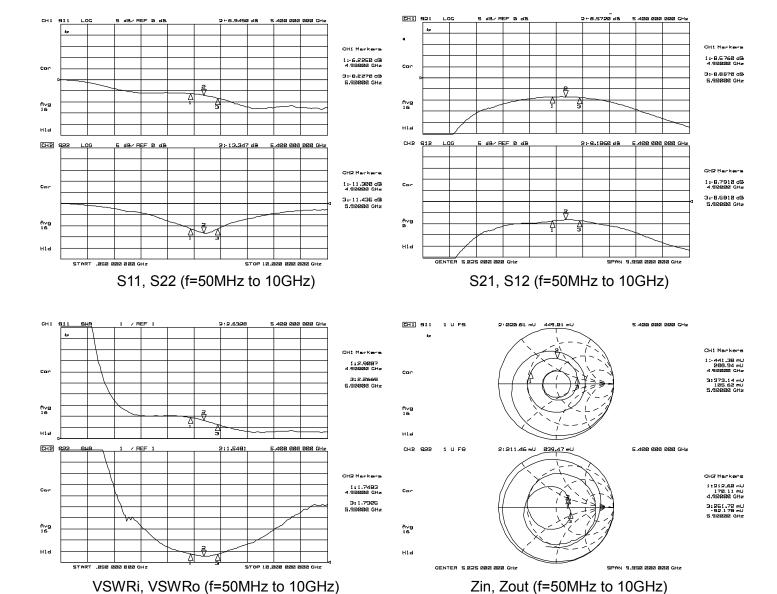






#### **■ ELECTRICAL CHARACTERISTICS** (RX Bypass mode)

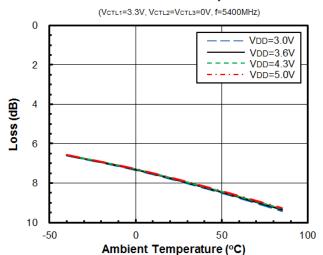
 $V_{DD}$ =3.6V,  $V_{CTL}$ 1=3.3V,  $V_{CTL}$ 2= $V_{CTL}$ 3=0V,  $T_a$ =+25°C,  $Z_s$ = $Z_i$ =50 $\Omega$ 



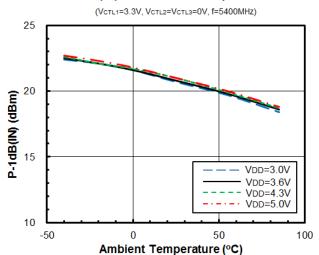
#### **■ ELECTRICAL CHARACTERISTICS** (RX Bypass mode)

 $V_{CTL}$ 1=3.3V,  $V_{CTL}$ 2= $V_{CTL}$ 3=0V,  $Z_s$ = $Z_l$ =50 $\Omega$ 

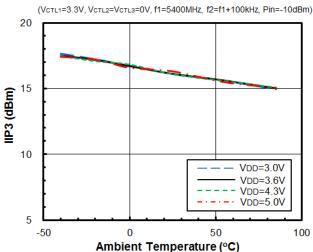
#### Loss vs. Ambient Temperature

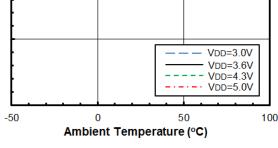


#### P-1dB(IN) vs. Ambient Temperature

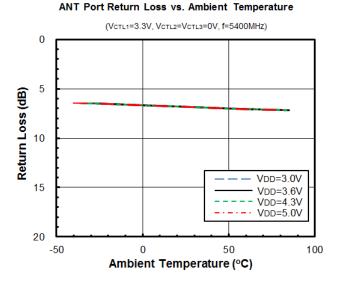


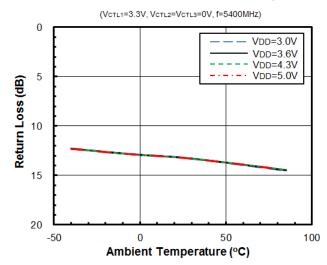
#### IIP3 vs. Ambient Temperature



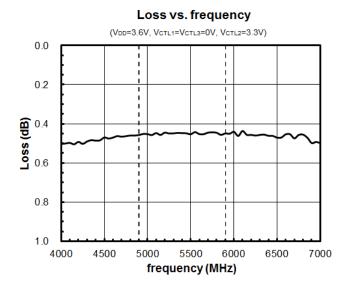


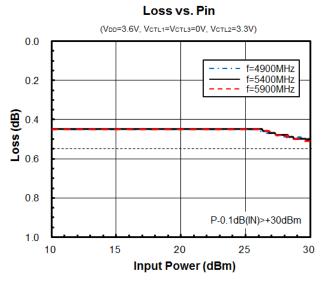
#### LNAOUT Port Return Loss vs. Ambient Temperature



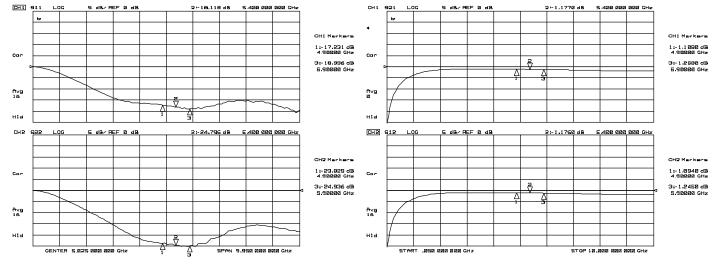


 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=0V,  $V_{CTL}$ 2=3.3V,  $T_a$ =+25°C,  $Z_s$ = $Z_l$ =50 $\Omega$ 



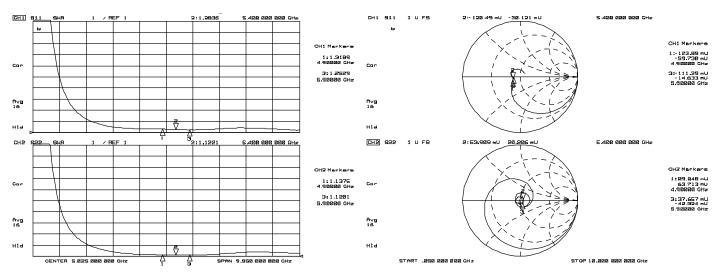


 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=0V,  $V_{CTL}$ 2=3.3V,  $T_a$ =+25°C,  $Z_s$ = $Z_l$ =50 $\Omega$ 



S11, S22 (f=50MHz to 10GHz)

S21, S12 (f=50MHz to 10GHz)

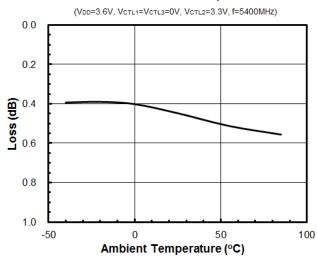


VSWRi, VSWRo (f=50MHz to 10GHz)

Zin, Zout (f=50MHz to 10GHz)

 $V_{DD}$ =3.6V,  $V_{CTL}$ 1= $V_{CTL}$ 3=0V,  $V_{CTL}$ 2=3.3V,  $Z_s$ = $Z_l$ =50 $\Omega$ 

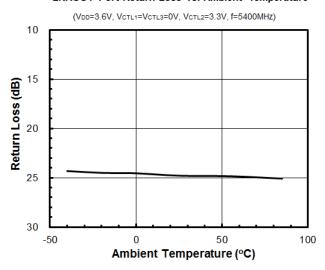
#### Loss vs. Ambient Temperature



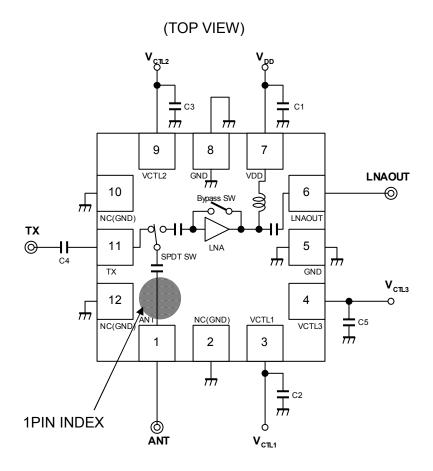
#### ANT Port Return Loss vs. Ambient Temperature

# (VDD=3.6V, VCTL1=VCTL3=0V, VCTL2=3.3V, f=5400MHz) 10 15 20 -50 0 50 100 Ambient Temperature (°C)

#### LNAOUT Port Return Loss vs. Ambient Temperature



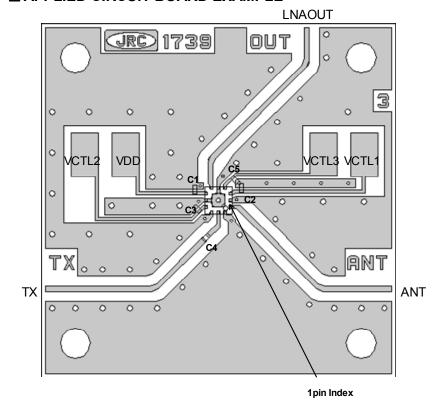
#### **■ APPLICATION CIRCUIT**



#### **■ PARTS LIST**

ID No.	Value	Notes
C1	0.1μF	
C2, C3, C5	10pF	Murata MFG (GRM03 series)
C4	27pF	

#### ■ APPLIED CIRCUIT BOARD EXAMPLE



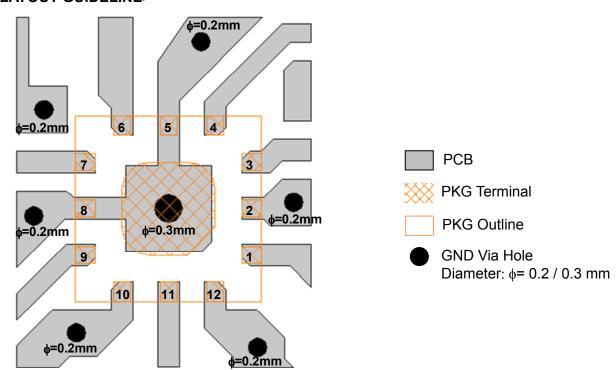
#### **PCB** Information

Size:

Substrate: FR-4 Thickness: 0.2mm Microstrip line width:

> 0.37mm ( $Z_0$ =50 $\Omega$ ) 26.0mm x 26.0mm

#### <PCB LAYOUT GUIDELINE>



#### **PRECAUTIONS**

- [1] All external parts should be placed as close as possible to the IC.
- [2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal.
- [3] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

#### ■ RECOMMENDED FOOTPRINT PATTERN (QFN12-51 PACKAGE Reference)

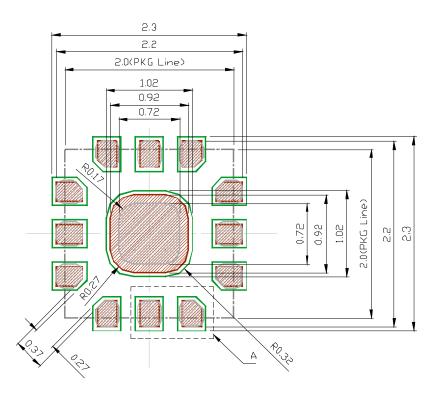
PKG: 2.0mm x 2.0mm

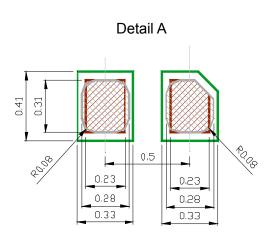
Pin pitch: 0.5mm

: Land

∭ : Mask (Open area) \*Metal mask thickness: 100μm

: Resist (Open area)





#### ■ NOISE FIGURE MEASUREMENT BLOCK DIAGRAM

#### **Measuring instruments**

NF Analyzer : Agilent N8975A Noise Source : Agilent 346A

#### Setting the NF analyzer

Measurement mode form

Device under test : Amplifier

System downconverter : off

Mode setup form

Sideband : LSB

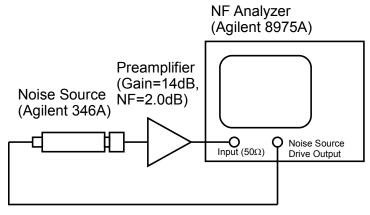
Averages : 16

Average mode : Point

Bandwidth : 4MHz

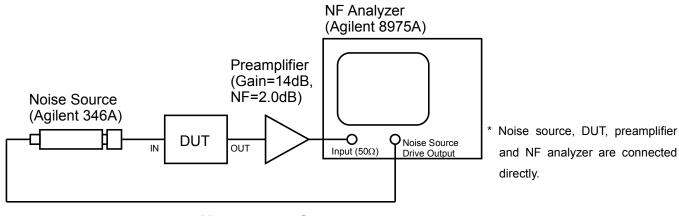
Loss comp : off

Tcold : setting the temperature of noise source (303K)



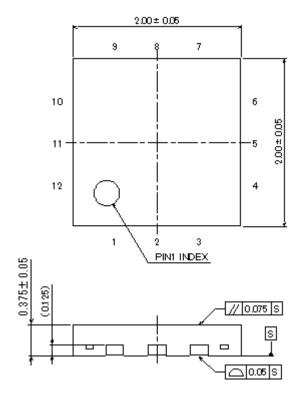
- \* Preamplifier is used to improve NF measurement accuracy.
- \* Noise source, preamplifier and NF analyzer are connected directly.

#### **Calibration setup**



#### **Measurement Setup**

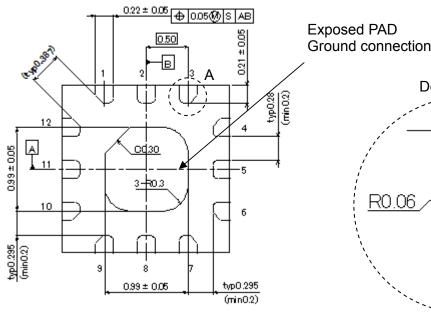
#### **■ PACKAGE OUTLINE (QFN12-51)**



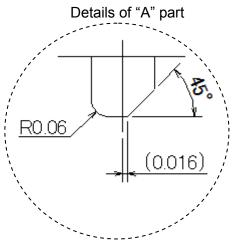
Unit : mm Board : Copper

: Ni/Pd/Au plating **Terminal Treat** Molding Material : Epoxy resin

Weight : 4.7mg



# Ground connection is required.



#### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]
The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

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