DC to 6 GHz, 45 dB TruPwr Detector with Envelope Threshold Detection

Data Sheet

ADL5904

FEATURES

RMS and envelope threshold detection
Broad input frequency range: dc to 6 GHz
RF input range: 45 dB (−30 dBm to +15 dBm)
RMS linear in decibel output, scaled 36.5 mV/dB
Input envelope threshold detection and latching
Programmable threshold and latch reset function
Fast response time: 12 ns from RFIN to Q/$\overline{Q}$ latch
All functions temperature and supply stable
Operates at 3.3 V from −40°C to +105°C
Low power: 3.5 mA
Power-down capability to 100 µA
16-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

Transmitter signal strength indication (TSSI)
Wireless power amplifier input and output protection
Wireless receiver input protection

FUNCTIONAL BLOCK DIAGRAM

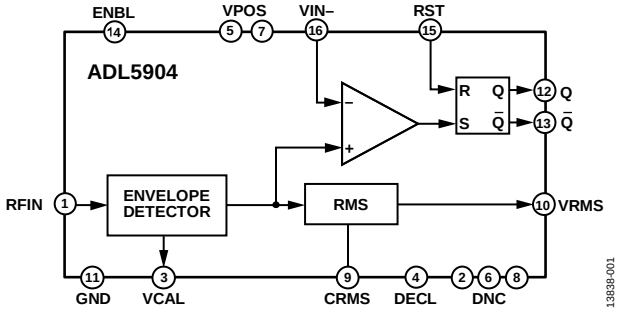

Figure 1.

GENERAL DESCRIPTION

The ADL5904 is a dual-function radio frequency (RF) TruPwr™ detector that operates from dc to 6 GHz. It provides rms power measurement along with a programmable envelope threshold detection function.

The rms power measurement function has a 45 dB detection range, nominally from −30 dBm to +15 dBm. The rms power measurement function features low power consumption and an intrinsically ripple free error transfer function.

The envelope threshold detection function compares the voltage from an internal envelope detector with a user defined input voltage. When the voltage from the envelope detector exceeds the user defined threshold voltage, an internal comparator captures and latches the event to a set/reset (SR) flip flop. The response time from the RF input signal exceeding the user programmed threshold to the output latching is 12 ns. The latched event is held on the flip-flop until a reset pulse is applied.

The RF input of the ADL5904 is dc-coupled, allowing operation down to arbitrarily low ac frequencies. It operates on a 3.3 V supply and consumes 3.5 mA. A disable mode reduces this current to 100 µA when a logic low is applied to the ENBL pin.

The ADL5904 is supplied in a 3 mm × 3 mm, 16-lead LFCSP for operation over the wide temperature range of −40°C to +105°C.

Rev. B
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REVISION HISTORY

7/2017—Rev. A to Rev. B

Changes to Basic Connection for RMS Measurement Section and Figure 44 ... 18
Change to Figure 54 ... 25
Change to C14 Default Value, Table 7 ... 26

5/2017—Rev. 0 to Rev. A

Changes to Ordering Guide ... 27

10/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{POS} = 3.3 V, continuous wave (CW) input, T_A = 25°C, Z_O = 50 Ω, Capacitor C_{RMS} = 10 nF, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			dc to 6000		MHz
f = 10 MHz					
±1.0 dB Input Range			45		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.63		V
	RFIN pin = −20 dBm		0.54		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.2		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.1/+0.2		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.2/+0.2		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.4/+0.2		dB
VRMS Logarithmic Slope	P_{IN} = −25 dBm to −10 dBm		36.5		mV/dB
	P_{IN} = −10 dBm to +10 dBm		35.3		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −25 dBm to −10 dBm		−35.2		dBm
	P_{IN} = −0 dBm to +10 dBm		−36		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		743		mV
	For threshold detection at 0 dBm		240		mV
	For threshold detection at −10 dBm		80		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.3/0		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.5/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.3/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.5/0		dB
f = 30 MHz					
±1.0 dB Input Range			45		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.62		V
	RFIN pin = −20 dBm		0.54		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.1/+0.1		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.2/+0.2		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.5/+0.2		dB
VRMS Logarithmic Slope	P_{IN} = −25 dBm to −10 dBm		36.8		mV/dB
	P_{IN} = −10 dBm to +10 dBm		35.4		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −25 dBm to −10 dBm		−34.7		dBm
	P_{IN} = −10 dBm to +10 dBm		−35.7		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		723		V
	For threshold detection at 0 dBm		238		mV
	For threshold detection at −10 dBm		80		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		0/0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.4/−0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.4/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		0/0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.4/−0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.4/0		dB
f = 100 MHz					
±1.0 dB Input Range			45		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −25 dBm, −10 dBm, and +10 dBm		15		dBm
Minimum			−30		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.63		V
	RFIN pin = −20 dBm		0.56		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.2		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.1/+0.2		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		0/0.1		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.2/+0.1		dB
VRMS Logarithmic Slope	P_{IN} = −25 dBm to −10 dBm		34.9		mV/dB
	P_{IN} = −10 dBm to +10 dBm		35		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −25 dBm to −10 dBm		−35.7		dBm
	P_{IN} = −10 dBm to +10 dBm		−35.6		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		742		mV
	For threshold detection at 0 dBm		239		mV
	For threshold detection at −10 dBm		81		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.4/−0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.5/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.4/−0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.5/0		dB
f = 900 MHz					
±1.0 dB Input Range			45		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−28		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.61		V
	RFIN pin = −20 dBm		0.57		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		0/0.1		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		0/0.1		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.2/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.4/+0.1		dB
VRMS Logarithmic Slope	P_{IN} = −20 dBm to 0 dBm		33.9		mV/dB
	P_{IN} = 0 dBm to 10 dBm		35.8		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −20 dBm to 0 dBm		−36.8		dBm
	P_{IN} = 0 dBm to 10 dBm		−34.8		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		752		mV
	For threshold detection at 0 dBm		241		mV
	For threshold detection at −10 dBm		81		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.2/+0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		0.1/0.3		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.2/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		0.1/0.3		dB
f = 1900 MHz					
±1.0 dB Input Range			45		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−28		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.62		V
	RFIN pin = −20 dBm		0.55		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.3		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.1/+0.3		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.2/−0.1		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.4/−0.2		dB
VRMS Logarithmic Slope	P_{IN} = −20 dBm to 0 dBm		34.8		mV/dB
	P_{IN} = 0 dBm to 10 dBm		36.9		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −20 dBm to 0 dBm		−35.9		dBm
	P_{IN} = 0 dBm to 10 dBm		−33.8		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		774		mV
	For threshold detection at 0 dBm		241		mV
	For threshold detection at −10 dBm		78		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		−0.2/+0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.1/0		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		±0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		−0.2/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.1/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		±0.2		dB
f = 2600 MHz					
±1.0 dB Input Range			43.5		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −20 dBm, 0 dBm, and +10 dBm		16		dBm
Minimum			−27.5		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.6		V
	RFIN pin = −20 dBm		0.51		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.3/+0.3		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.3/+0.3		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.2/0		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.3/0		dB
VRMS Logarithmic Slope	P_{IN} = −20 dBm to 0 dBm		36.1		mV/dB
	P_{IN} = 0 dBm to 10 dBm		37.5		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −20 dBm to 0 dBm		−34		dBm
	P_{IN} = 0 dBm to 10 dBm		−32.7		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		775		mV
	For threshold detection at 0 dBm		236		mV
	For threshold detection at −10 dBm		76		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		−0.3/+0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		−0.2/0		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.4/−0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		−0.3/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		−0.2/0		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.4/−0.1		dB
f = 3500 MHz					
±1.0 dB Input Range			42		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −18 dBm, 0 dBm, and +10 dBm		17		dBm
Minimum			−25		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.54		V
	RFIN pin = −20 dBm		0.44		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.3		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.2/+0.3		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		−0.3/−0.1		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		−0.4/−0.1		dB
VRMS Logarithmic Slope	P_{IN} = −18 dBm to 0 dBm		35.9		mV/dB
	P_{IN} = 0 dBm to +10 dBm		38.8		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −18 dBm to 0 dBm		−32.1		dBm
	P_{IN} = 0 dBm to +10 dBm		−29.7		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		608		mV
	For threshold detection at 0 dBm		177		mV
	For threshold detection at −10 dBm		55		mV
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		±0.1		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.5/−0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		±0.1		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.5/−0.1		dB
f = 5800 MHz					
±1.0 dB Input Range			37		dB
Input Level, ±1.0 dB					
Maximum	Three-point calibration at −10 dBm, 0 dBm, and +10 dBm		19		dBm
Minimum			−18		dBm
VRMS Output Voltage	RFIN pin = 10 dBm		1.34		V
	RFIN pin = −20 dBm		0.26		V
VRMS Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C, P_{IN} = 10 dBm		−0.1/+0.1		dB
	−40°C < T_A < +105°C, P_{IN} = 10 dBm		−0.1/+0.1		dB
	−40°C < T_A < +85°C, P_{IN} = −15 dBm		0/0.5		dB
	−40°C < T_A < +105°C, P_{IN} = −15 dBm		0/0.5		dB
VRMS Logarithmic Slope	P_{IN} = −10 dBm to 0 dBm		36.4		mV/dB
	P_{IN} = 0 dBm to 10 dBm		39.9		mV/dB
VRMS Logarithmic Intercept	P_{IN} = −10dBm to 0 dBm		−25.9		dBm
	P_{IN} = 0 dBm to 10 dBm		−23.7		dBm
VIN− Setpoint Voltage	For threshold detection at 10 dBm		334		mV
	For threshold detection at 0 dBm		92		mV
	For threshold detection at −10 dBm		29		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Threshold Variation vs. Temperature	−40°C < T_A < +85°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +85°C, P_{IN} ≈ 0 dBm		±0.4		dB
	−40°C < T_A < +85°C, P_{IN} ≈ −10 dBm		−0.6/+0.4		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 10 dBm		±0.2		dB
	−40°C < T_A < +105°C, P_{IN} ≈ 0 dBm		±0.4		dB
	−40°C < T_A < +105°C, P_{IN} ≈ −10 dBm		−0.6/+0.4		dB
THRESHOLD DETECT OUTPUT	Q, $\overline{Q}$, and RST pins, 900 MHz input frequency				
Propagation Delay	RFIN pin = off to 10 dBm, V_{IN-} = 400 mV (5 dB overdrive)		12		ns
	RFIN pin = off to −5 dBm, V_{IN-} = 75 mV (5 dB overdrive)		12		ns
Output Voltage	Q, $\overline{Q}$				
Low	I_{OL} = 1 mA			300	mV
High	I_{OH} = 1 mA	3.0			V
RESET INTERFACE	RST pin				
RST Input Voltage					
Low				0.6	V
High		2			V
RST Input Bias Current			20		nA
Reset Time	RST at 50% to Q low and $\overline{Q}$ high		15		ns
COMPARATOR INTERFACE	VIN− pin				
VIN− Input Range			0 to 1.5		V
VIN− Input Bias Current			−20		µA
VIN− for Comparator Disable		V_{POS}			V
VCAL INTERFACE	VCAL pin				
VCAL Output Voltage	RFIN pin = off		750		mV
	RFIN pin = −10 dBm, 900 MHz		825		mV
	RFIN pin = 10 dBm, 900 MHz		1.5		V
POWER-DOWN INTERFACE	ENBL pin				
Voltage Level to Enable		2		V_{POS}	V
Voltage Level to Disable		0		0.6	V
Input Bias Current	V_{ENBL} = 2.2 V		<20		nA
POWER SUPPLY INTERFACE	VPOS pin				
Supply Voltage		3.15	3.3	3.45	V
Quiescent Current	T_A = 25°C, no signal at RFIN		3.5		mA
	T_A = 105°C, no signal at RFIN		4		mA
Power-Down Current	ENBL = low		100		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
Input Average RF Power[1]	25 dBm
Equivalent Voltage, Sine Wave Input	5.62 V peak
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Driven from a 50 Ω source. Input ac-coupled with an external 82.5 Ω shunt resistor.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-16-22	80.05	4.4	°C/W

[1] Thermal impedance simulated value is based on no airflow with the exposed pad soldered to a 4-layer JEDEC board.
[1] Thermal impedance from junction to exposed pad on underside of package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

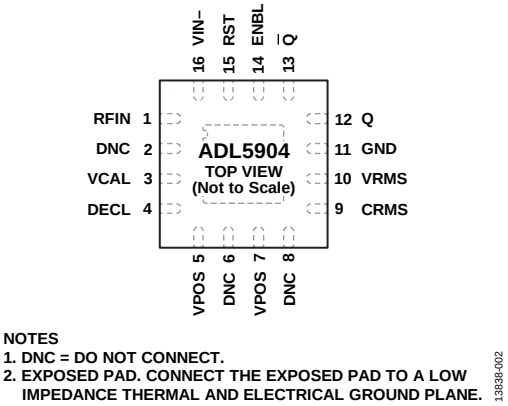


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is dc-coupled and is not internally matched. A broadband 50 Ω match is achieved using an external 82.5 Ω shunt resistor with a 0.47 µF ac coupling capacitor placed between the shunt resistor and the RF input. Smaller ac coupling capacitor values can be used if low frequency operation is not required.
2, 6, 8	DNC	Do Not Connect. Do not connect to these pins.
3	VCAL	Threshold Calibration. The voltage on this pin determines the correct threshold voltage that must be applied to Pin 16 (VIN–) to set a particular RF power threshold. This process has two steps: first, measure the output voltage on VCAL with no RF signal applied to RFIN (this voltage is typically 750 mV). Next, apply the RF input power to RFIN, which causes the circuit to trip and again measure the voltage on the VCAL pin. The difference between these two voltages is equal to the threshold voltage that must be applied to VIN– during operation.
4	DECL	Internal Decoupling. Bypass this pin to ground using a 4.02 Ω resistor connected in series with a 100 nF capacitor.
5, 7	VPOS	The supply voltage range = 3.3 V ±10%. Place power supply decoupling capacitors on Pin 5. There is no requirement for power supply decoupling caps on Pin 7.
9	CRMS	RMS Averaging Capacitor. Connect a capacitor between the DECL pin and the CRMS pin to set the appropriate level of rms averaging. Set the value of the rms averaging capacitor based on the peak to average ratio and bandwidth of the input signal and based on the desired output response time and residual output noise.
10	VRMS	RMS Detector Output. The output from the VRMS pin is proportional to the logarithm of the rms value at the input level.
11	GND	Device Ground. Connect the GND pin to system ground using a low impedance path.
12, 13	Q, $\overline{Q}$	Differential Digital Outputs of Threshold Detect Flip Flop. Q latches high when the output of the internal envelope detector exceeds the threshold voltage on the internal comparator VIN– input.
14	ENBL	Device Enable. Connect the ENBL pin to logic high to enable the device.
15	RST	Flip Flop Reset. Taking RST high clears the latched flip flop output, setting the Q and $\overline{Q}$ outputs to low and high, respectively.
16	VIN–	Inverting Input to the Threshold Detection Comparator. The voltage on this pin is compared to the output voltage of the internal envelope detector, which is driven by the RF input level. If the output voltage of the envelope detector exceeds the voltage on VIN–, the flip flop latches the Q output to high and the $\overline{Q}$ output to low.
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{POS} = 3.3 V, C_{RMS} = 10 nF, Input levels referred to 50 Ω source. Input RF signal is a sine wave (CW), unless otherwise indicated.

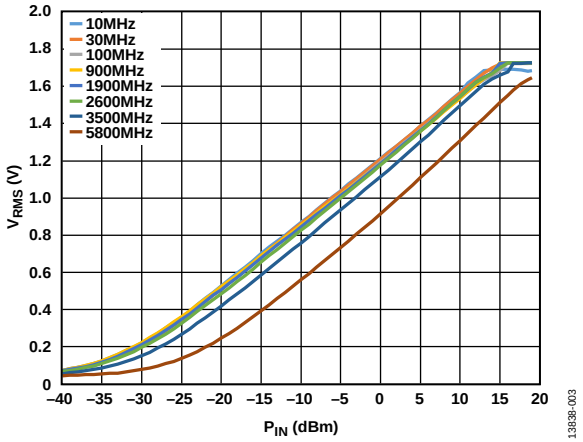


Figure 3. V_{RMS} vs. Input Level (P_{IN}) for Various Frequencies (30 MHz to 6 GHz) at 25°C

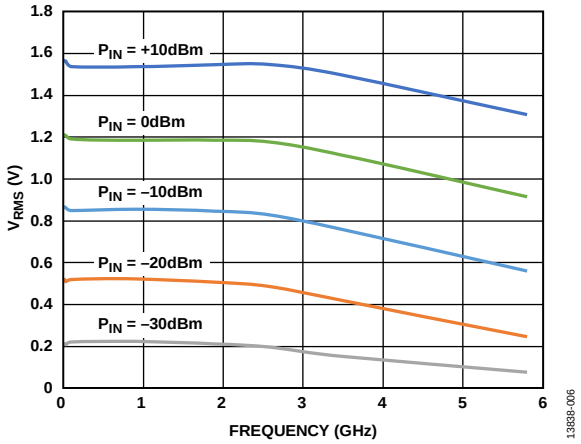


Figure 6. V_{RMS} vs. Frequency for Four Input Levels (10 MHz to 6 GHz)

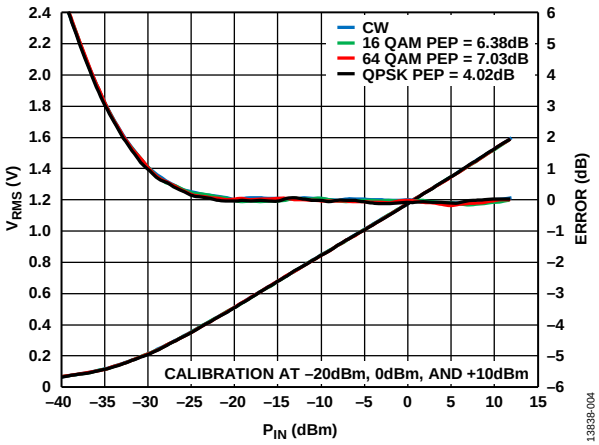


Figure 4. V_{RMS} and Error from CW Linear Reference vs. Input Level and Signal Modulation (QPSK, 16 QAM, 64 QAM), Frequency = 900 MHz, C_{RMS} = 1 µF (PEP Is Peak Envelope Power)

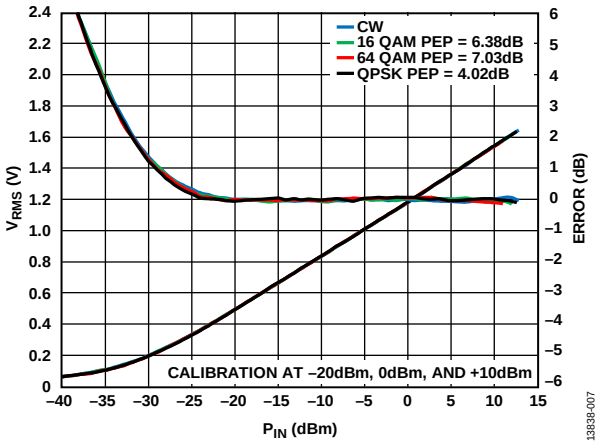


Figure 7. V_{RMS} and Error from CW Linear Reference vs. Input Level and Signal Modulation (QPSK, 16 QAM, 64 QAM), Frequency = 2.14 GHz, C_{RMS} = 1 µF

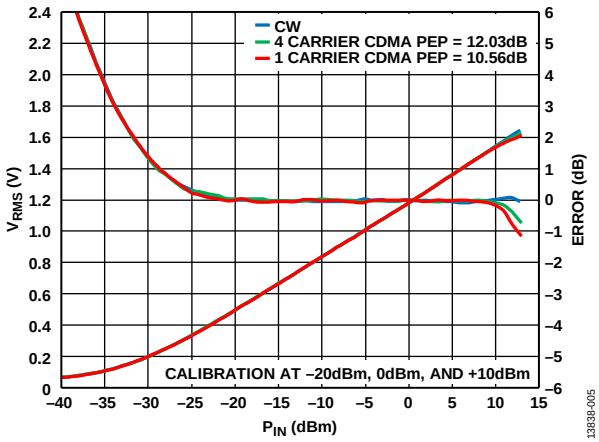


Figure 5. V_{RMS} and Error from CW Linear Reference vs. Input Level and Signal Modulation (One-Carrier W-CDMA, Four-Carrier W-CDMA), Frequency = 2.14 GHz, C_{RMS} = 1 µF

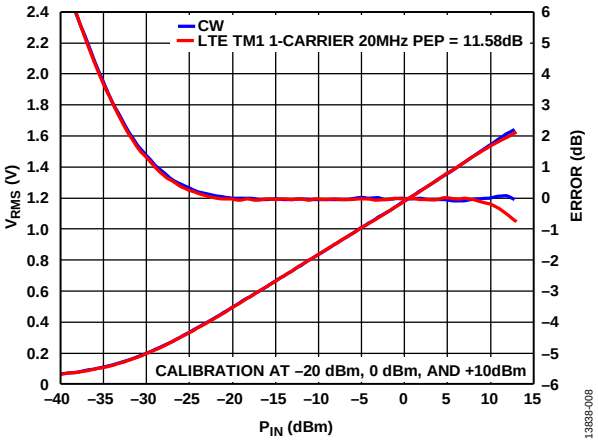


Figure 8. V_{RMS} and Error from CW Linear Reference vs. Input Level and Signal Modulation (LTE TM1 One-Carrier, 20 MHz), Frequency = 2.14 GHz, C_{RMS} = 1 µF

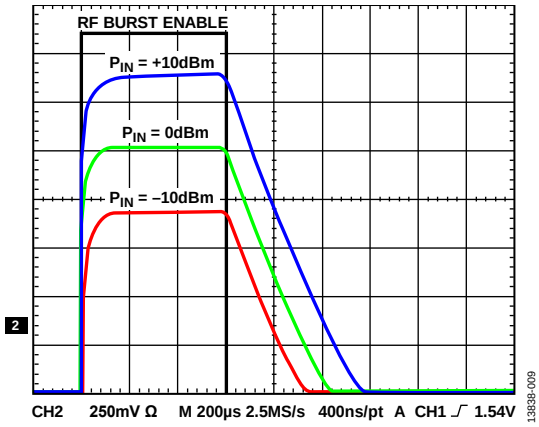


Figure 9. Output Response to RF Burst Input, Carrier Frequency = 900 MHz, C_{RMS} = 100 nF (see Figure 41 in the Test Circuits Section)

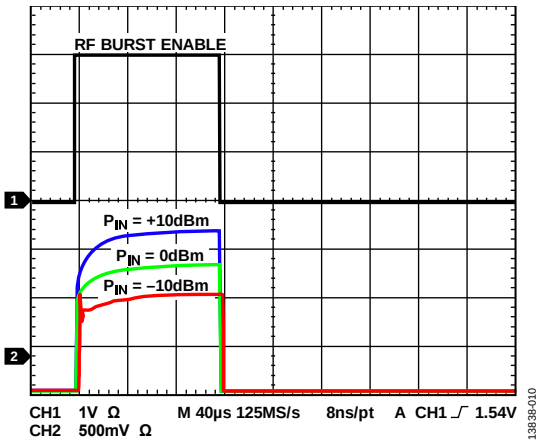


Figure 10. Output Response to Gating on ENBL Pin for Various RF Input Levels, Carrier Frequency = 900 MHz, C_{RMS} = 100 nF

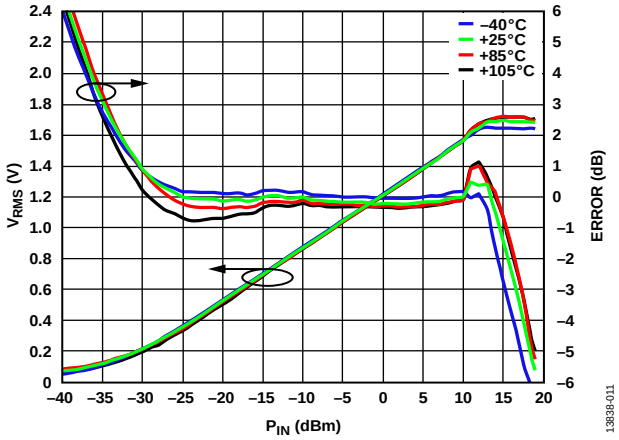


Figure 11. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 10 MHz

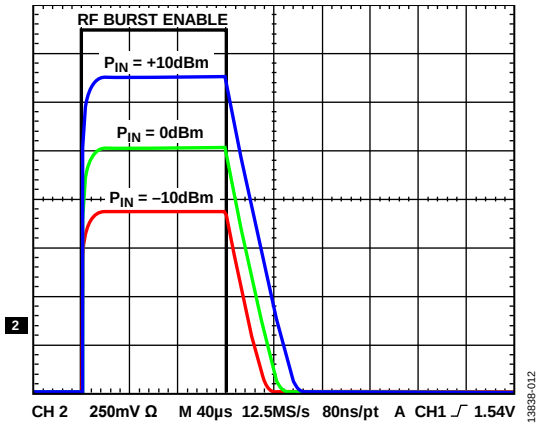


Figure 12. Output Response to RF Burst Input, Carrier Frequency = 900 MHz, C_{RMS} = 10 nF (see Figure 41 in the Test Circuits Section)

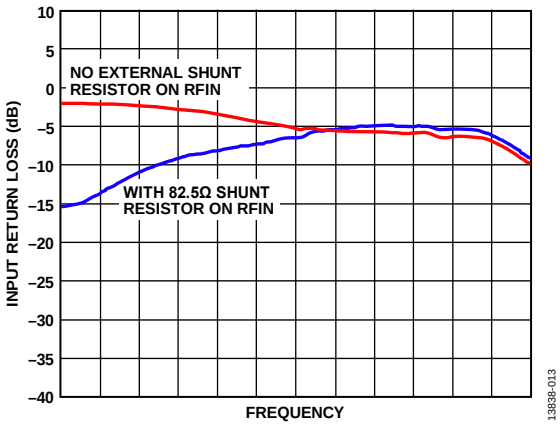


Figure 13. Input Return Loss vs. RF Frequency (With and Without External 82.5 Ω Shunt Resistor) from 10 MHz to 6 GHz

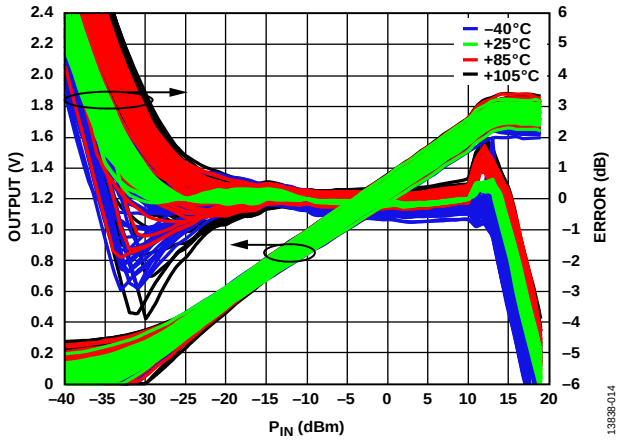


Figure 14. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 10 MHz

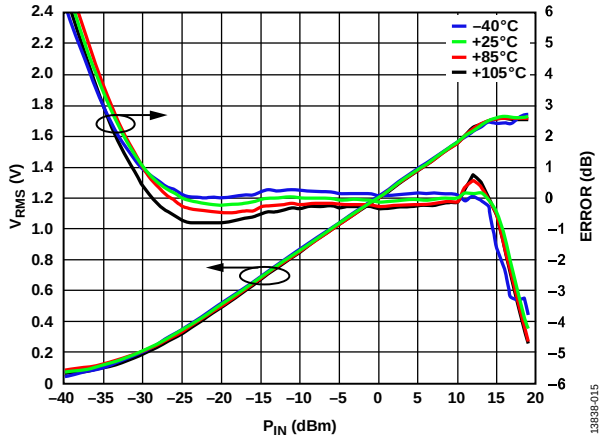


Figure 15. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 30 MHz

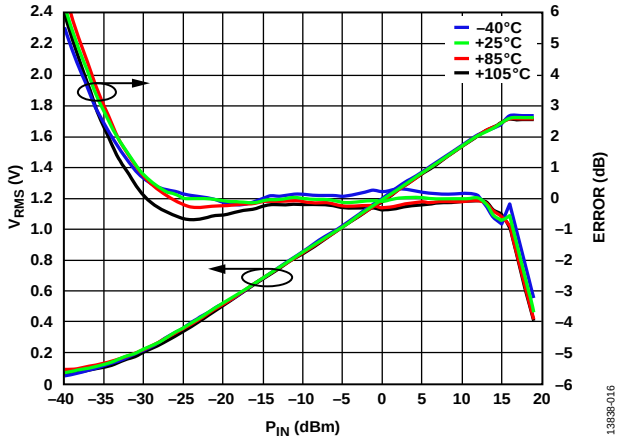


Figure 16. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 100 MHz

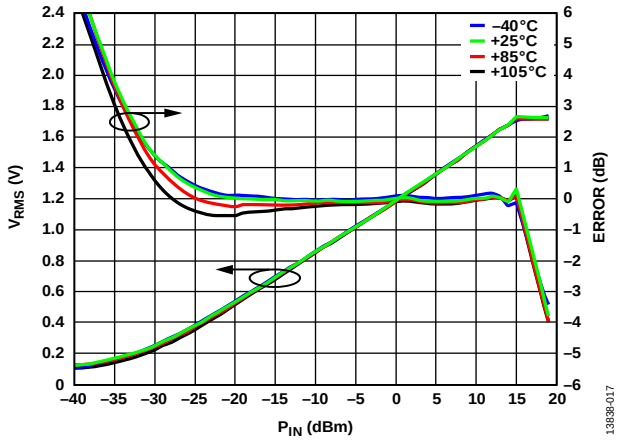


Figure 17. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 900 MHz

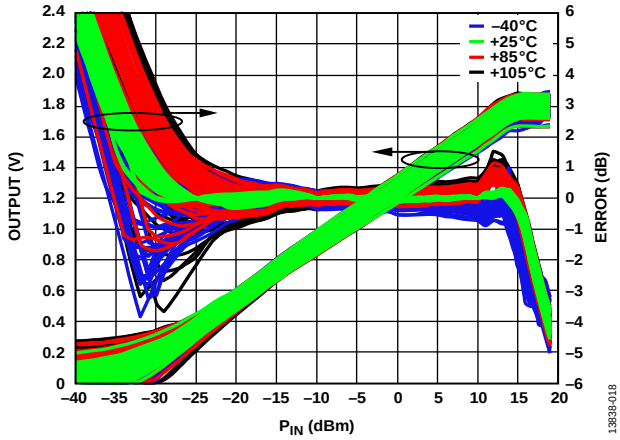


Figure 18. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 30 MHz

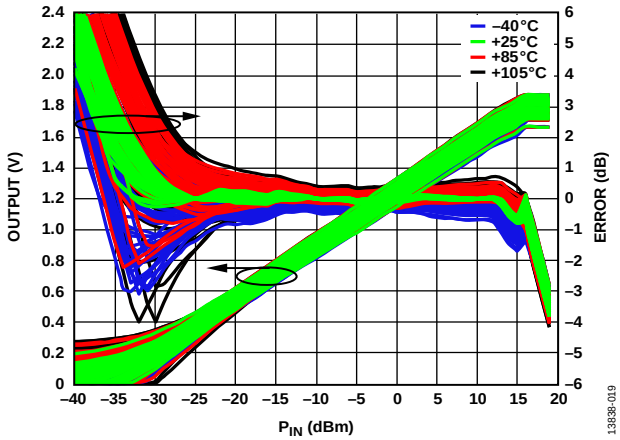


Figure 19. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 100 MHz

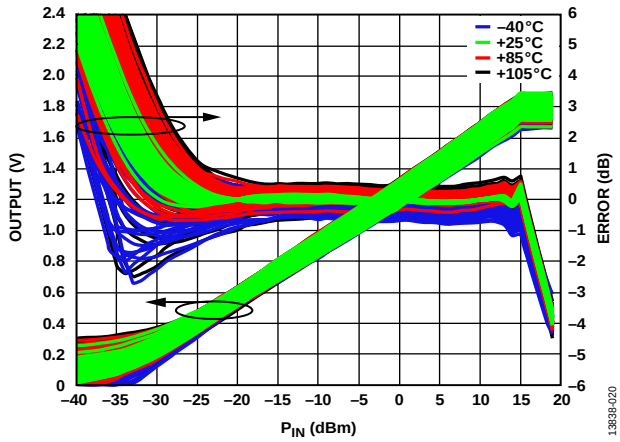


Figure 20. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 900 MHz

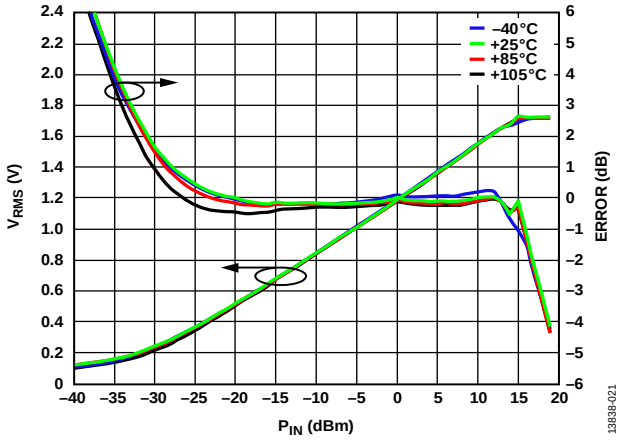


Figure 21. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 1.9 GHz

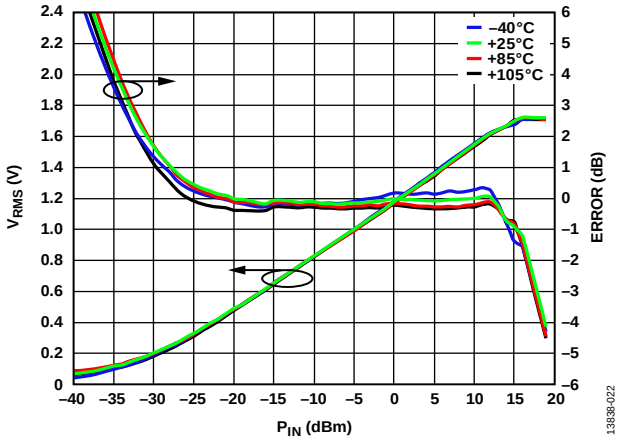


Figure 22. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 2.6 GHz

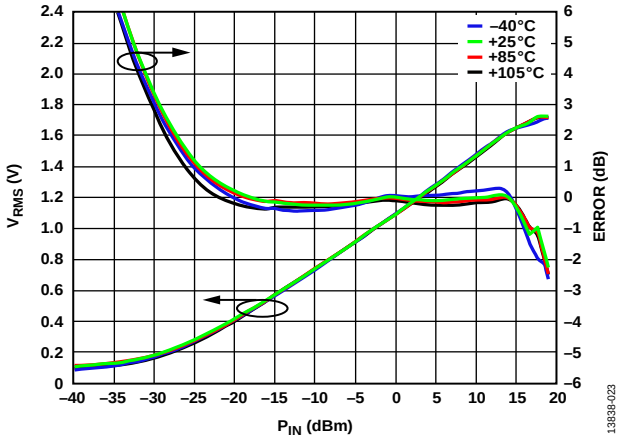


Figure 23. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 3.5 GHz

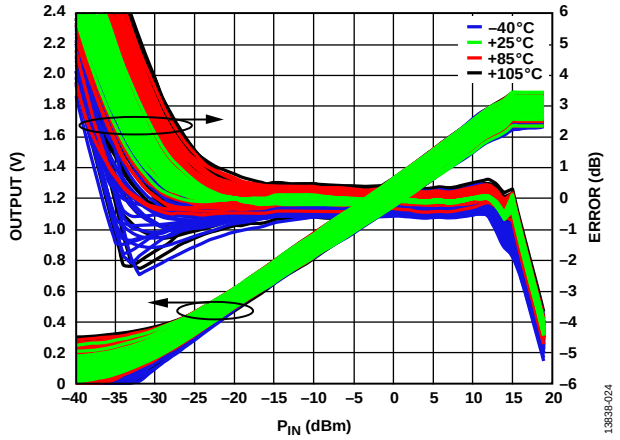


Figure 24. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 1.9 GHz

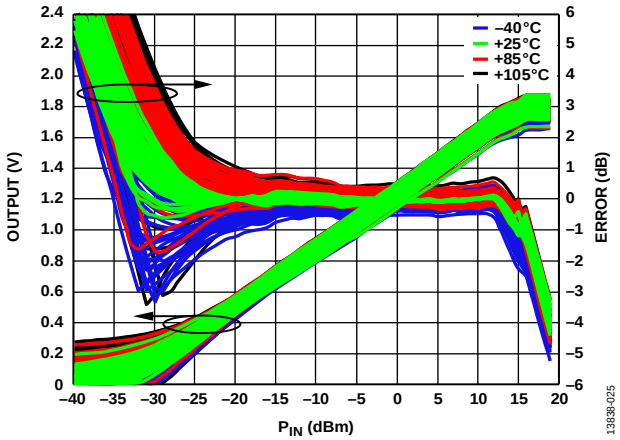


Figure 25. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 2.6 GHz

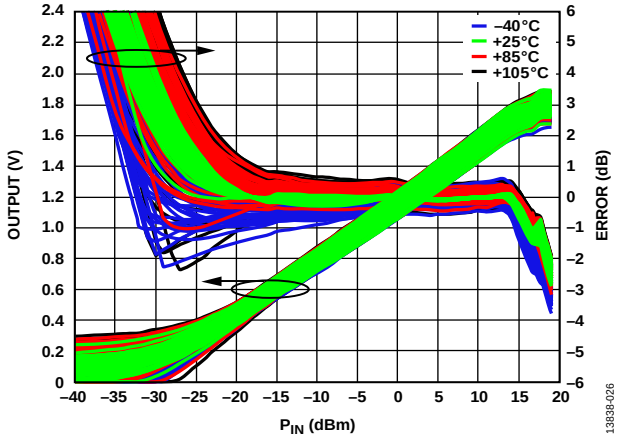


Figure 26. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 3.5 GHz

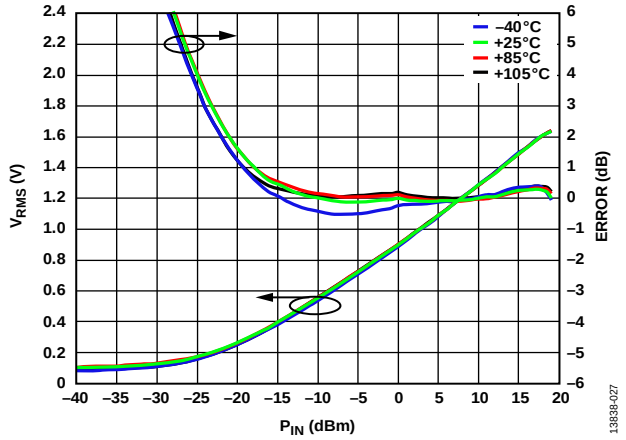


Figure 27. V_{RMS} and Log Conformance Error vs. Input Level (P_{IN}) for Various Temperatures at 5.8 GHz

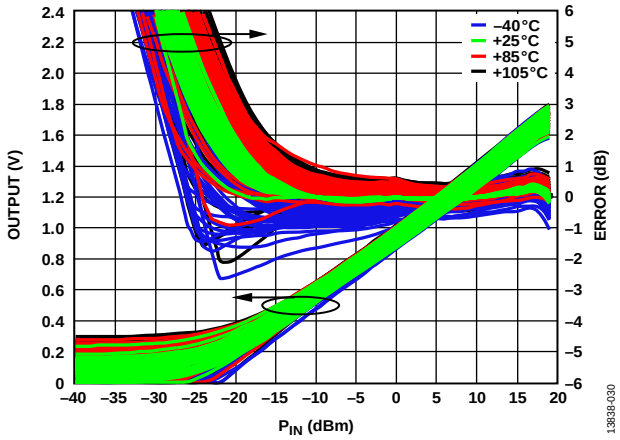


Figure 30. Distribution of Log Conformance Error with Respect to Calibration at 25°C vs. Input Level (P_{IN}) for Various Temperatures at 5.8 GHz

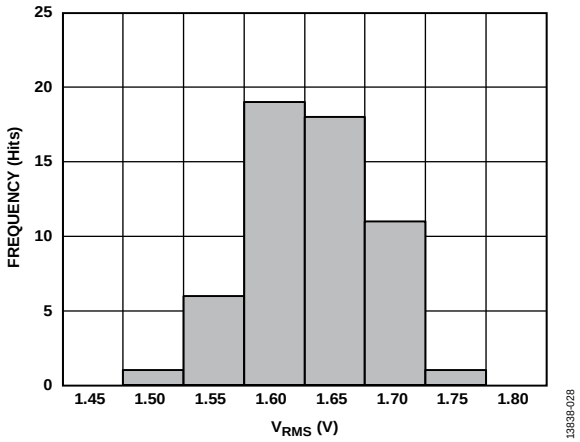


Figure 28. Distribution of V_{RMS}, P_{IN} = 10 dBm, 900 MHz

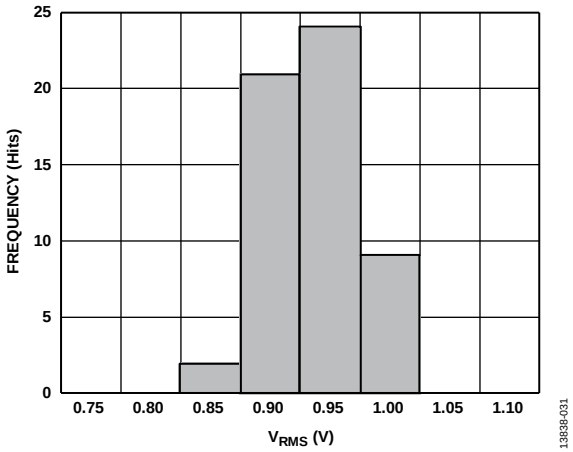


Figure 31. Distribution of V_{RMS}, P_{IN} = –10 dBm, 900 MHz

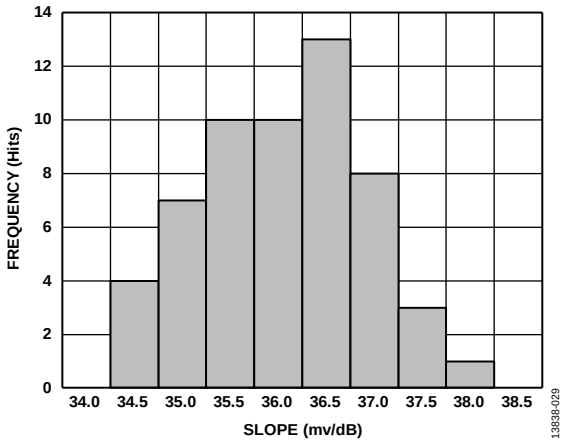


Figure 29. Distribution of Slope at 900 MHz, Intercept Calculated Using VRMS at 0 dBm and 10 dBm

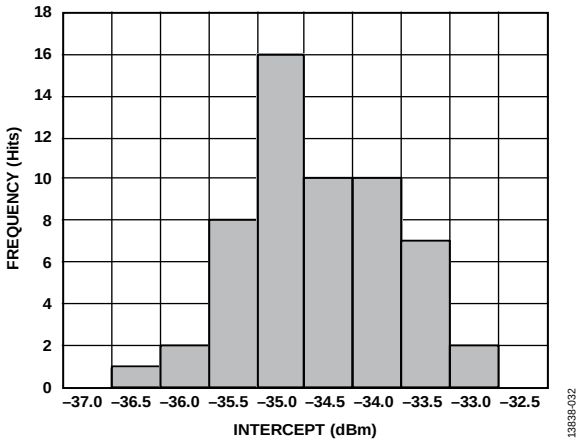


Figure 32. Distribution of Intercept at 900 MHz, Slope Calculated Using VRMS at 0 dBm and 10 dBm

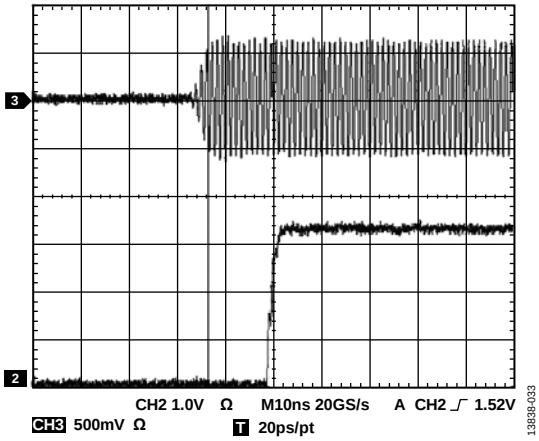


Figure 33. Q Output Response, P_{IN} = Off to 6 dBm, VIN– (400 mV) Set to Trigger at 5 dBm (Overdrive Level = 1 dB)

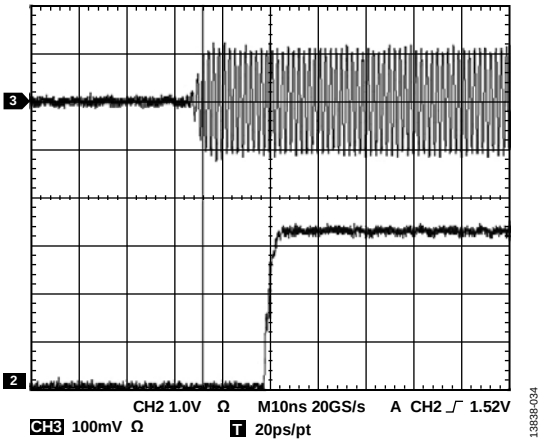


Figure 34. Q Output Response, P_{IN} = Off to −9 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 1 dB, V_{IN-} = 75 mV)

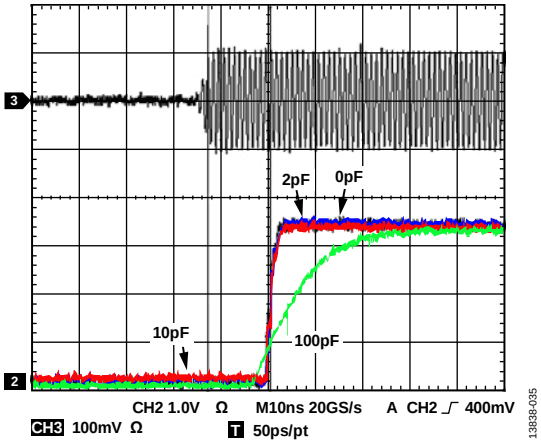


Figure 35. Q Output Response vs. Load Capacitance, P_{IN} = Off to −10 dBm; Overdrive Threshold Voltage Set to Trigger at −11 dBm (Overdrive Level = 1 dB, V_{IN-} = 65 mV)

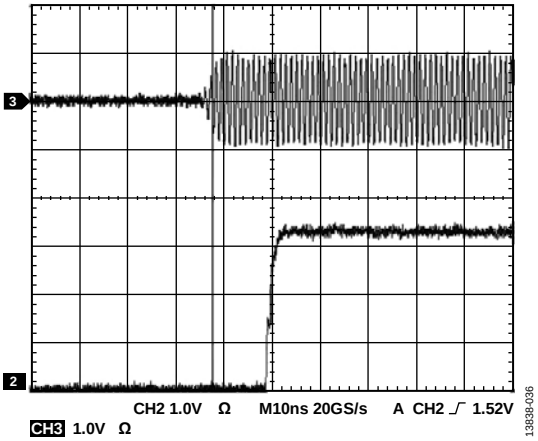


Figure 36. Q Output Response, P_{IN} = Off to 10 dBm, VIN– (400 mV) Set to Trigger at 5 dBm (Overdrive Level = 5 dB)

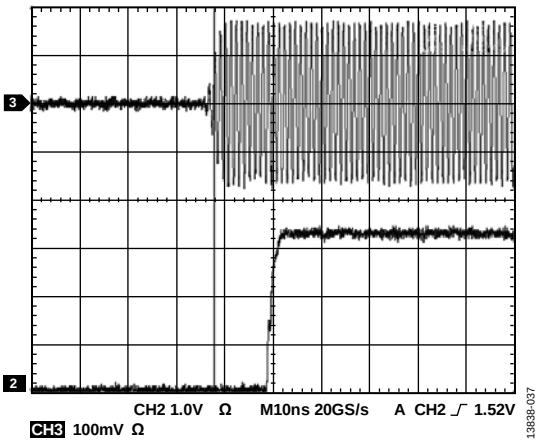


Figure 37. Q Output Response, P_{IN} = Off to −5 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 5 dB, V_{IN-} = 75 mV)

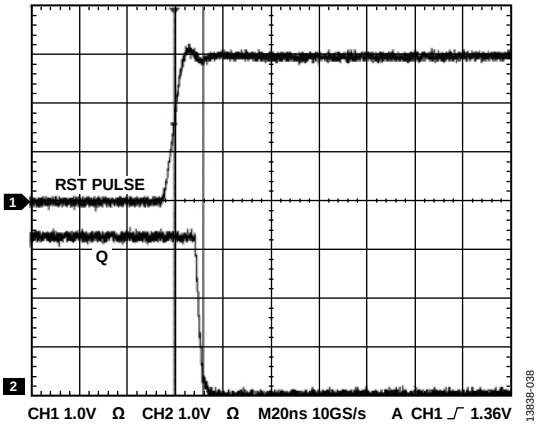


Figure 38. Response of Q Output to RST

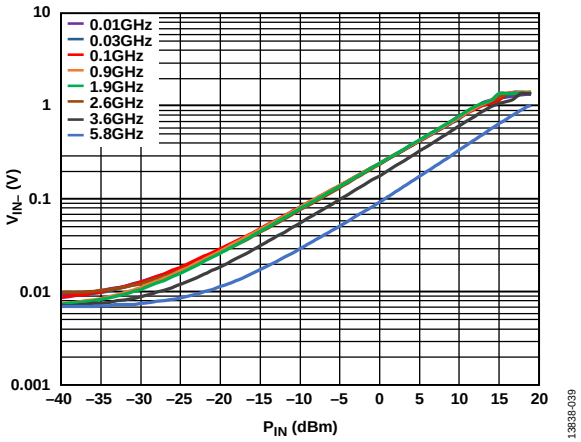


Figure 39. V_{IN-} vs. P_{IN} at Various Frequencies

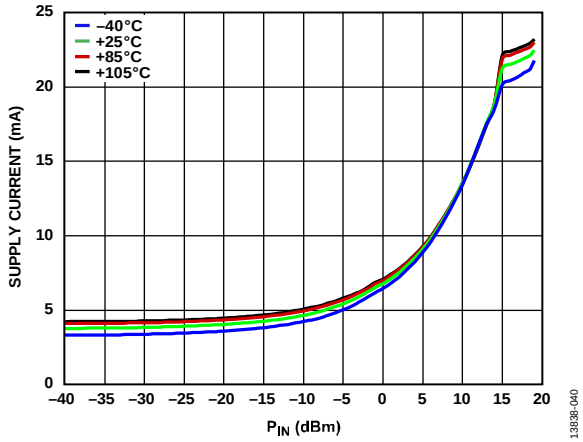


Figure 40. Supply Current vs. Input Level (P_{IN}) for Various Temperatures

TEST CIRCUITS

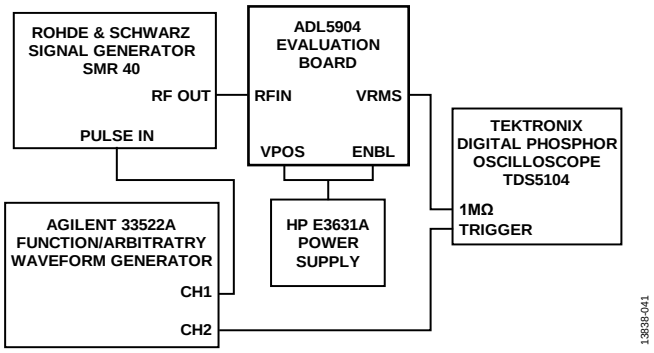


Figure 41. Hardware Configuration for Output Response to RF Burst Input Measurements

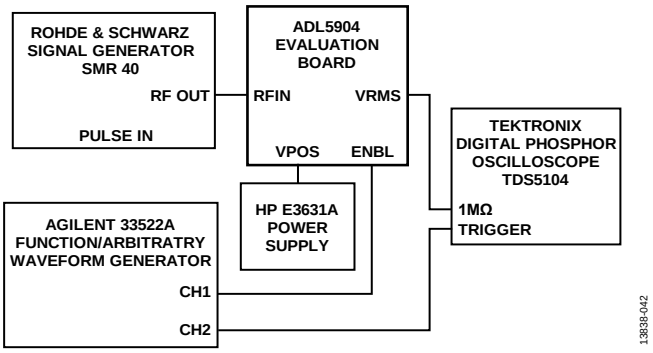


Figure 42. Hardware Configuration for Output Response to ENBL Pin Gating Measurements

THEORY OF OPERATION

The ADL5904 is a true rms detector with a 45 dB measurement range at 1.9 GHz with useable range up to 6 GHz. It features no error ripple over its range, low temperature drift, and very low power consumption. Temperature stability of the rms output measurements provides ≤±0.5 dB error (typical) over the temperature range of −40°C to +85°C at up to 3.5 GHz. The measurement output voltage scales linearly in decibels with a slope of typically 36.9 mV/dB at 1.9 GHz.

The core rms processing of the ADL5904 uses a proprietary multistage technique that provides accuracy for complex modulation signals irrespective of the crest factor of the input signal. An integrating filter capacitor at the CRMS pin performs the square domain averaging.

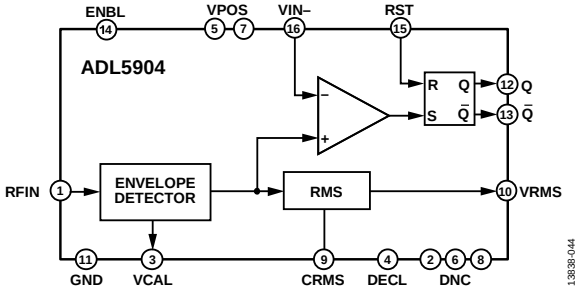


Figure 43. Functional Block Diagram

The output of the first signal processing stage (the envelope detector), also drives the noninverting input of a threshold detecting comparator. The inverting input of this comparator is typically driven by a fixed external dc voltage. When the output of the envelope detector exceeds the voltage on the inverting input of the comparator, the comparator goes high. This excursion is then captured and held by an SR flip flop. The state of this flip flop is then held until the level sensitive RST pin is taken high.

BASIC CONNECTIONS FOR RMS MEASUREMENT

The ADL5904 requires a single supply of 3.3 V. The supply is connected to the VPOS supply pins. Decouple these pins using two capacitors with values equal or similar to those shown in the Figure 44. Place these capacitors as close to Pin 5 as possible. Connect Pin 11 (GND) and the exposed pad to a ground plane with low electrical and thermal impedance.

A single-ended input at the RFIN pin drives the ADL5904. Because the input is dc-coupled, an external ac coupling capacitor must be used. A 470 nF capacitor is recommended for applications that require frequency coverage from 6 GHz down to tens of kilohertz. For applications that do not need such low frequency coverage, a larger value of capacitance can be used.

In addition to the ac-coupling capacitor, an external 82.5 Ω shunt resistor is required to provide a wideband input match. Figure 13 shows a comparison of the input return loss, with and without the external shunt resistor.

The rms measurement voltage is available on the VRMS pin. Place a 10 nF load capacitor on this pin.

The DECL pin provides a bypass capacitor connection for an on-chip regulator. The DECL pin is connected to ground with a 4.02 Ω resistor and a 0.1 µF capacitor. The CRMS pin is the averaging node for the rms computation. Place an rms averaging capacitor between the CRMS and DECL pins. For information on choosing the C_{RMS} capacitor, see the Choosing a Value for CRMS section. Using smaller values for C_{RMS} allows quicker response times to a pulsed waveform. Higher values of C_{RMS} are required for correct rms computation as the peak to average ratio of modulated signals increases and the bandwidth of the modulated signals decreases.

If the threshold detection circuitry is not used, the VIN− pin can be tied to V_{POS} or left open (this pin has an internal pull-up to VPOS).

The ENBL pin configures the device enable interface. Connecting the ENBL pin to a logic high signal (2 V to 3.3 V) enables the device, and connecting the pin to a logic low signal (0 V to 0.6 V) disables the device. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

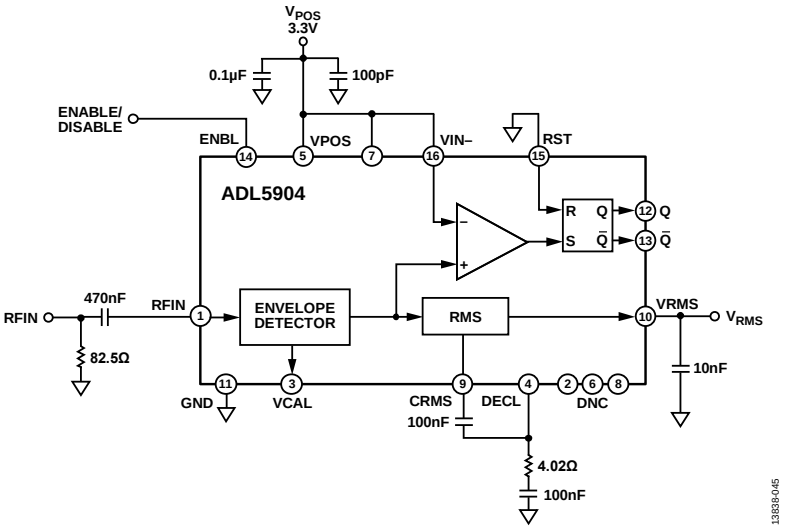


Figure 44. Basic Connections for RMS Power Measurement

CHOOSING A VALUE FOR C_{RMS}

C_{RMS} provides the averaging function for the internal rms computation. Using the minimum value for C_{RMS} allows the quickest response time to a pulsed waveform, but leaves significant output noise on the output voltage signal. However, a large filter capacitor reduces output noise and improves the rms measurement accuracy but at the expense of the response time.

In applications where the response time is not critical, place a relatively large capacitor on the CRMS pin. In Figure 44, a value of 100 nF is used. For most signal modulation schemes, this value ensures excellent rms measurement accuracy and low residual output noise. There is no maximum capacitance limit for C_{RMS}.

Figure 45 and Figure 46 show how output noise varies with C_{RMS} when the ADL5904 is driven by a single-carrier W-CDMA (Test Model TM1-64, peak envelope power = 10.6 dB, bandwidth = 3.84 MHz) and by an LTE signal (Test Model TM1-20, peak envelope power = 11.58 dB, bandwidth = 20 MHz), respectively.

Figure 45 and Figure 46 also show how the value of C_{RMS} affects the response time. This response time is measured by applying an RF burst at 2.14 GHz at 0 dBm to the ADL5904. The 10% to 90% rise time and 90% to 10% fall time are then measured.

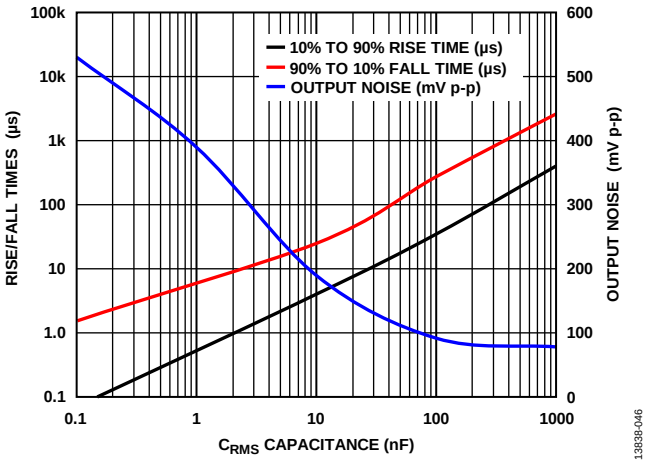


Figure 45. Output Noise, Rise and Fall Times vs. C_{RMS} Capacitance, Single-Carrier W-CDMA (Test Model TM1-64) at 900 MHz with P_{IN} = 0 dBm

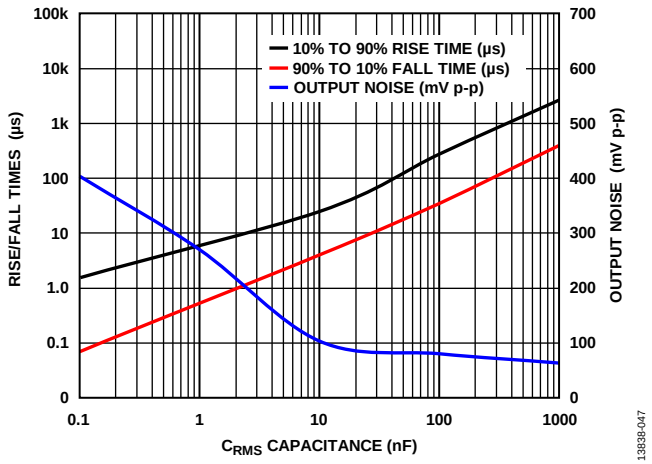


Figure 46. Output Noise, Rise and Fall Times vs. C_{RMS} Capacitance, Single-Carrier LTE (Test Model TM1-20) at 900 MHz with P_{IN} = 0 dBm

Table 5 shows the recommended minimum values of C_{RMS} for various modulation schemes. Table 5 also shows the output rise and fall times and noise performance. Using lower capacitor values results in faster response times but can result in degraded rms measurement accuracy. If the output noise shown in Table 5 is unacceptably high, it can be reduced by increasing C_{RMS} or by implementing an averaging algorithm after the output voltage of the ADL5904 is sampled by an analog-to-digital converter (ADC).

The values in Table 5 were experimentally determined to be the minimum capacitance that ensures good rms accuracy for that particular signal type. This test was initially performed with a large capacitance value on the CRMS pin (for example, 10 µF). The value of V_{RMS} was noted for a fixed input level (for example, −10 dBm). The value of C_{RMS} was then progressively reduced (this can be accomplished with press-down capacitors) until the value of V_{RMS} started to deviate from its original value (this indicates that the accuracy of the rms computation is degrading and that C_{RMS} is becoming too small).

In general, the minimum C_{RMS} value required increases as the peak to average ratio of the carrier increases. The minimum required C_{RMS} also tends to increase as the bandwidth of the carrier decreases. With narrow-band carriers, the noise spectrum of the V_{RMS} output tends to have a correspondingly narrow profile. The relatively narrow spectral profile requires a larger value of C_{RMS} that reduces the low-pass corner frequency of the averaging function and ensures a valid rms computation.

Table 5. Recommended Minimum C_{RMS} Values for Various Modulation Schemes

Modulation/Standard	Peak Envelope Power Ratio Ratio (dB)	Carrier Bandwidth (MHz)	C_{RMSMIN} (nF)	Output Noise (mV p-p)	Rise/Fall Times (µs)
QPSK, 5 MSPS (SQR COS) Filter, α = 0.35)	3.3	5	10	42	4/25
QPSK ,15 MSPS (SQR COS Filter, α = 0.35)	3.3	15	1	38	0.5/6
64 QAM, 1 MSPS (SQR COS Filter, α = 0.35)	7.4	1	100	64	35/276
64 QAM, 5 MSPS (SQR COS Filter, α = 0.35)	7.4	5	100	54	35/276
64 QAM, 13 MSPS (SQR COS Filter, α = 0.35)	7.4	13	10	56	4/25
W-CDMA, One-Carrier, TM1-64	10.6	3.84	100	92	35/276
W-CDMA Four-Carrier, TM1-64, TM1-32, TM1-16, TM1-8	15.96	18.84	100	98	35/276
LTE, TM1, One-Carrier, 20 MHz (2048 QPSK Subcarriers)	11.58	20	100	80	35/276

VRMS CALIBRATION AND ERROR CALCULATION

The measured transfer function of the ADL5904 at 900 MHz is shown in Figure 47, which contains plots of both output voltage and log conformance error vs. input level for one device. As the input level varies from −30 dBm to +15 dBm, the output voltage varies from 200 mV to approximately 1.7 V.

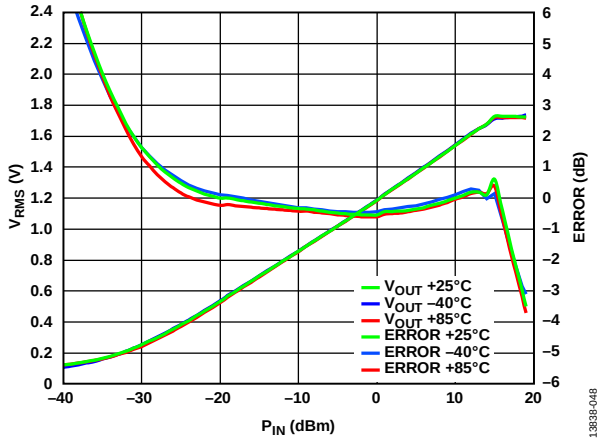


Figure 47. V_{RMS} and Log Conformance Error at 900 MHz, −40°C, +25°C, and +85°C with Log Conformance Error Calculated Based on Two-Point Calibration at −20 dBm and +10 dBm

Calibration must be performed to achieve high accuracy because the output voltage for a particular input level varies from device to device. For a two-point calibration, the equation for the idealized output voltage is

$$V_{RMS\,(IDEAL)} = Slope \times (P_{IN} - Intercept) \quad (1)$$

where:
Slope is the change in output voltage divided by the change in input level (unit is mV/dB).
P_{IN} is the input level (unit is dBm).
Intercept is the calculated input level at which the output voltage is equal to 0 V (note that *Intercept* is an extrapolated theoretical value and not a measured value). *Intercept* has a unit of dBm.

In general, calibration is performed during equipment manufacture by applying two or more known signal levels to the input of the ADL5904 and measuring the corresponding output voltages. The calibration points must be within the linear operating range of the device.

With a two-point calibration, calculate the slope and intercept as follows:

$$Slope = (V_{RMS1} - V_{RMS2})/(P_{IN1} - P_{IN2}) \quad (2)$$

$$Intercept = P_{IN1} - (V_{RMS1}/Slope) \quad (3)$$

After the slope and intercept are calculated (and stored in some form), use the following equation to calculate an unknown input level based on the output voltage of the detector:

$$P_{IN}\,(Unknown) = (V_{RMS\,(MEASURED)}/Slope) + Intercept \quad (4)$$

The log conformance error is the difference between this straight line and the actual performance of the detector.

$$Error\ (\text{dB}) = (V_{RMS\,(MEASURED)} - V_{RMS(IDEAL)})/Slope \quad (5)$$

Use multipoint calibration to extend the measurement dynamic range further. In this case, the transfer function is segmented, with each segment having its own slope and intercept. Figure 48 shows the error plot of the same device with calibration points at −20 dBm, 0 dBm, and +10 dBm. The three-point calibration results in tighter log conformance and a slight extension of the linear operating range of the device.

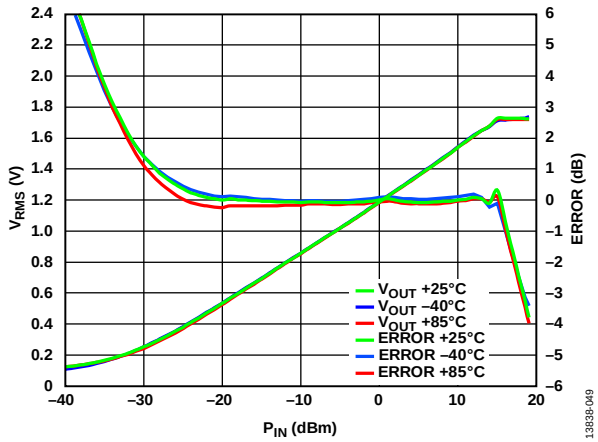


Figure 48. V_{RMS} and Log Conformance Error at 900 MHz, −40°C, +25°C, and +85°C with Log Conformance Error Calculated Based on Three-Point Calibration at −20 dBm, 0 dBm, and +10 dBm

Where three-point calibration is used, two values of slope and two values of intercept must be calculated and stored during calibration. In addition, the transition point between the two calibration regions must be recorded so that the system knows which slope/intercept pair to use. In a typical system, the output of the ADL5904 is sampled by a precision ADC. For the example in Figure 48 (calibration points at −20 dBm, 0 dBm, and +10 dBm), the ADC output code for an input power of 0 dBm is stored with the calculated slopes and intercept. When the system is in operation in the field, the code from the ADC is compared to this stored code to determine whether to use the upper or lower slope/intercept pair.

The calibration scheme for ADL5904 can be extended beyond three points. This technique can be used, for example, to linearize the response for input powers below −30 dBm. This effort, however, is less beneficial if the device is to be used over a wide temperature range. The multidevice plots (see Figure 15, Figure 19 to Figure 21, Figure 25 to Figure 27, and Figure 31) show how temperature stability becomes less predictable at low input power level.

BASIC CONNECTIONS FOR THRESHOLD DETECTION

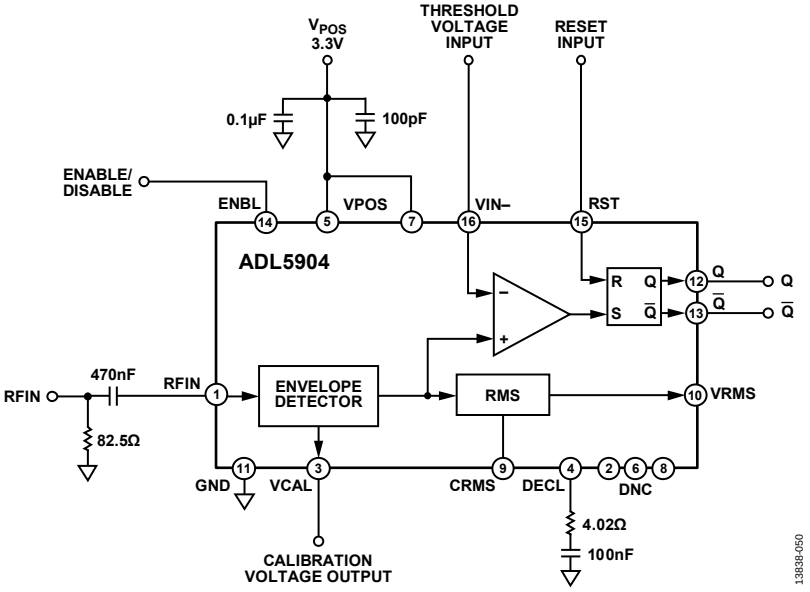


Figure 49. Basic Connections for Threshold Detection

Figure 49 shows the basic connections for operating the ADL5904 in threshold detection mode. A threshold voltage is applied to the VIN– input that corresponds to the RF power level at which the circuit trips. When the level on RFIN drives the envelope detector to an output voltage that exceeds the programmed threshold, the comparator output goes high causing the Q output to latch high and the $\overline{Q}$ output to latch low. The levels on Q and $\overline{Q}$ can be reset by setting the RST pin high (note that the RST function is level triggered, not edge triggered). Q and $\overline{Q}$ are held at low and high states respectively as long as RST is high, even if the RF input level is exceeding the programmed threshold voltage. RST must be taken low for the threshold detection circuit to reactivate.

Q AND $\overline{Q}$ RESPONSE TIME

Figure 50 shows the response of the Q output when the input power exceeds the programmed threshold by approximately 1 dB. The response time from the input power exceeding the threshold to the Q output reaching 50% of its final value is approximately 12 ns

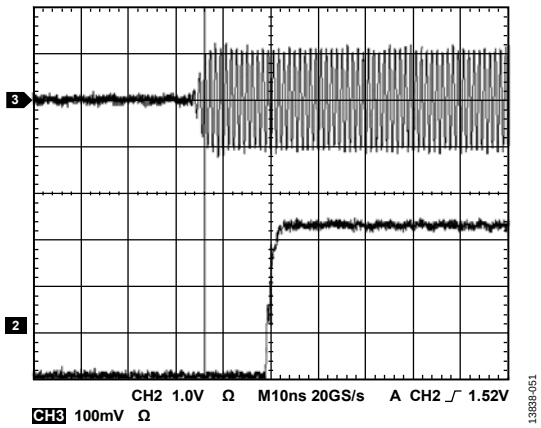


Figure 50. Q Output Response at 900 MHz, P_{IN} = Off to −9 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 1 dB)

The response time of the Q and $\overline{Q}$ outputs is somewhat dependent on the level of overdrive with higher overdrive levels, giving a slightly faster response time. Figure 51 shows the response of the Q output when the RF input level overdrives the threshold by 5 dB, which reduces the response time to approximately 12 ns. Overdrive levels beyond 5 dB tend not to reduce the response time below this level. Capacitive loading on Q and $\overline{Q}$ also affects the response time, as shown in Figure 35.

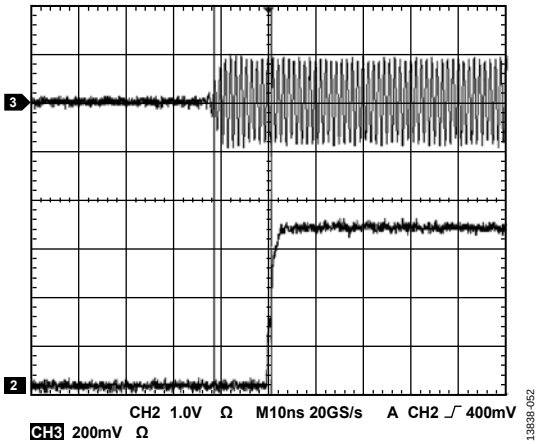


Figure 51. Q Output Response, P_{IN} = Off to −5 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 5 dB, V_{IN-} = 75 mV)

Figure 52 shows the response of the $\overline{Q}$ output, which goes low when the input threshold is exceeded. As shown in Figure 52, the response time of $\overline{Q}$ is equal to that of the Q output.

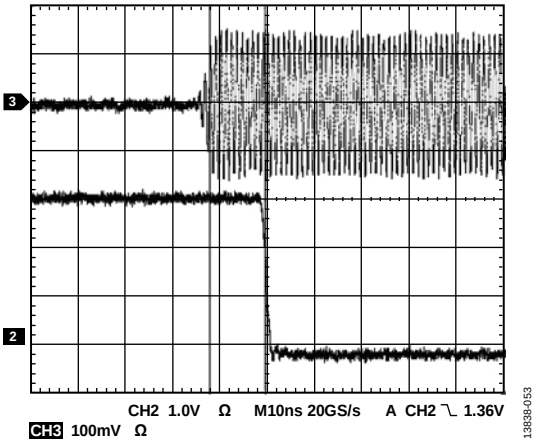


Figure 52. $\overline{Q}$ Output Response, P_{IN} = Off to −7 dBm, Overdrive Threshold Voltage Set to Trigger at −10 dBm (Overdrive Level = 3 dB)

SETTING THE V_{IN-} THRESHOLD DETECTION VOLTAGE

Figure 53 shows the typical relationship between the voltage on the VIN− pin and the resulting RF power threshold that causes Q and $\overline{Q}$ to latch high and low, respectively. This data is also presented in Table 6.

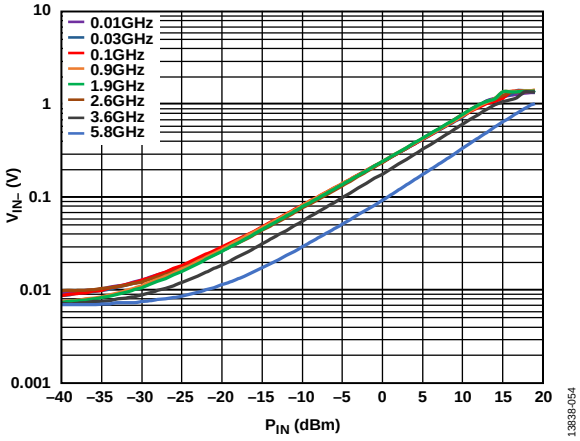


Figure 53. V_{IN-} Threshold Voltage vs. P_{IN} at Various Frequencies

Use Figure 53 and Table 6 to set the threshold voltage on the VIN− pin. However, because the relationship between the threshold voltage on VIN− and the resulting RF threshold power varies from device to device, there is an error level of up to ±2.5 dB. For example, if the voltage on VIN− is set to cause the circuit to trip when the input power exceeds 0 dBm at 900 MHz (V_{IN-} = 241 mV from Table 6), the trip point can vary from device to device by ±2.5 dB at frequencies at or above 100 MHz and +2.5 dB to −5.5 dB for frequencies below 100 MHz. In Table 6, no recommended voltages are provided for input power levels below −25 dBm from 10 MHz to 3.5 GHz and below −20 dBm at 5.8 GHz. This is as a result of the increased temperature drift at these input power levels. Likewise, from 10 MHz to 3.5 GHz, no recommended voltages are provided for input power levels above 13 dBm because, at this power level, the response of the ADL5904 starts to become more nonlinear.

To set the threshold detect level more precisely, there are two calibration options. A single-point calibration is easily accomplished by applying the threshold trip power level and then adjusting V_{IN-} until Q trips high. Initially, set V_{IN-} to a high level such as 2 V, and then assert RST high and back to low to ensure that Q is low. Next, apply the RF input threshold power level to RFIN. Then, reduce the voltage on V_{IN-} until the Q output goes high. Use this resulting voltage to set the threshold level when the equipment is in operation.

Alternatively, by measuring the voltage on the VCAL output pin with and without RF power applied, an equation can be derived that establishes a precise relationship between the V_{IN-} voltage and the associated RF input power trip point.

Within the linear operating range of the ADL5904, there is a linear relationship between VCAL − $VCAL_{OFF}$ and the input voltage on RFIN.

$$VCAL - VCAL_{OFF} = Slope \times (V_{RFIN} - Intercept) \quad (6)$$

where:
VCAL is the measured output voltage on the VCAL pin.
$VCAL_{OFF}$ is the measured output voltage on the VCAL pin with no RF input signal applied.
V_{RFIN} is the RF input power (in dBm) converted into volts rms, that is,

$$V_{RFIN} = \sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} \quad (8)$$

where:
R is the characteristic impedance (usually 50 Ω).
P_{IN} is the input power in dBm.

Rewriting the equation results in

$$V_{CAL} - V_{CALOFF} = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} - Intercept \right) \quad (9)$$

The voltage that must be applied to the VIN− pin for a particular input power is equal to (VCAL − $VCAL_{OFF}$). Therefore, Equation 9 can be rewritten as

$$VIN - = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{IN}}{10}\right)}{10^3}} - Intercept \right) \quad (10)$$

Table 6. Recommended Typical Values for Threshold Voltage (V_{IN-}) When Operating Uncalibrated[1]

Input Threshold Power (dBm)	Threshold Voltage (mV)							
	10 MHz	30 MHz	100 MHz	900 MHz	1900 MHz	2600 MHz	3500 MHz	5800 MHz
−25.0	18	18	18	17	16	17	12	N/A
−24.0	19	19	20	18	17	18	13	N/A
−23.0	21	21	22	20	19	20	14	N/A
−22.0	23	23	24	22	21	22	15	N/A
−21.0	25	25	26	25	23	24	17	N/A
−20.0	28	28	29	27	26	26	19	11
−19.0	31	31	32	31	29	29	21	12
−18.0	34	34	35	34	32	32	23	13
−17.0	37	38	39	38	36	35	25	14
−16.0	41	42	43	42	40	39	28	16
−15.0	47	47	48	47	45	44	31	17
−14.0	52	52	53	52	50	49	35	19
−13.0	58	58	59	58	56	54	39	21
−12.0	64	64	66	65	62	60	44	23
−11.0	71	72	73	72	70	68	49	26
−10.0	80	80	81	81	78	76	55	29
−9.0	88	89	90	90	87	84	61	32
−8.0	98	99	101	101	97	94	69	36
−7.0	110	111	112	112	109	105	77	40
−6.0	123	123	125	125	122	118	87	45
−5.0	137	137	139	139	136	132	98	51
−4.0	154	153	155	155	153	148	110	57
−3.0	172	172	173	173	171	167	124	64
−2.0	193	192	193	193	192	186	140	73
−1.0	214	214	216	216	215	210	158	81
0.0	240	238	239	241	241	236	177	92
1.0	269	266	268	272	270	266	200	104
2.0	300	298	300	304	303	298	226	119
3.0	336	334	336	340	341	337	255	135
4.0	376	374	377	380	383	380	289	153
5.0	421	419	421	425	431	425	327	175
6.0	472	466	471	477	485	481	370	199
7.0	529	522	528	534	543	544	419	225
8.0	592	585	591	598	611	610	474	257
9.0	664	652	663	670	688	690	537	293
10.0	743	723	742	752	774	775	608	334
11.0	858	844	830	842	871	875	684	381
12.0	939	957	927	942	976	982	774	434
13.0	1078	1072	1005	1047	1066	1061	876	495
14.0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	564
15.0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	642

[1] N/A means not applicable

Use a two-point or a three-point calibration to establish the slope and intercept values in Equation 10. The procedure for a two-point calibration is as follows:

1. With no RF input signal applied, measure the voltage on the VCAL pin ($VCAL_{OFF}$).
2. Apply an RF input power that is towards the bottom end of the RF input range ($RFIN_{LOW}$). Calculate the associated rms input voltage ($VRMS_{LOW}$) and measure the voltage on the VCAL pin ($VCAL_{LOW}$).
3. Apply an RF input power that is towards the top end of the RF input range ($RFIN_{HIGH}$). Calculate the associated rms input voltage ($VRMS_{HIGH}$) and measure the voltage on the VCAL pin ($VCAL_{HIGH}$) pin.
4. Calculate SLOPE using the following equation:

   $Slope = (VCAL_{HIGH} - VCAL_{LOW})/(VRMS_{HIGH} - VRMS_{LOW})$

5. Calculate intercept using the following equation:

   $Intercept = V_{RFIN} - (VCAL - VCAL_{OFF})/Slope$

When the slope and intercept are known, nsert them into the equation for V_{IN-}.

$$V_{IN-} = Slope \times \left(\sqrt{\frac{R \times \log^{-1}\left(\frac{P_{THRESHOLD}}{10}\right)}{10^3}} - Intercept \right) \quad (11)$$

where $P_{THRESHOLD}$ is the desired RF power level at which the circuit trips.

APPLICATIONS INFORMATION

EVALUATION BOARD SCHEMATIC AND CONFIGURATION OPTIONS

The ADL5904-EVALZ is a fully populated, 4-layer, FR4-based evaluation board. Apply a power supply of 3.3 V to the VPOS and GND test loops. To exercise the RMS detector portion of the circuit, apply the RF signal to be measured to the RFIN SMA connector. The corresponding rms output voltage is then available on the VRMS SMA connector and on the TP1 test point.

To operate the threshold detection circuitry, apply the RF signal that is being monitored again to the RFIN SMA connector. Apply the dc threshold voltage that causes the circuit to trip to the VIN_N SMA connector or to the TPVIN_N yellow test point. Reset the internal SR flip flop by pressing the RST button.

Detailed configuration options for the evaluation board are listed in Table 7.

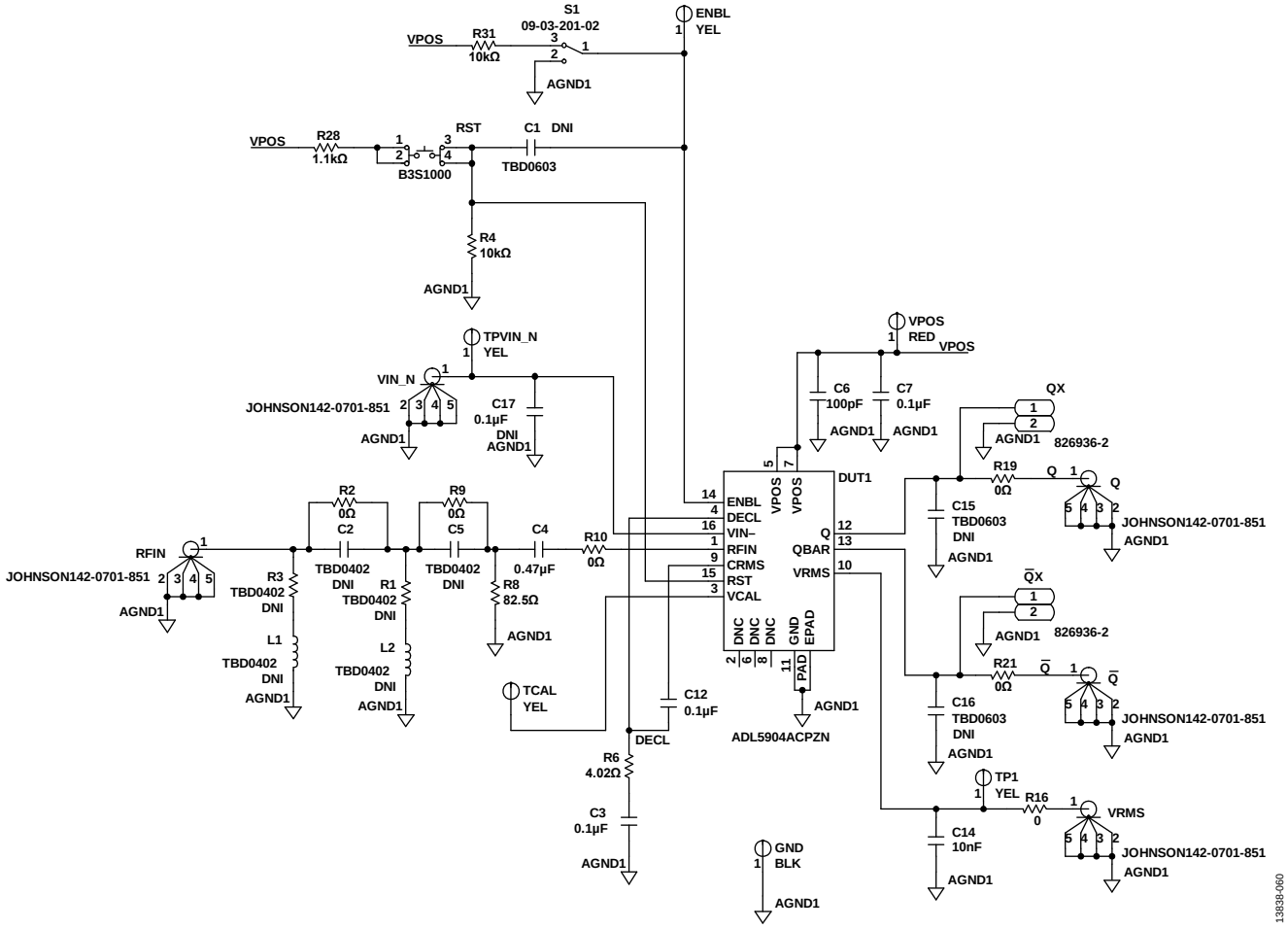
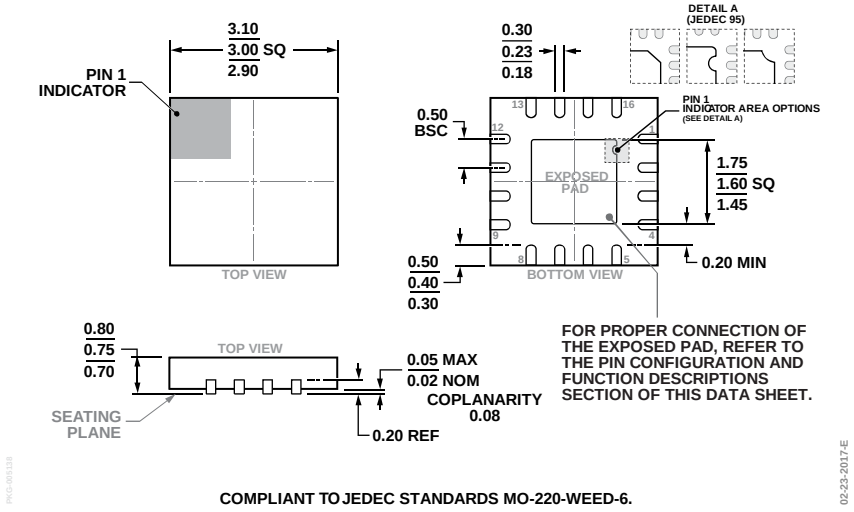


Figure 54. Evaluation Board Schematic

Table 7. Evaluation Board Configuration Options

Component	Function	Notes	Default Values
RFIN, R1, R2, R3, R8, R9, R10, L1, L2, C2, C4, C5	RF input	Apply the RF input signal to the ADL5904 to the SMA connector labeled RFIN. The ADL5904 RFIN pin (Pin 1) is dc-coupled and is not internally matched. A broadband 50 Ω match is achieved using an external 82.5 Ω shunt resistor with a 0.47 µF ac coupling capacitor placed between the shunt resistor and the RF input. An external preemphasis network can be built to improve flatness vs. frequency using the components between R8 and the RFIN SMA connector.	C4= 0.47uF (0402) R8 = 82.5 Ω (0402) R2, R9, R10 = 0 Ω (0402) R1, R3 = open (0402) L1, L2 = open (0402) C2, C5 = open (0402)
VCAL, VIN_N, TPVIN_N, C17,	VCAL threshold calibration	The output voltage from the threshold calibration pin (VCAL, Pin 3) is available on the yellow VCAL clip lead. Use the voltage on this pin to determine the correct threshold voltage that must be applied to Pin 16 (VIN−) to set a particular RF power threshold. This process includes two steps: first, measure the output voltage on the VCAL yellow clip lead with no RF signal applied to RFIN (this voltage is approximately 750 mV). Next, apply the RF input power to RFIN, which causes the circuit to trip, and again measure the voltage on the VCAL yellow clip lead. The difference between these two voltages is equal to the voltage that must be applied to VIN− during operation. This voltage can be applied either to the VIN_N SMA connector or to the TPVIN_N yellow clip lead. Use C17 to provide noise decoupling of the applied input voltage.	C17 = open (0603)
R6, C3	DECL internal decoupling node	A resistor in series with a capacitor to ground must be connected to the DECL pin (Pin 4).	C3 = 100 nF (0402) R6 = 4.02 Ω (0402)
VPOS, GND, C7, C6	Power supply interface	Apply the 3.3 V power supply for the evaluation board to the VPOS (red) and GND (black) test loops. The nominal supply decoupling consists of a 100 pF capacitor and a 0.1 µF capacitor, with the 100 pF capacitor placed closest to the VPOS pin (Pin 5).	C7 = 0.1 µF (0402), C6 = 100 pF (0402) VPOS = 3.3 V
VRMS, TP1, R16, C14	Output interface	The rms output voltage is available on the VRMS SMA connector or on the TP1 yellow clip lead.	R16 = 0 Ω (0402) C14 = 10 nF (0603)
C12	RMS averaging capacitor	Set the value of the rms averaging capacitor based on the peak to average ratio and bandwidth of the input signal and based on the desired output response time and residual output noise.	C12 = 0.1 µF (0402)
Q, $\overline{Q}$, QX, $\overline{Q}$X, R19, R21, C15, C16	Threshold detect output (Q and $\overline{Q}$)	The threshold detect flip flop outputs (Q and $\overline{Q}$) are available on the SMA connectors labeled Q and $\overline{Q}$ and on the 2-pin headers labeled QX and $\overline{Q}$X. To test the response time of Q and $\overline{Q}$, remove R19 and R21 and probe QX and $\overline{Q}$X with low capacitance FET probes.	C15 = C16 = open (0603) R19, R21 = 0 Ω (0603)
ENBL, S1, R31	Enable interface	The ADL5904 can be enabled by applying 3.3 V to the ENBL SMA connector or using the S1 switch. The enable voltage must be equal to but not greater than the 3.3 V supply voltage.	R31 = 10 kΩ (0603)
RST push-button switch, R4, C1, R28	Threshold detect reset	The threshold detect flip-flop is reset using the RST push-button switch. The RST switch is connected the V_{POS} supply voltage through a 1.1 kΩ resistor (R28). A 100 kΩ pull-down resistor (R4) is connected to the RST pin, which pulls RST low in the absence of any other stimulus. The ADL5904 normally powers up with the Q and $\overline{Q}$ outputs high and low, respectively. A reset on the power-up circuit can be implemented by installing a capacitor on C1. When the VPOS supply turns on, RST goes high momentarily before being pulled low by R4.	R4 = 10 kΩ (0603) R28 = 1.1 kΩ (0603) C1 = open (0603)
VIN_N, TPVIN_N, C17	Threshold detect level set	The voltage applied to the VIN_N SMA connector or to the TPVIN_N yellow test loop drives the inverting input of the threshold detect comparator (VIN−) and thereby defines the RF power level that trips the threshold detect comparator and flip flop. The threshold detect voltage can be optionally decoupled using C17.	C17 = open (0603)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 55. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5904ACPZN-R7	−40°C to +105°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-22	Q24	3000
ADL5904-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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