EL1883

Sync Separator with Horizontal Output

FN7010
Rev 2.00
April 24, 2006

The EL1883 video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input and also in the presence of Macrovision pulses. It provides composite sync, vertical sync, burst/back porch timing, and horizontal outputs. Fixed 70mV sync tip slicing provides sync edge detection when the video input level is between $0.5V_{P-P}$ and $2V_{P-P}$ (sync tip amplitude 143mV to 572mV). A single external resistor sets all internal timing to adjust for various video standards. The composite sync output follows video in sync pulses and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The horizontal output gives horizontal timing with pre/post equalizing pulses.

The EL1883 is available in an 8-pin SO package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL1883IS	1883IS	-	8-Pin SO	MDP0027
EL1883IS-T7	1883IS	7”	8-Pin SO	MDP0027
EL1883IS-T13	1883IS	13”	8-Pin SO	MDP0027
EL1883ISZ (See Note)	1883ISZ	-	8-Pin SO (Pb-free)	MDP0027
EL1883ISZ-T7 (See Note)	1883ISZ	7”	8-Pin SO (Pb-free)	MDP0027
EL1883ISZ-T13 (See Note)	1883ISZ	13”	8-Pin SO (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Fixed 70mV slicing of video input levels from $0.5V_{P-P}$ to $2V_{P-P}$
- Low supply current - 1.5mA typ.
- Single 3V to 5V supply
- Composite sync output
- Vertical output
- Horizontal output
- Burst/back porch output
- Macrovision compatible
- Available in 8-pin SO package
- Pb-Free plus anneal available (RoHS compliant)

Applications

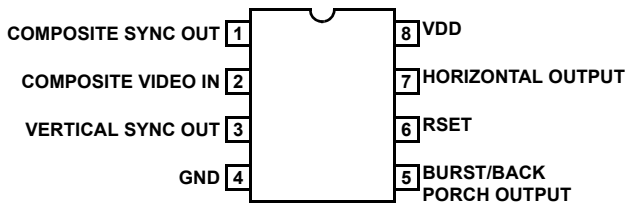
- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Demo Board

- A dedicated demo board is available

Pinout

EL1883
(8-PIN SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply 7V
Pin Voltages . . . . . -0.5V to V_{CC} +0.5V
Operating Ambient Temperature Range . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .150°C
Storage Temperature . . . . . .-65°C to +150°C
Power Dissipation 400mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_{DD} = 3.3V, T_A = 25°C, R_{SET} = 681kΩ, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3	mA
Clamp Voltage	Pin 2, I_{LOAD} = -100µA	1.35	1.5	1.65	V
Clamp Discharge Current	Pin 2 = 2V	6	12	16	µA
Clamp Charge Current	Pin 2 = 1V	-0.85	-0.65	-0.45	mA
R_{SET} Pin Reference Voltage	Pin 6	1.1	1.22	1.35	V
V_{OL} Output Low Voltage	I_{OL} = 1.6mA		0.24	0.5	V
V_{OH} Output High Voltage	I_{OH} = -40µA	3	3.2		V
	I_{OH} = -1.6mA	2.5	3.0		V

Dynamic Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Comp Sync Prop Delay, t_{CS}	See Figure 13		35	75	ns
Horizontal Sync Delay, t_{HS}			40	80	ns
Horizontal Sync Width		3.8	5.2	6.2	µs
Vertical Sync Width, t_{VS}	Normal or Default Trigger, 50%-50%	190	230	300	µs
Vertical Sync Default Delay, t_{VSD}	See Figure 14	35	62	85	µs
Burst/Back Porch Delay, t_{BD}	See Figure 13	120	200	300	ns
Burst/Back Porch Width, t_B	See Figure 13	2.5	3.5	4.5	µs
Input Dynamic Range	Video Input Amplitude to Maintain Slice Level Spec, V_{DD} = 5V	0.5		2	V_{P-P}
Slice Level	V_{SLICE} above V_{CLAMP}	50	70	90	mV

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	Composite Sync Out	Composite sync pulse output; sync pulses start on a falling edge and end on a rising edge
2	Composite Video In	AC coupled composite video input; sync tip must be at the lowest potential (positive picture phase)
3	Vertical Sync Out	Vertical sync pulse output; the falling edge of vert sync is the start of the vertical period
4	GND	Supply ground
5	Burst/Back Porch Output	Burst/back porch output; low during burst portion of composite video
6	RSET (Note)	An external resistor to ground sets all internal timing; a 681k 1% resistor will provide correct timing for NTSC signals
7	Horizontal Output	Horizontal output; falling edge active
8	VDD 5V	Positive supply (5V)

NOTE: R_{SET} must be a 1% resistor

Typical Performance Curves

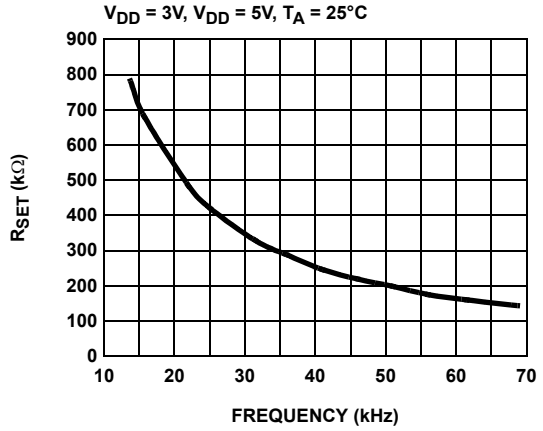


FIGURE 1. R_{SET} vs HORIZONTAL FREQUENCY

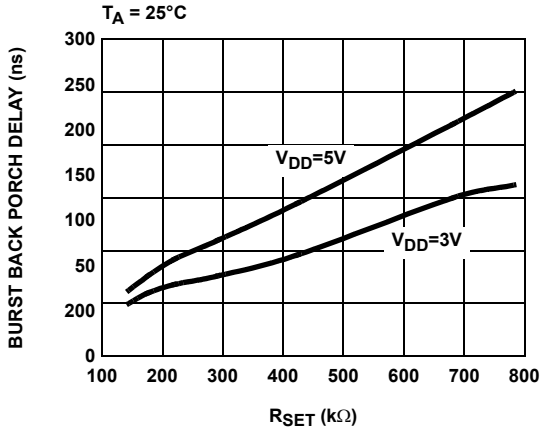


FIGURE 2. BURST/BACK PORCH DELAY vs R_{SET}

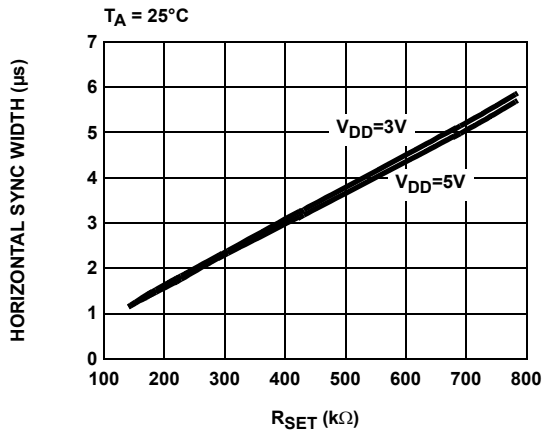


FIGURE 3. HORIZONTAL SYNC WIDTH vs R_{SET}

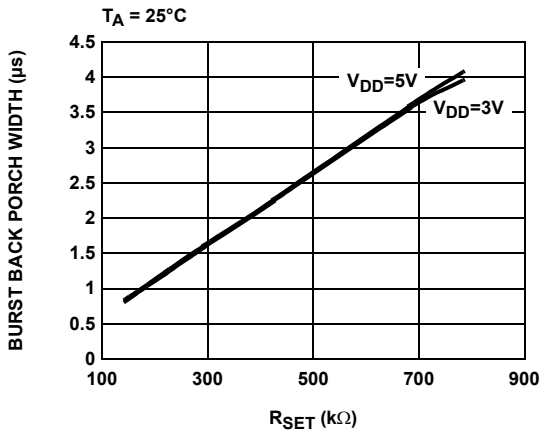


FIGURE 4. BURST/BACK PORCH WIDTH vs R_{SET}

Typical Performance Curves (Continued)

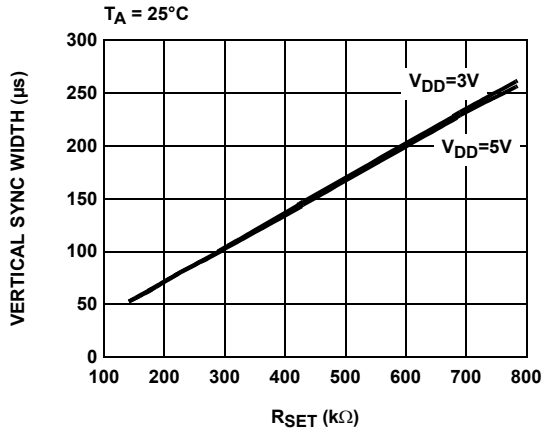


FIGURE 5. VERTICAL SYNC WIDTH vs R_{SET}

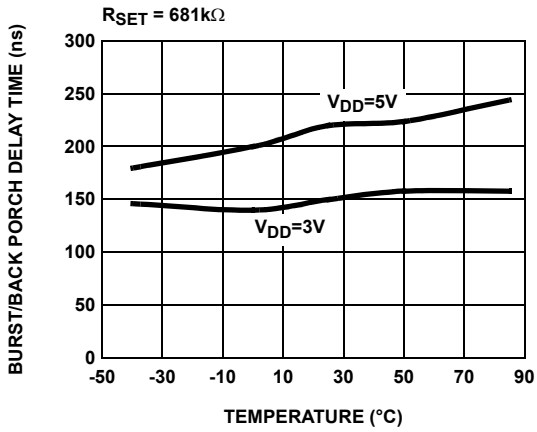


FIGURE 6. BURST/BACK PORCH DELAY vs TEMPERATURE

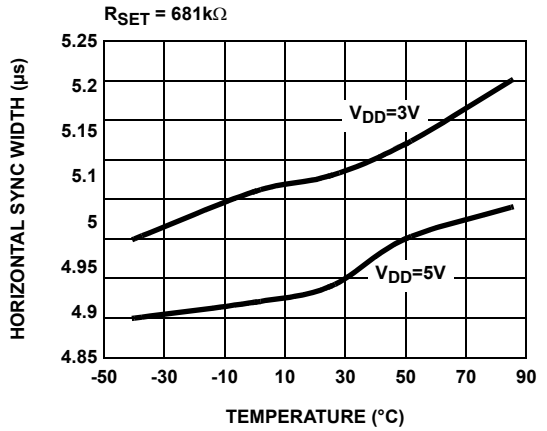


FIGURE 7. HORIZONTAL SYNC WIDTH vs TEMPERATURE

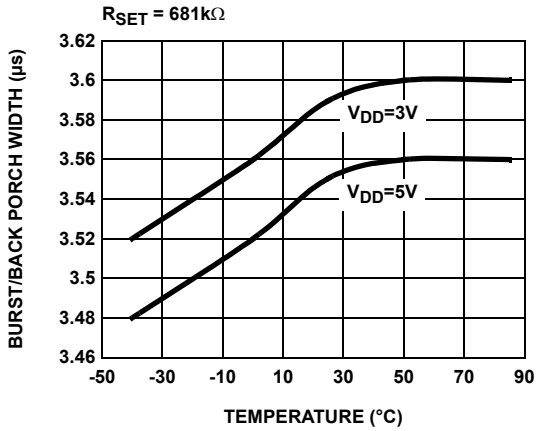


FIGURE 8. BURST/BACK PORCH WIDTH vs TEMPERATURE

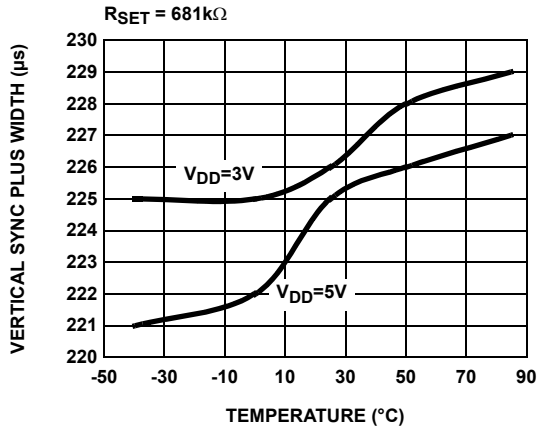


FIGURE 9. VERTICAL SYNC PULSE WIDTH vs TEMPERATURE

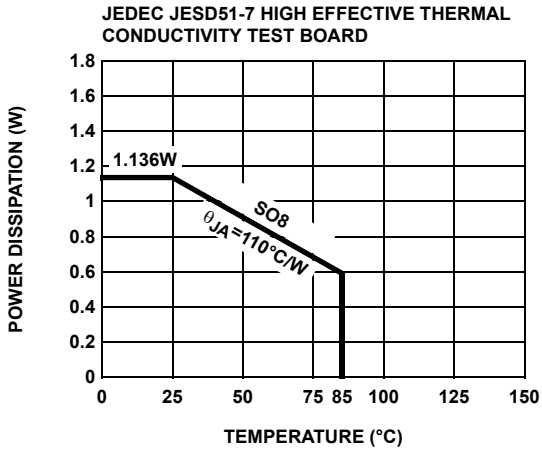


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

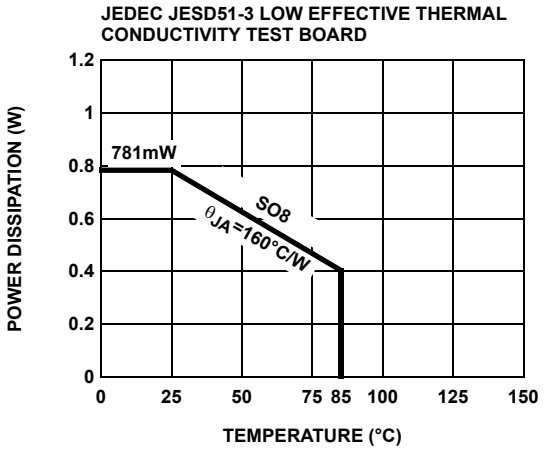


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

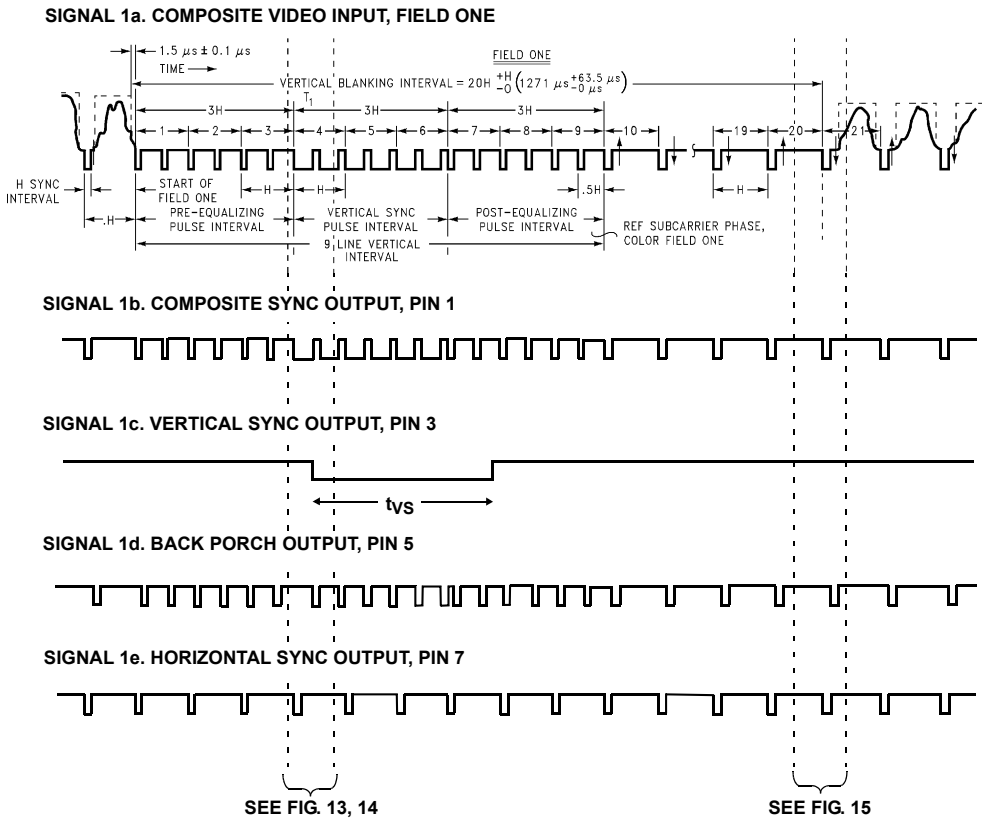


FIGURE 12. TIMING DIAGRAM

NOTES:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

e. Horizontal sync output produces the true “H” pulses of nominal width of 5µs. It has the same delay as the composite sync.

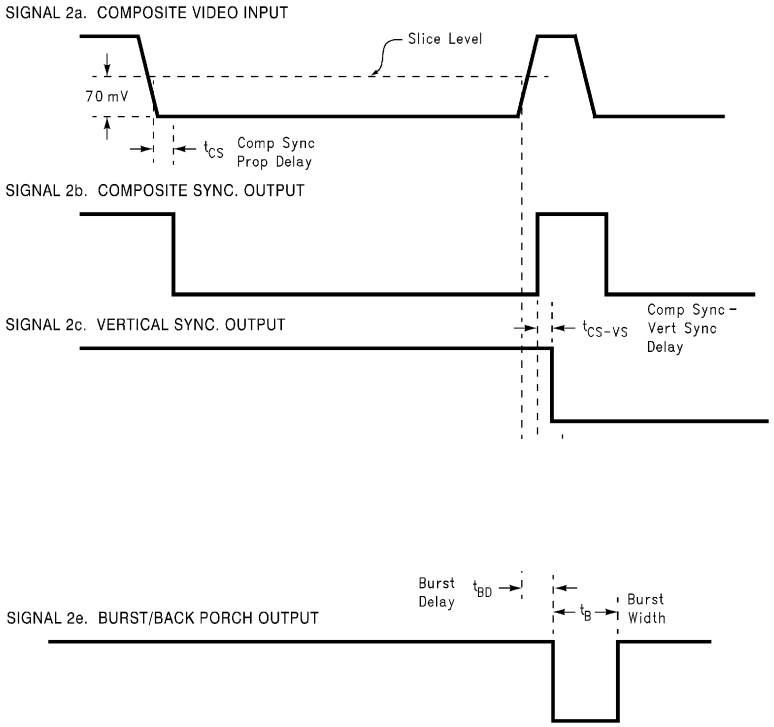


FIGURE 13. STANDARD VERTICAL TIMING

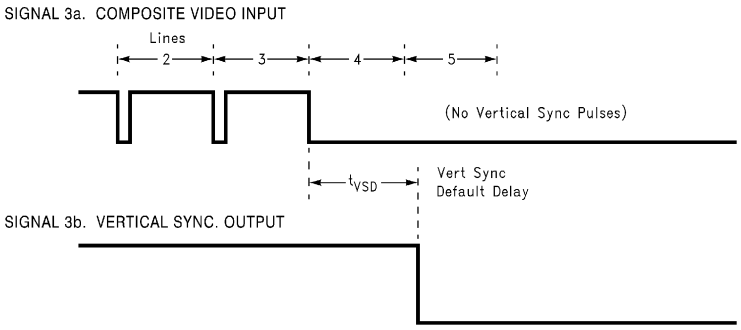


FIGURE 14. NON-STANDARD VERTICAL TIMING

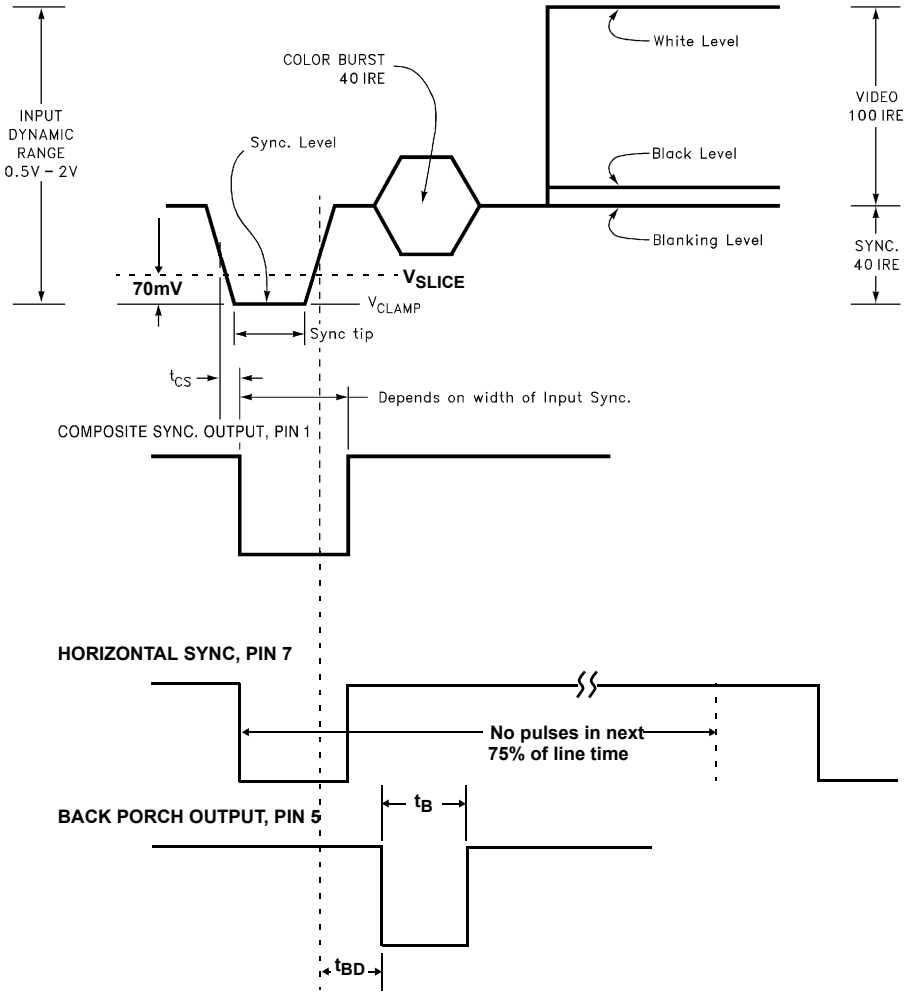


FIGURE 15. NON-STANDARD VERTICAL TIMING

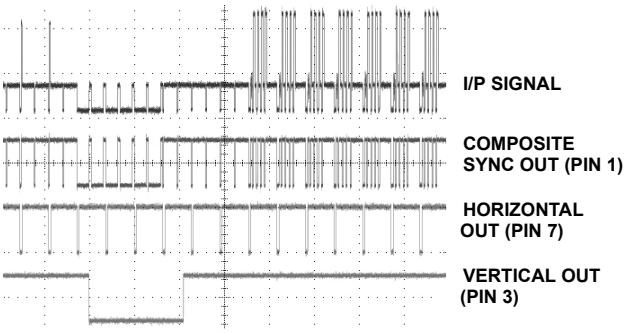


FIGURE 16. EXAMPLE OF EL1883 WITH NTSC SIGNAL THAT INCLUDES MACROVISION COPY PROTECTION (R_{SET}=681kΩ)

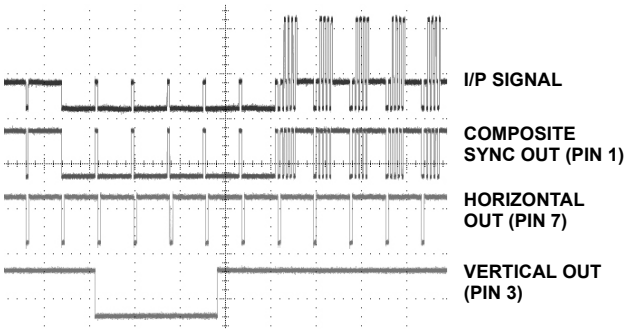


FIGURE 17. EXAMPLE OF EL1883 WITH 480p SIGNAL THAT INCLUDES MACROVISION COPY PROTECTION (R_{SET}=310kΩ)

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to Video In pin 2 via C1, nominally 0.1µF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1mA. A clamp discharge current of about 10µA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period - sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73kHz, and a sync tip width of 4.7µs. This gives a period of 63.6µs and a time T = 58.9µs. The droop voltage will then be V = 5.9mV. This is less than 2% of a nominal sync tip amplitude of 286mV. The charge represented by this droop is replaced in a time given by T = CV/I, where I = clamp charge current = 1mA. Here T = 590ns, about 12% of the sync pulse width of 4.7µs. It is important to choose C1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Composite Sync

The Composite Sync output is simply a reproduction of the input signal with the active video removed. The sync tip of the Composite video signal is clamped to 1.5V at pin 2 and then slices at 70mV above the sync tip reference. The output signal is buffered out to pin 1. With loss of the input signal, the Composite Sync output is held low.

Burst

A low-going burst pulse follows each rising edge of sync, and lasts approximately 3.5µs for an R_{SET} of 681kΩ. With loss of the input signal, the Back Porch output is held high.

Vertical Sync

A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1883 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60µS after the last falling edge of the vertical equalizing phase for R_{SET} = 681kΩ. With loss of the input signal, the vertical output is held low.

Horizontal Sync

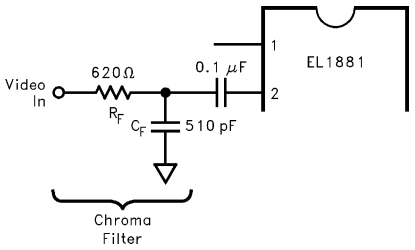
The Horizontal circuit senses the composite sync edges and produces the true horizontal pulses of nominal width 5.2µs with R_{SET} = 681kΩ. The leading edge is triggered from the leading edge of the input H sync, with the same propagation delay as composite sync. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H line eliminator circuit. This is a circuit that inhibits horizontal output pulses until 75% of the line time is reached, then the horizontal output operation is enabled again. Any signals present on the I/P signal after the true H sync will be ignored, thus the horizontal output will not be affected by MacroVision copy protection. With loss of the input signal, the Horizontal Sync output is held high.

R_{SET}

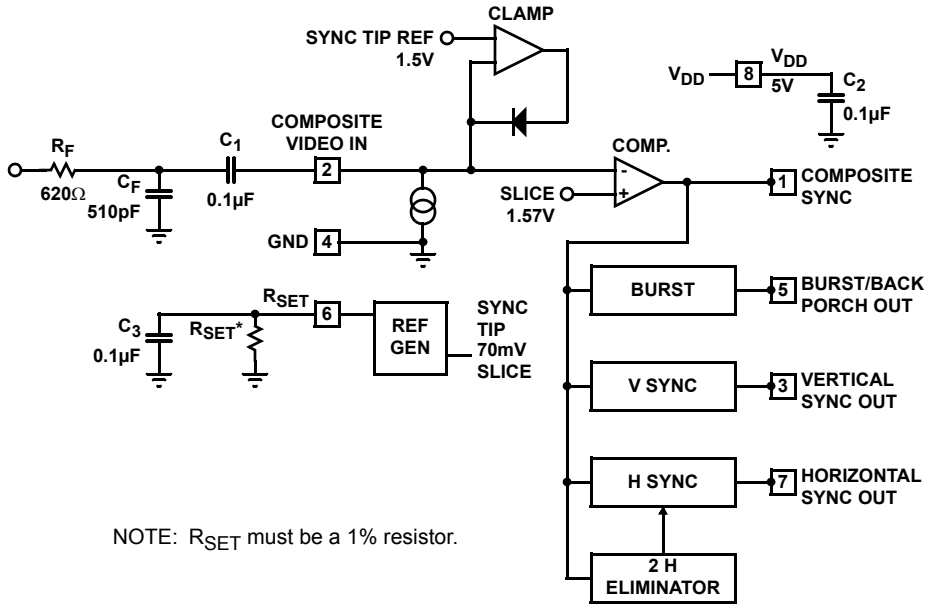
An external R_{SET} resistor, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in the figure below. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500pF, which gives a single pole roll-off frequency of about 500kHz. This sufficiently attenuates the 3.58MHz (NTSC) or 4.43MHz (PAL) color burst signal, yet passes the approximately 15kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from the composite input to the outputs.



Simplified Block Diagram



NOTE: R_{SET} must be a 1% resistor.