

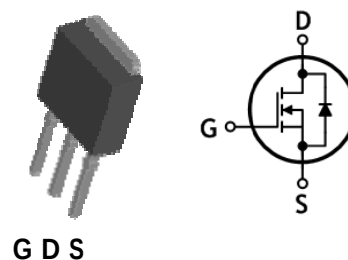
SWITCHING REGULATOR APPLICATION

Features

- Drain-Source breakdown voltage: $BV_{DSS}=600V$ (Min.)
- Low gate charge: $Q_g=3.9nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=11.5\Omega$ (Max.)
- 100% avalanche tested
- RoHS compliant device

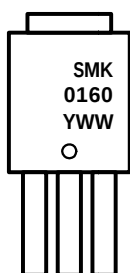
Ordering Information

Part Number	Marking	Package
SMK0160IS	SMK0160	I-PAK (Short Lead)



I-PAK

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 -. Y: Year Code
 -. WW: Week Code

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) *	I_D	$T_c=25^\circ C$	1
		$T_c=100^\circ C$	0.77
Drain current (Pulsed) *	I_{DM}	4	A
Single pulsed avalanche energy (Note 2)	E_{AS}	49	mJ
Repetitive avalanche current (Note 1)	I_{AR}	1	A
Repetitive avalanche energy (Note 1)	E_{AR}	2.5	mJ
Power dissipation	P_D	28	W
Junction temperature	T_J	150	$^\circ C$
Storage temperature range	T_{stg}	-55-150	$^\circ C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 4.46	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=0.5\text{A}$	-	9.3	11.5	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=0.5\text{A}$	-	0.32	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	131	164	pF
Output capacitance	C_{oss}		-	19.4	24.3	
Reverse transfer capacitance	C_{rss}		-	3.4	4.3	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=300\text{V}$, $I_D=1\text{A}$, $R_G=25\Omega$	-	5.5	-	ns
Rise time (Note 3,4)	t_r		-	5	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	13	-	
Fall time (Note 3,4)	t_f		-	28	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=1\text{A}$	-	3.9	4.9	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	1.7	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	0.85	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	1.0	A
Source current (Pulsed)	I_{SM}		-	-	4.0	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=1\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=1\text{A}$, $V_{GS}=0\text{V}$ $di_F/dt=100\text{A}/\mu\text{s}$	-	190	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	0.53	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=90\text{mH}$, $I_{AS}=1\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curves

Fig. 1 $I_D - V_{DS}$

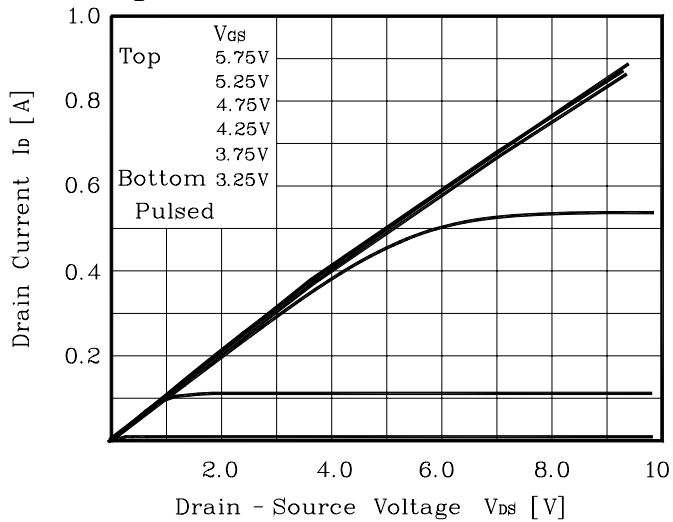


Fig. 2 $I_D - V_{GS}$

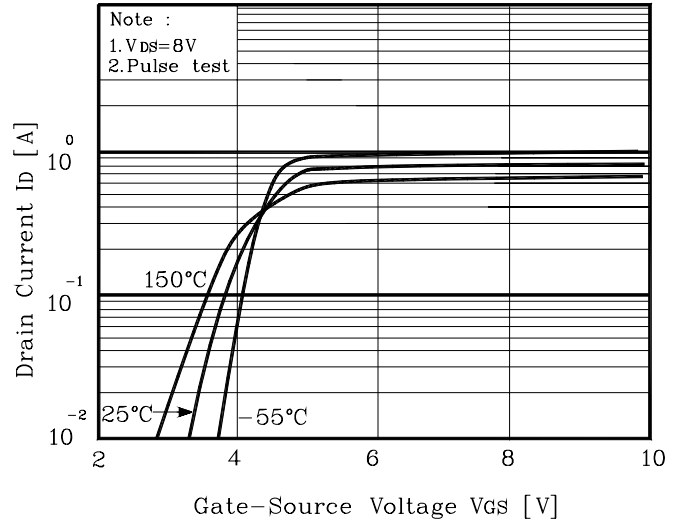


Fig. 3 $R_{DS(on)} - I_D$

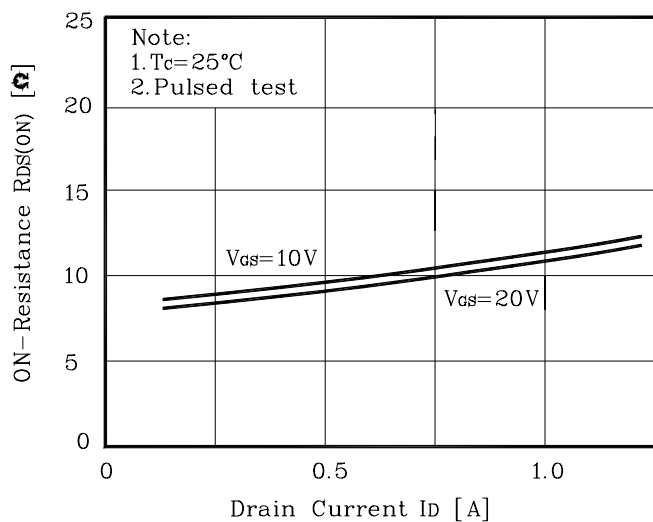


Fig. 4 $I_S - V_{SD}$

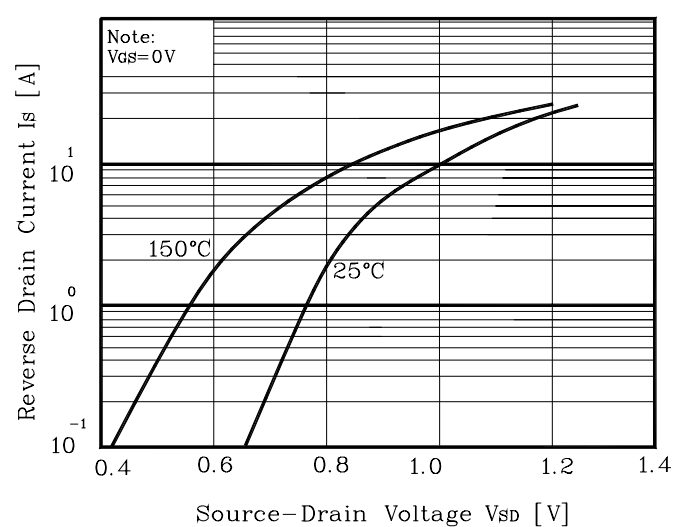


Fig. 5 Capacitance - V_{DS}

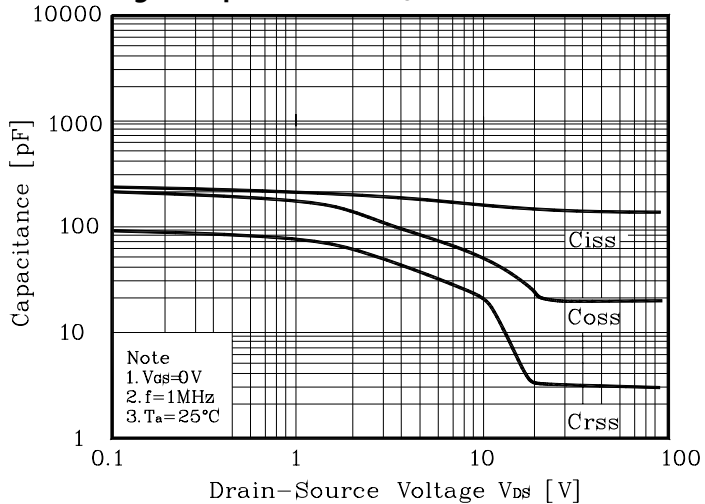


Fig. 6 $V_{GS} - Q_G$

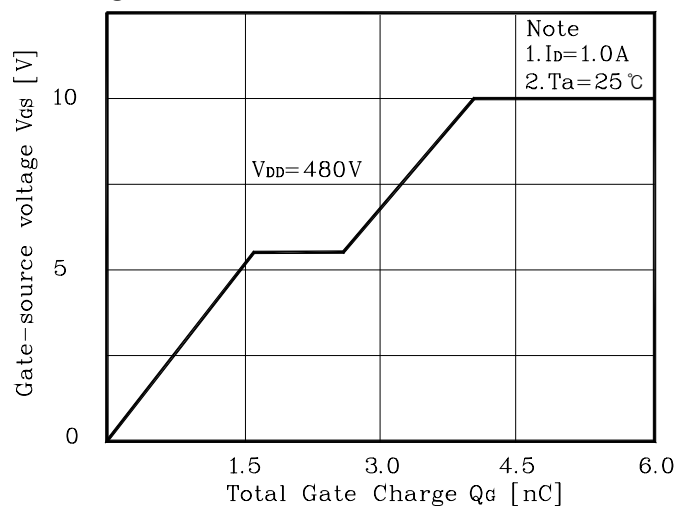


Fig. 7 $V_{DSS} - T_J$

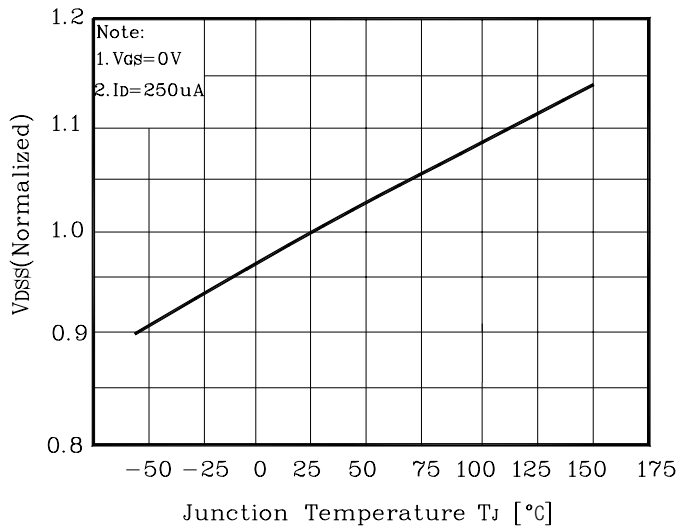


Fig. 8 $R_{DS(on)} - T_J$

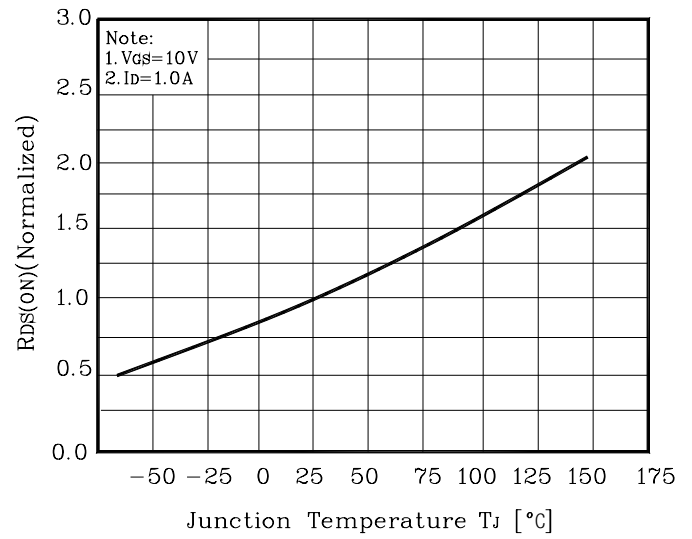


Fig. 9 $I_D - T_a$

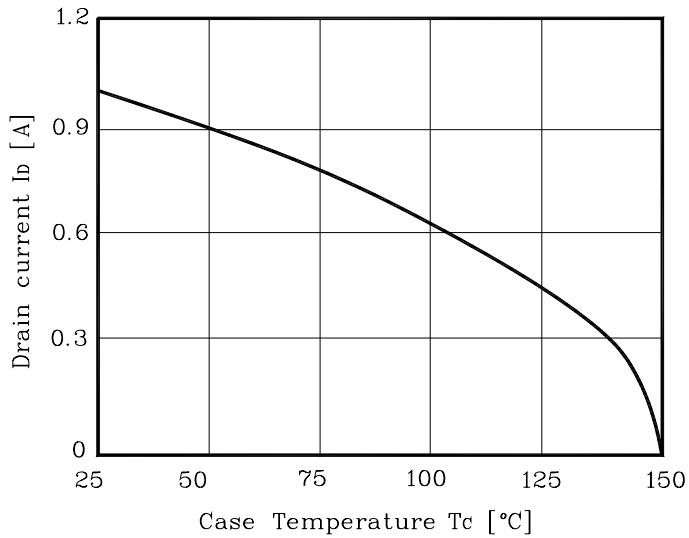


Fig. 10 Safe Operating Area

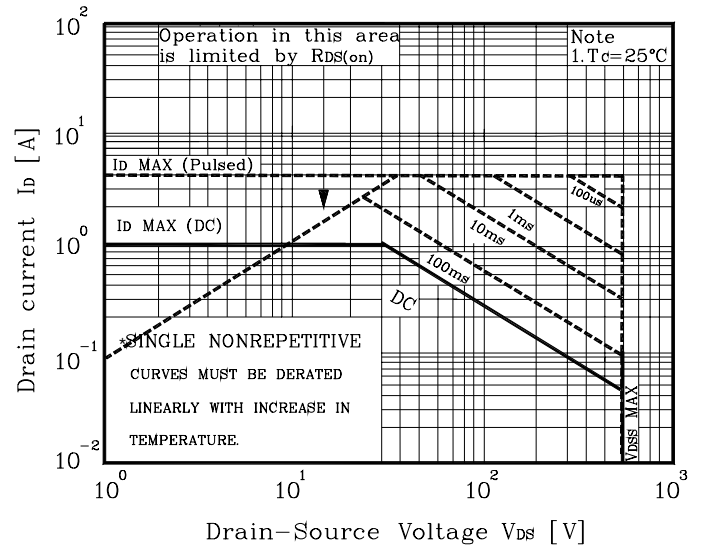


Fig. 11 Gate Charge Test Circuit & Waveform

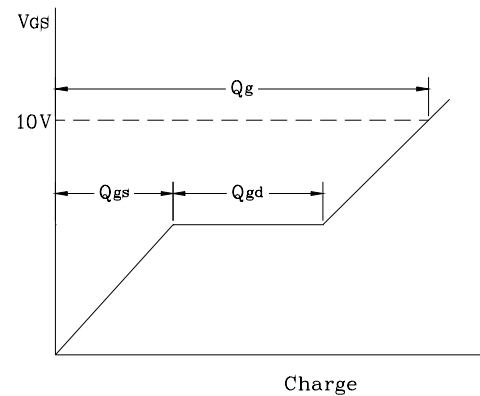
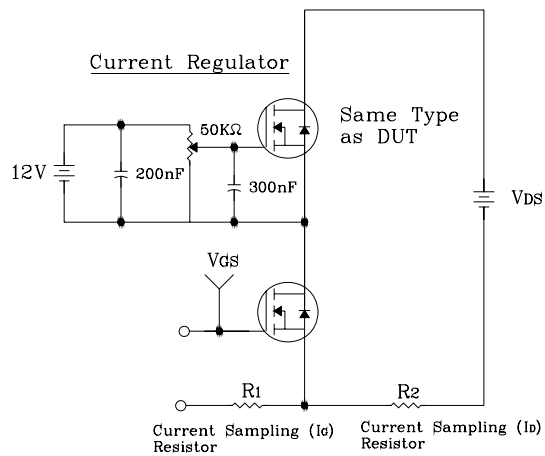


Fig. 12 Resistive Switching Test Circuit & Waveform

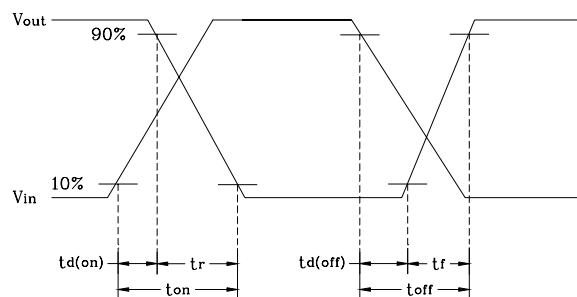
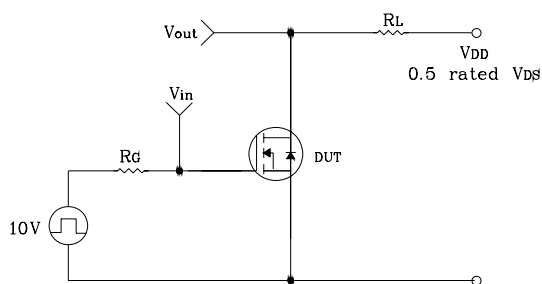


Fig. 13 E_{AS} Test Circuit & Waveform

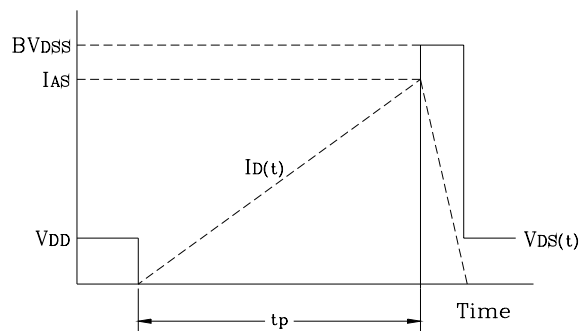
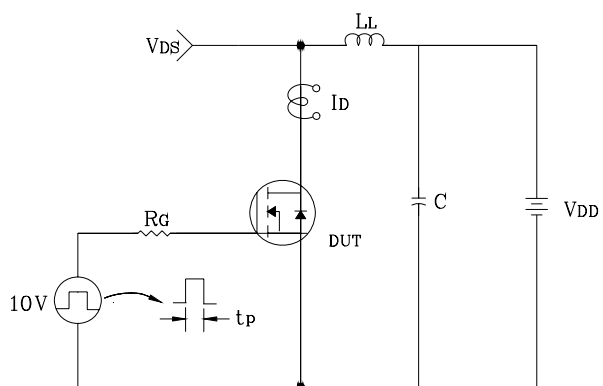
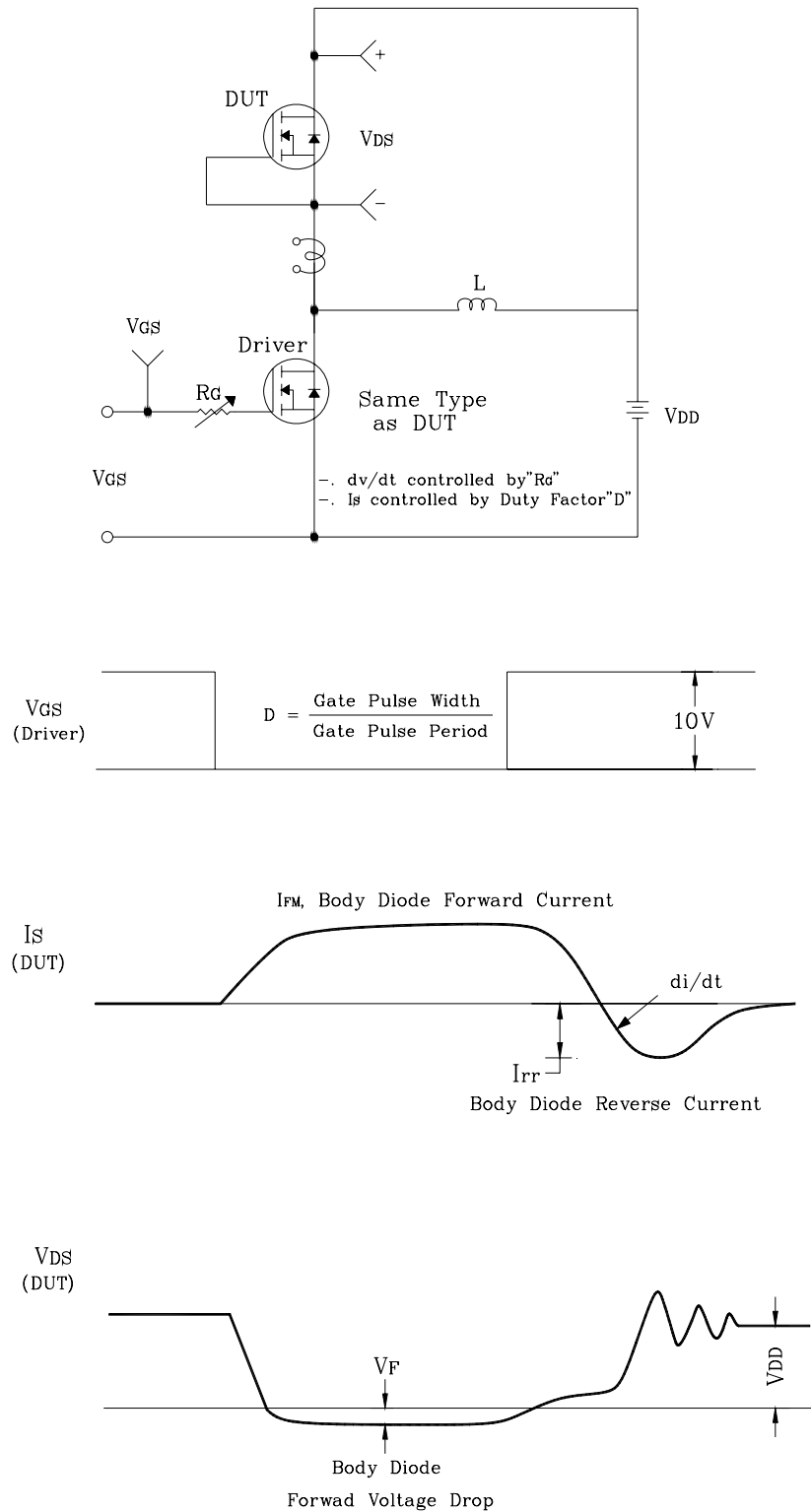
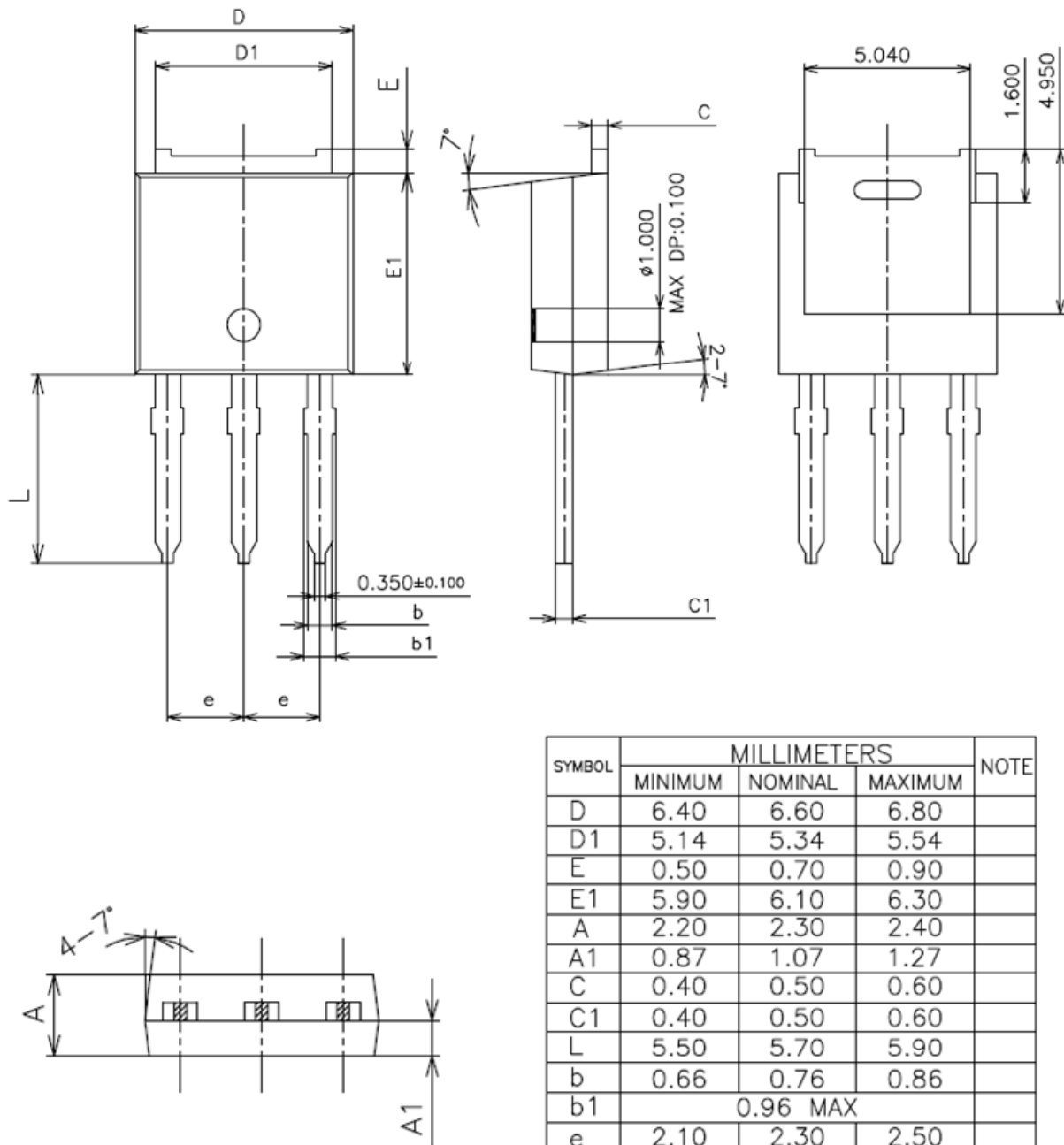


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



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