CMOS Static RAM
1 Meg (128K x 8-Bit)

IDT71024S

Features

- **128K x 8 advanced high-speed CMOS static RAM**
- **Commercial (0°C to +70°C), Industrial (–40°C to +85°C)**
- **Equal access and cycle times**
  - *Commercial and Industrial: 12/15/20ns*
- **Two Chip Selects plus one Output Enable pin**
- **Bidirectional inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
- **Available in 300 and 400 mil Plastic SOJ.**

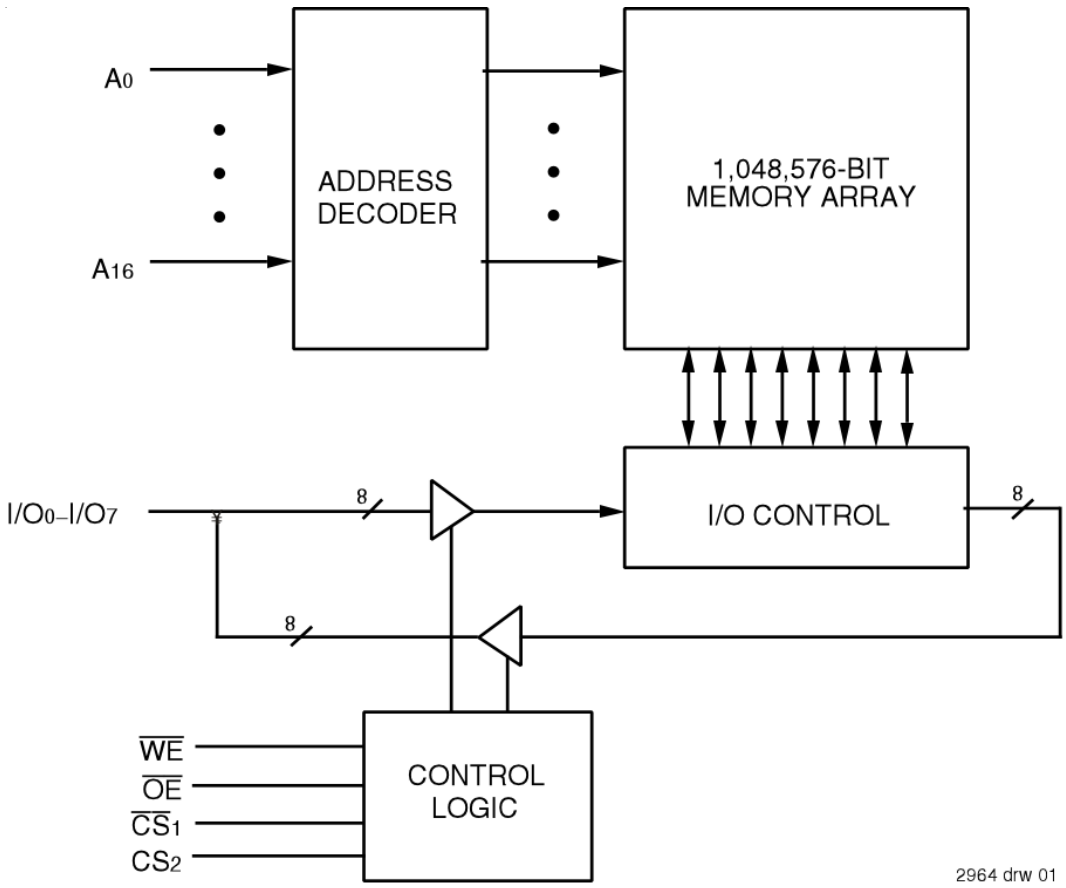
Description

The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible, and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

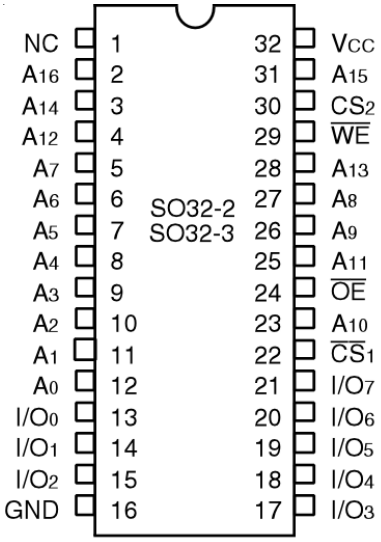
The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ and 32-pin 400 mil Plastic SOJ.

Functional Block Diagram



FEBRUARY 2013

Pin Configuration



2964 drw 02

SOJ
Top View

Truth Table(1,3)

Inputs				I/O	Function
$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$		
X	H	X	X	High-Z	Deselected – Standby (I_{SB})
X	V_{HC}(2)	X	X	High-Z	Deselected – Standby (I_{SB1})
X	X	L	X	High-Z	Deselected – Standby (I_{SB})
X	X	V_{LC}(2)	X	High-Z	Deselected – Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	$DATA_{OUT}$	Read Data
L	L	H	X	$DATA_{IN}$	Write Data

2964 tbl 01

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 0.5V
Industrial	–40°C to +85°C	0V	5.0V ± 0.5V

2964 tbl 05

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

2964 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

2964 tbl 03

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2964 tbl 04

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC Electrical Characteristics

(V_{CC} = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2964 tbl 06

DC Electrical Characteristics(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameters	71024S12		71024S15		71024S20		Unit
		Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Dynamic Operating Current, $CS_2 \geq V_{IH}$ and $\overline{CS_1} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	160	160	155	155	140	140	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS_1} \geq V_{IH}$ or $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f=f_{MAX}(2)	40	40	40	40	40	40	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS_1} \geq V_{HC}$ or $CS_2 \leq V_{LC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	10	10	10	10	10	10	mA

2964 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 08

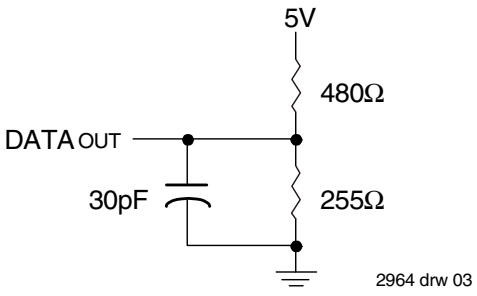
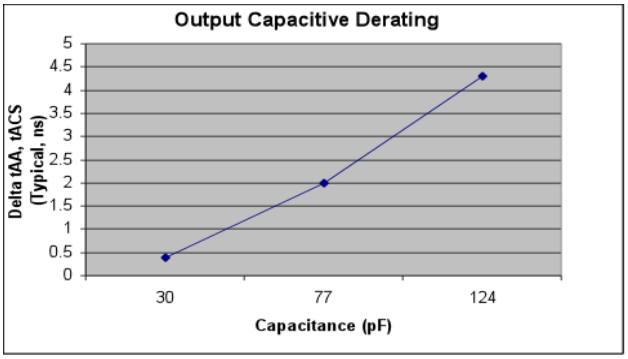


Figure 1. AC Test Load



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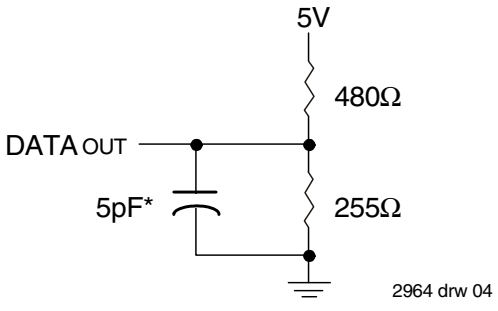


*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC Electrical Characteristics

(Vcc = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

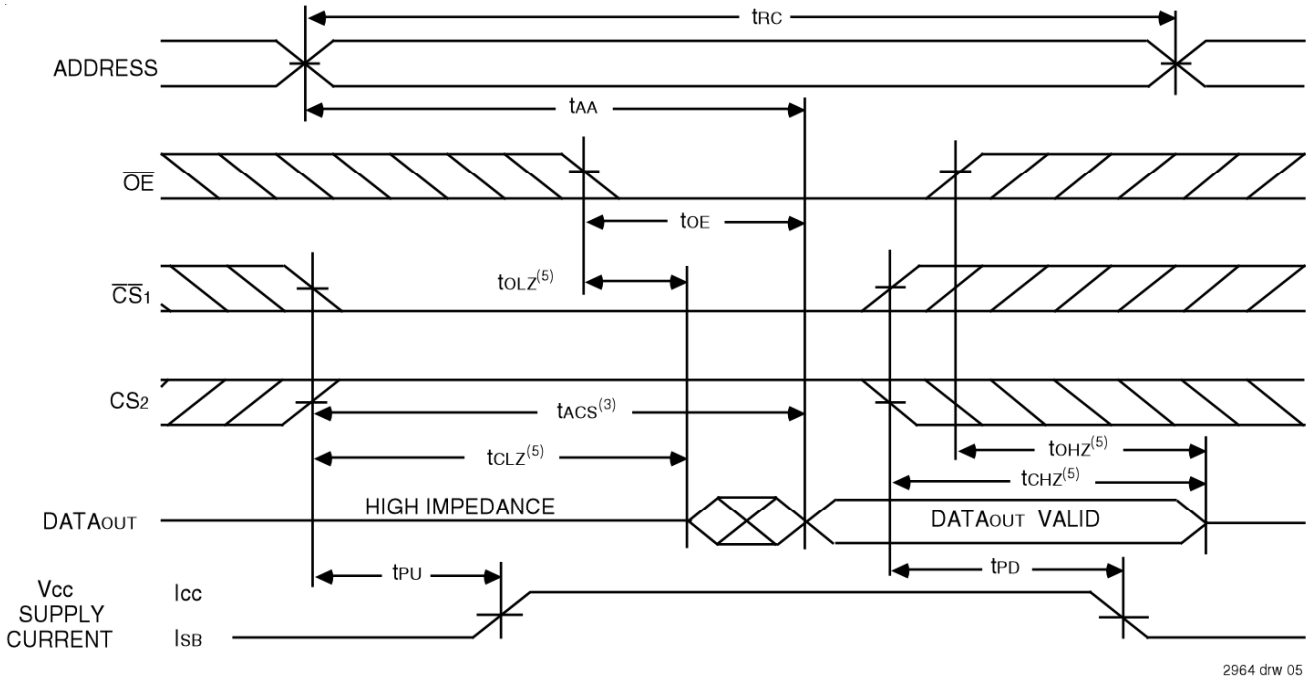
Symbol	Parameter	71024S12		71024S15		71024S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	12	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	12	—	15	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	3	—	3	—	4	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

2964 tbl 09

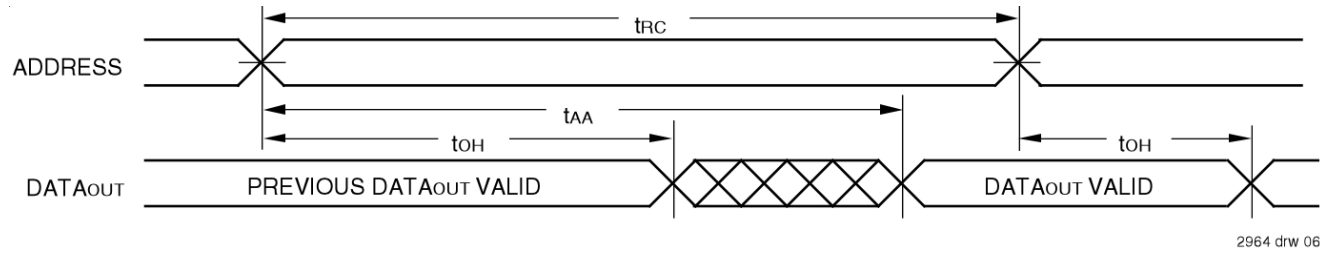
NOTE:

1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1(1)

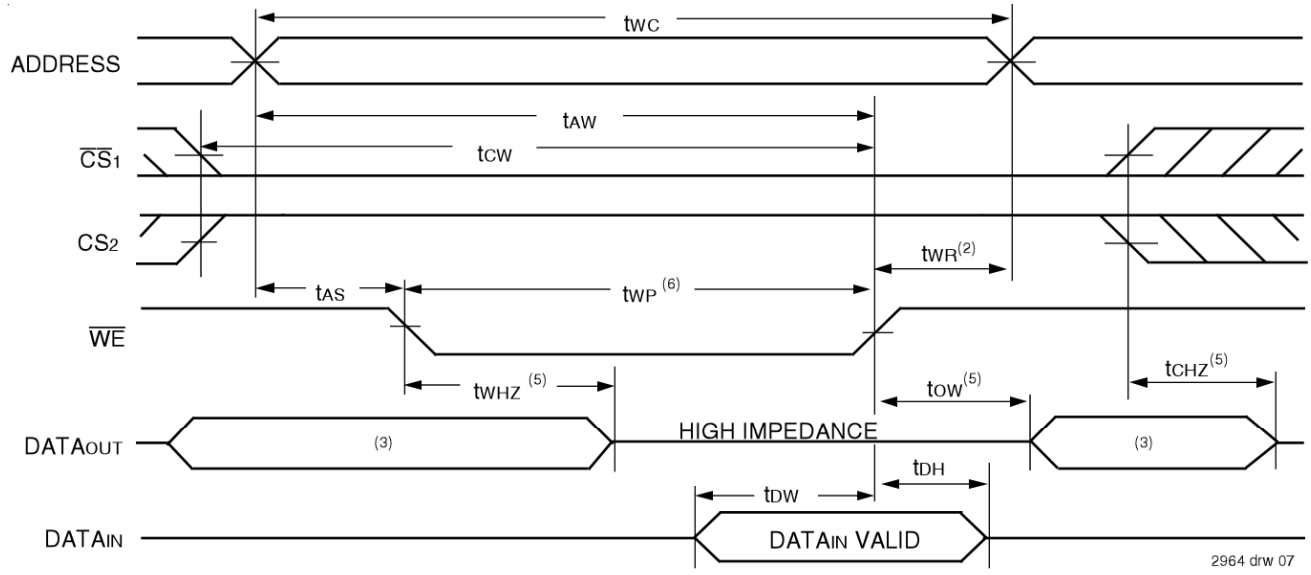


Timing Waveform of Read Cycle No. 2(1,2,4)

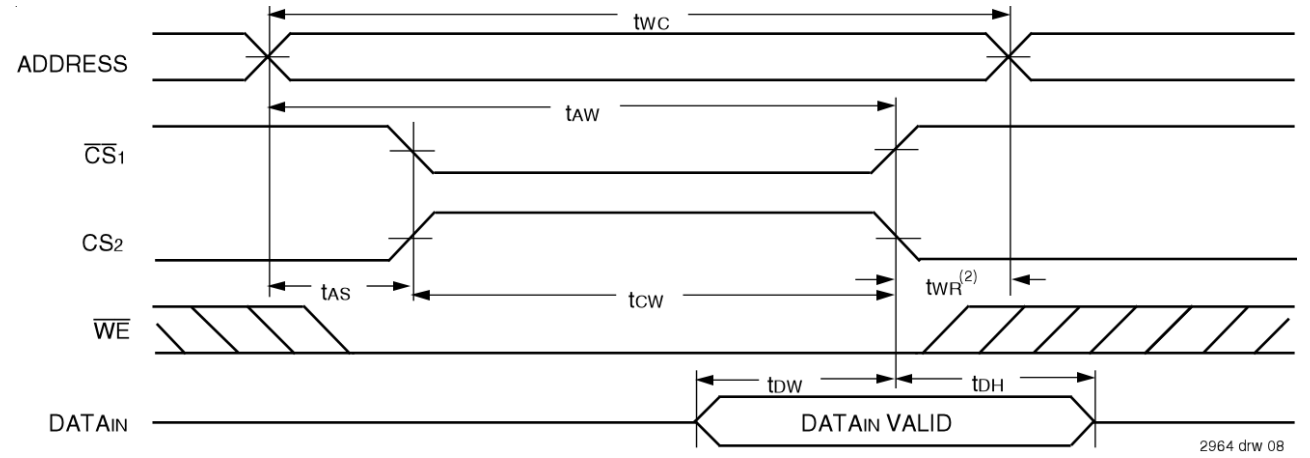


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ is LOW, CS_2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS_1}$ transition LOW and CS_2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,4,6)



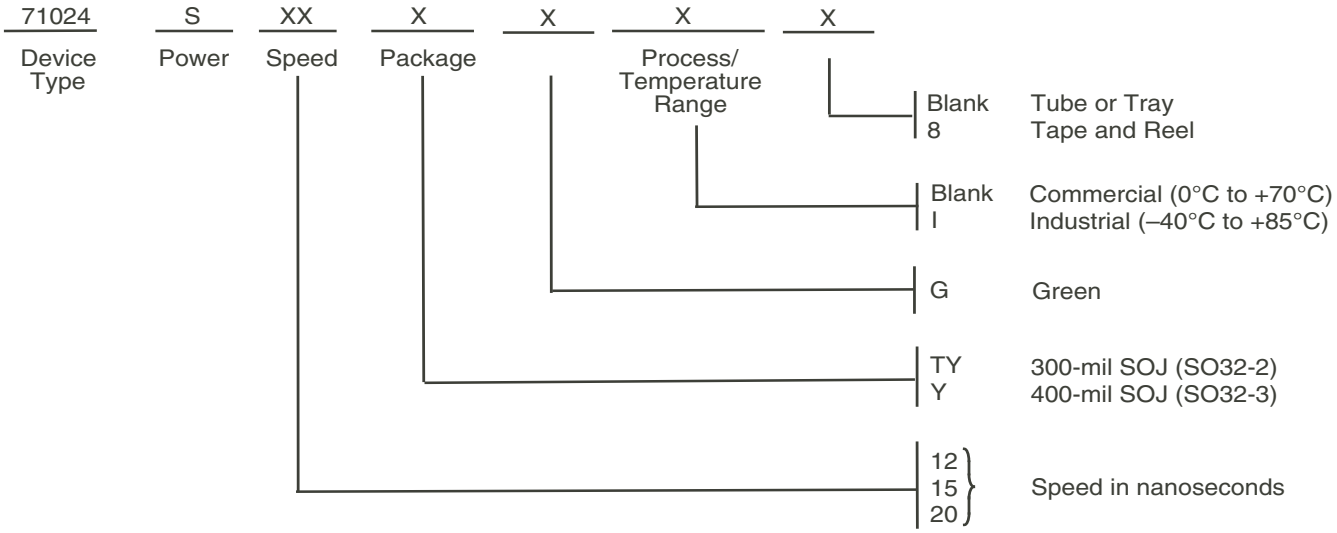
Timing Waveform of Write Cycle No. 2 ($\overline{CS}_1$ AND CS_2 Controlled Timing)(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}_1$, HIGH CS_2, and a LOW $\overline{WE}$.
2. t_{WR} is measured from the earlier of either $\overline{CS}_1$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}_1$ LOW transition or the CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}_1$ and CS_2 must both be active during the t_{CW} write period.
5. Transition is measured ±200mV from steady state.
6. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.

Ordering Information



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Datasheet Document History

9/30/99		Updated to new format
	Pg. 1, 3, 4, 7	Added 12ns industrial speed grade offering
	Pg. 1–4, 7	Removed military temperature offerings Removed 17ns and 25ns speed grades
	Pg. 3	Revised I_{CC} and I_{SB1} for 15ns and 20ns industrial speed grades
	Pg. 6	Removed Note 1, reordered notes and footnotes
	Pg. 8	Added Datasheet Document History
1/6/2000	Pg. 4	Changed t_{WP}(min) for 12ns speed grade from 10ns to 8ns.
2/18/00	Pg. 3	Revised Icc and I_{SB} for Industrial Temperature offerings to meet commercial specifications
3/14/00	Pg. 3	Revised I_{SB} to accommodate speed functionality
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
01/30/04	Pg. 7	Added "Restricted hazardous substance device" to the ordering information.
05/22/06	Pg.3	Added drawing Output Capacitive Derating drawing.
02/13/07	Pg.7	Added M generation die step to data sheet ordering information.
08/13/09	Pg.2	Corrected note reference.
02/05/13	Pg.1	Removed /MS from datasheet header. Removed IDT's reference to fabrication.
	Pg.7	Updated ordering information by adding Tape and Reel, updated Restricted Hazardous Substance Device wording to Green and removed the Die Stepping Revision, the"M" designator.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or
408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
sramhelp@idt.com
408-284-4532