

CEM2005



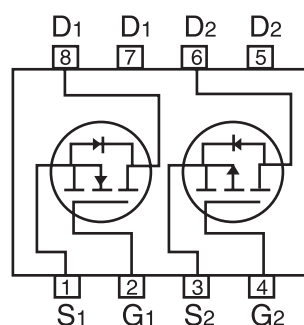
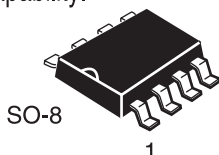
PRELIMINARY

Dual Enhancement Mode Field Effect Transistor(N and P Channel)

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FEATURES

- 20V , 5A , $R_{DS(ON)}=32m\ \Omega$ @ $V_{GS}=4.5V$.
 $R_{DS(ON)}=43m\ \Omega$ @ $V_{GS}=2.5V$.
 -20V , -4A , $R_{DS(ON)}=95m\ \Omega$ @ $V_{GS}=-4.5V$.
 $R_{DS(ON)}=125m\ \Omega$ @ $V_{GS}=-2.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 8	± 8	V
Drain Current-Continuous ^a @ $T_J=125^\circ C$ -Pulsed ^b	I_D	± 5	± 4	A
	I_{DM}	± 30	± 16	A
Drain-Source Diode Forward Current ^a	I_S	1.7	-2.5	A
Maximum Power Dissipation ^a	P_D	2		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ C/W$
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N-Channel ELECTRICAL CHARACTERISTICS (TA 25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = 250μA	0.5	0.68	1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D = 5.0A		26	32	mΩ
		V _{GS} =2.5V, I _D = 4.2A		30	43	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 4.5V	20			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D =5.0A	7	24		S
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} =8V, V _{GS} = 0V f =1.0MHz		1128	1500	pF
Output Capacitance	C _{OSS}			480	630	pF
Reverse Transfer Capacitance	C _{RSS}			119	160	pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 10V, I _D = 1A, V _{GEN} = 4.5V, R _L = 10Ω R _{GEN} = 6Ω		29	60	ns
Rise Time	t _r			65	140	ns
Turn-Off Delay Time	t _{D(OFF)}			60	140	ns
Fall Time	t _f			50	60	ns
Total Gate Charge	Q _g	V _{DS} =10V, I _D = 5A, V _{GS} =4.5V		47	60	nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			8		nC

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P-Channel ELECTRICAL CHARACTERISTICS (TA 25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-20	-26		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = -250μA	-0.6			V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -2.2A		55	95	mΩ
		V _{GS} = -2.5V, I _D = -1.8A		90	125	mΩ
On-State Drain Current	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-20			A
Forward Transconductance	g _{FS}	V _{DS} = -16V, I _D = -2.2A	4			S
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} =-15V, V _{GS} = 0V f =1.0MHz		1490	1950	pF
Output Capacitance	C _{OSS}			480	630	pF
Reverse Transfer Capacitance	C _{RSS}			135	180	pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _D = -10V, I _D = -2.2A, V _{GEN} = - 4.5V, R _{GEN} = 6Ω		8		ns
Rise Time	t _r			26		ns
Turn-Off Delay Time	t _{D(OFF)}			51		ns
Fall Time	t _f			33		ns
Total Gate Charge	Q _g	V _{DS} =-6V, I _D = -2.2A, V _{GS} =-4.5V		19	60	nC
Gate-Source Charge	Q _{gs}			2.5		nC
Gate-Drain Charge	Q _{gd}			6		nC

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 1.7A$	N-Ch	0.72	1.2	V
		$V_{GS} = 0V, I_S = -1.8A$	P-Ch	-0.9	-1.0	

Notes

- a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
- b. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- c. Guaranteed by design, not subject to production testing.

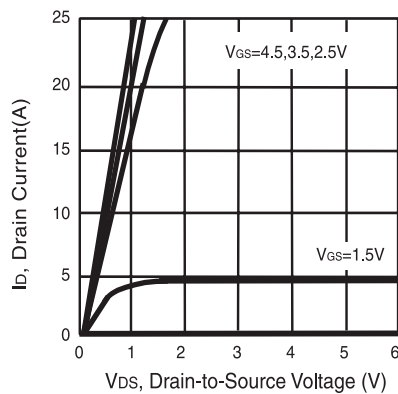


Figure 1. Output Characteristics

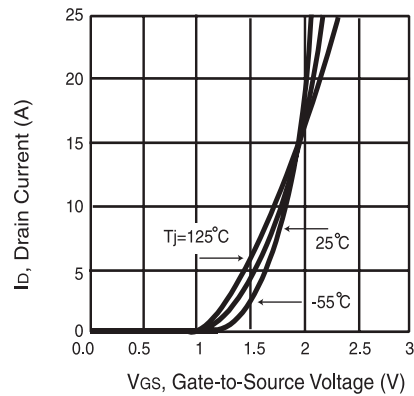


Figure 2. Transfer Characteristics

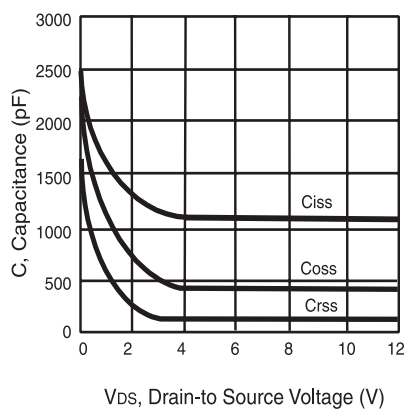


Figure 3. Capacitance

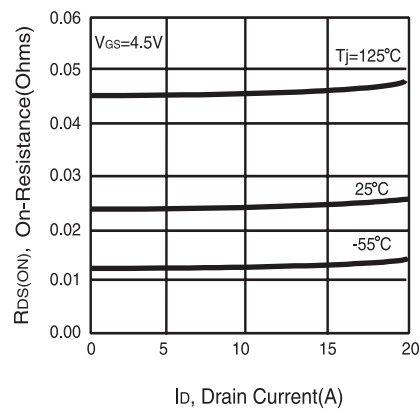


Figure 4. On-Resistance Variation with Drain Current and Temperature

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N-Channel

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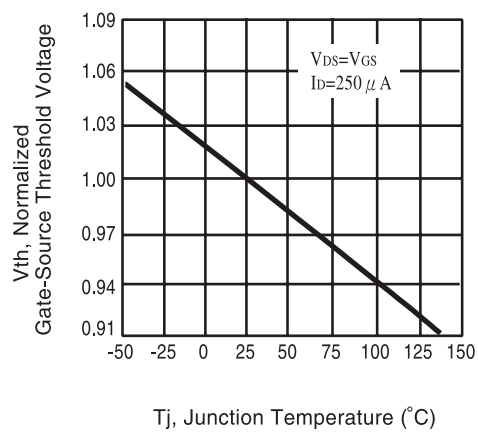


Figure 5. Gate Threshold Variation with Temperature

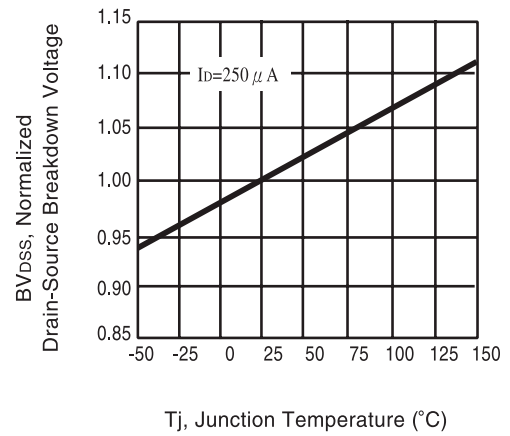


Figure 6. Breakdown Voltage Variation with Temperature

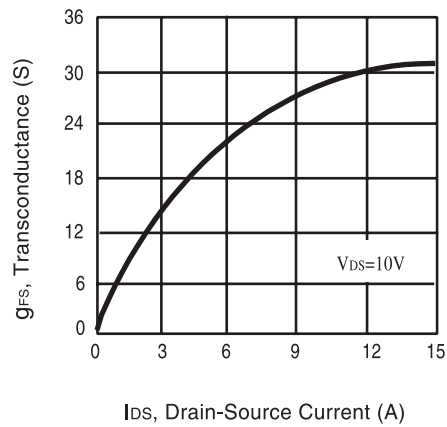


Figure 7. Transconductance Variation with Drain Current

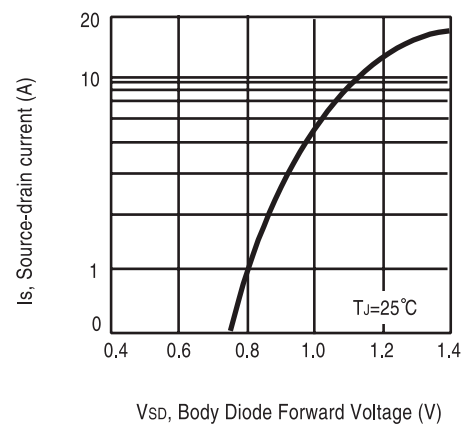


Figure 8. Body Diode Forward Voltage Variation with Source Current

P-Channel

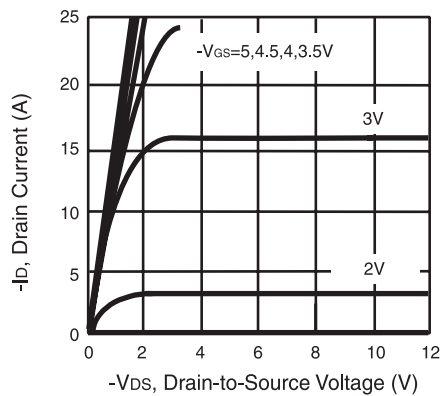


Figure 1. Output Characteristics

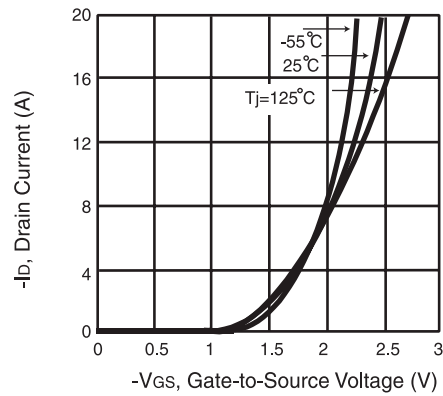


Figure 2. Transfer Characteristics

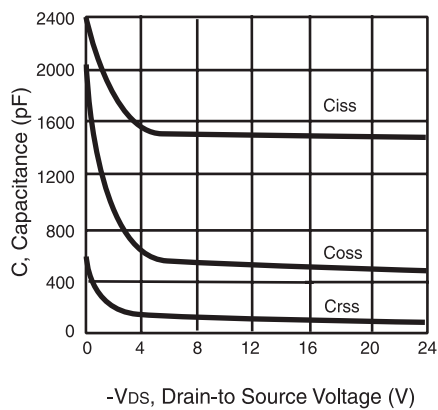


Figure 3. Capacitance

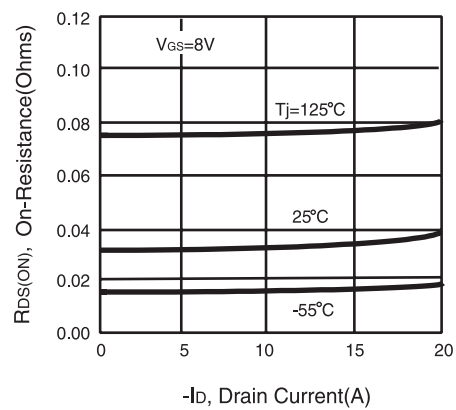


Figure 4. On-Resistance Variation with Drain Current and Temperature

P-Channel

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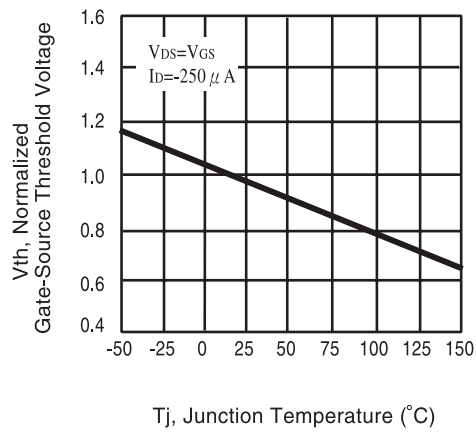


Figure 5. Gate Threshold Variation with Temperature

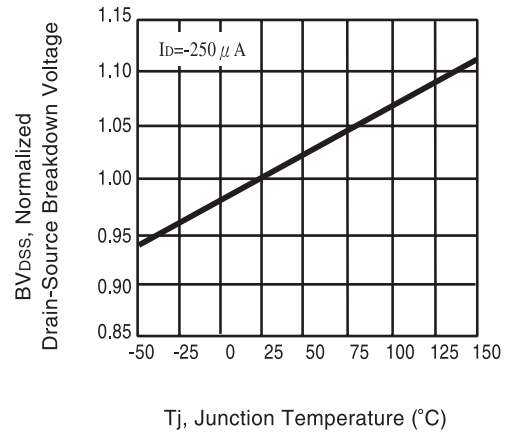


Figure 6. Breakdown Voltage Variation with Temperature

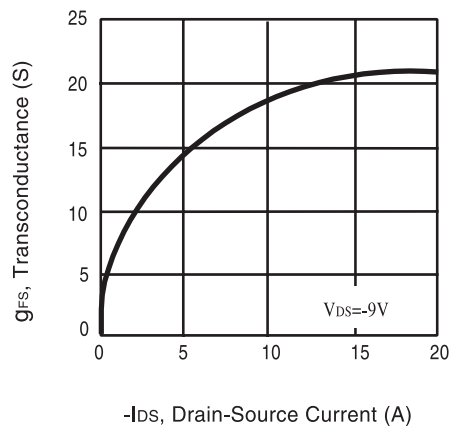


Figure 7. Transconductance Variation with Drain Current

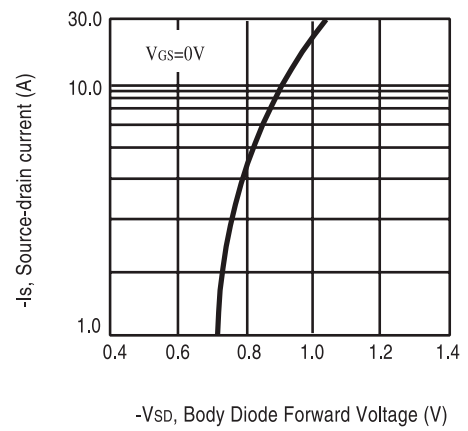
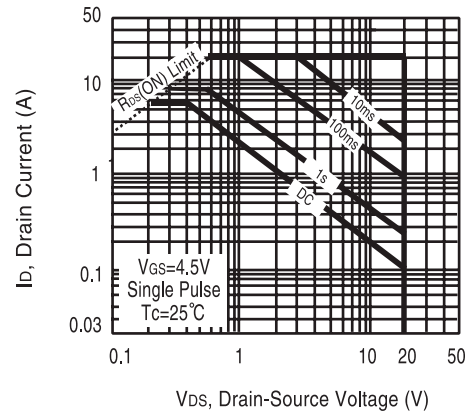
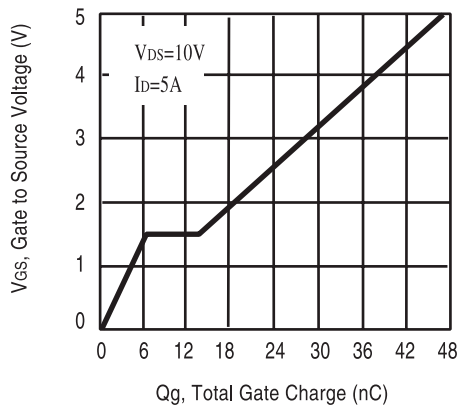


Figure 8. Body Diode Forward Voltage Variation with Source Current

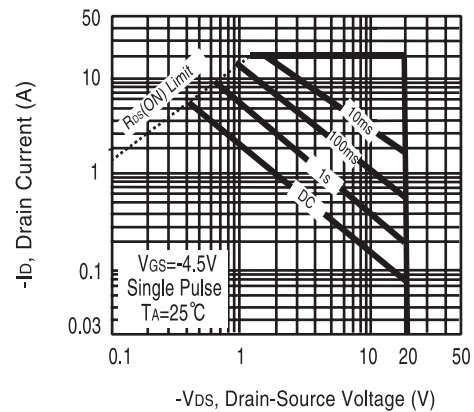
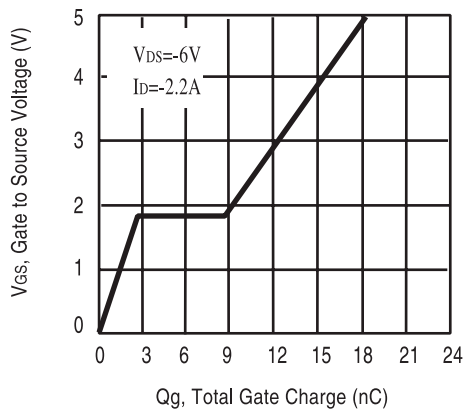
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N-Channel



P-Channel



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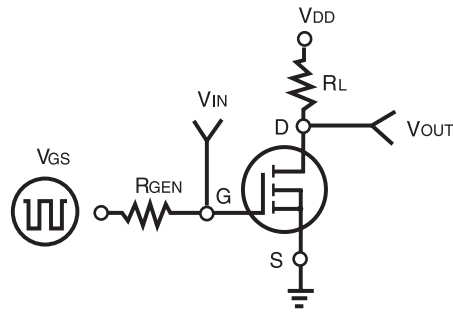


Figure 11. Switching Test Circuit

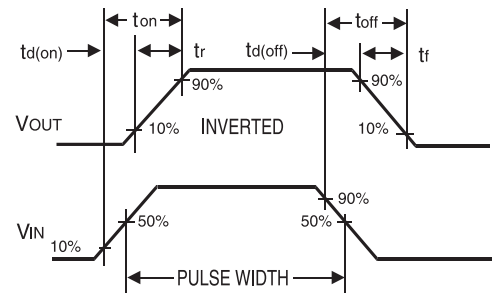


Figure 12. Switching Waveforms

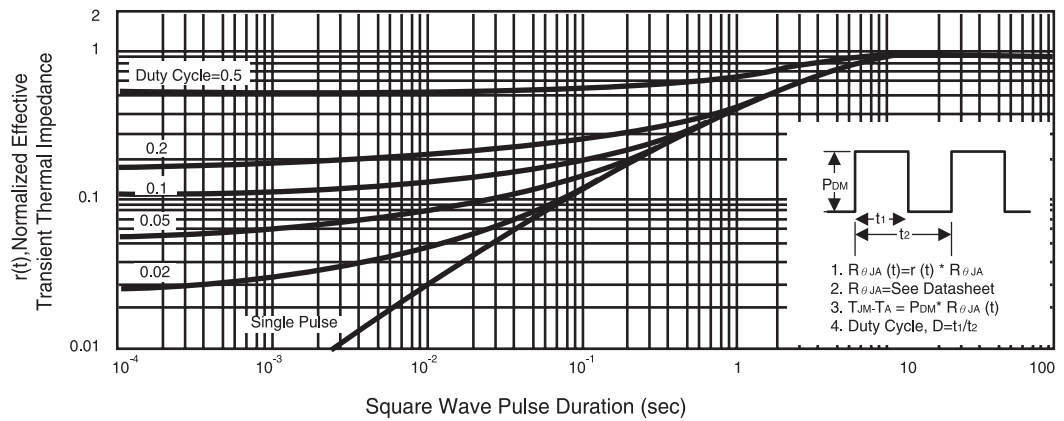


Figure 13. Normalized Thermal Transient Impedance Curve