

Features

- High speed: 45 ns
- Temperature ranges
 □ Industrial: -40 °C to +85 °C
 □ Automotive-A: -40 °C to +85 °C
 □ Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62126DV30
- Ultra low standby power
 Typical standby current: 1 μA
 Maximum standby current: 4 μA
- Ultra low active power
 Typical active current: 1.3 mA at f = 1 MHz
- **Easy** memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II packages

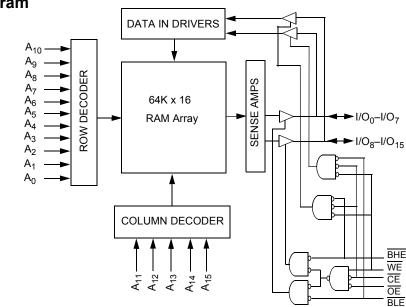
Functional Description

The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery LifeTM (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , BLE HIGH) or during a write operation (\overline{CE} LOW and WE LOW).

To write to the device, take Chip Enable $\overline{(CE)}$ and Write Enable $\overline{(WE)}$ inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

To read <u>from</u> the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.



Logic Block Diagram

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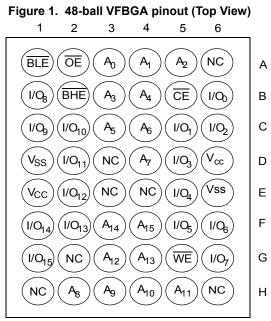
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Pin Configuration



| $\begin{array}{cccc} A_4 \ \square & 0 \\ A_3 \ \square & 2 \\ A_3 \ \square & 2 \\ A_4 \ \square & A_6 \\ A_5 \ \square & A_6 \\ A_6 \ \square & A_6 \ \square & A_6 \\ A_6 \ \square & A_6 \ \square & A_6 \ \square & A_6 \\ A_6 \ \square & A_6 $ | |
|--|--|
| $A_3 \square 2$ $43 \square A_6$ | |
| | |
| A ₂ 3 42 A ₇ | |
| A ₁ 4 41 0E | |
| A ₀ 5 40 BHE | |
| | |
| I/O ₀ □ 7 38 □ I/O ₁₅ | |
| I/O ₁ □ 8 37 □ I/O ₁₄ | |
| I/O ₂ □ 9 36 □ I/O ₁₃ | |
| $I/O_3 \square 10$ $35 \square I/O_{12}$ | |
| | |
| | |
| $V_{SS} = 12$ 33 V_{CC} | |
| | |
| | |
| I/O ₆ □15 30 □ I/O ₉ | |
| <u>I/O</u> 7☐16 29 ☐ I/O ₈ | |
| WE 17 28 NC | |
| A ₁₅ □ 18 27 □ A ₈ | |
| $A_{14} \square 19$ 26 $\square A_9$ | |
| A ₁₃ □ 20 25 □ A ₁₀ | |
| $A_{12} \square 21$ 24 $\square A_{11}$ | |
| NC 22 23 🗆 NC | |

Figure 2. 44-pin TSOP II pinout (Top View)^[1]

Product Portfolio

| | | V _{CC} Range (V) | | | | Power Dissipation | | | | | |
|---------------|--------------|---------------------------|---------------------------|-----|-------|---------------------------------|-----|---------------------------|-----|---------------------------|-----|
| Product | Banga | | | | Speed | Operating, I _{CC} (mA) | | | | Standby, I _{SB2} | |
| Floudel | Kange | Range | | | | f = 1 MHz | | f = f _{max} | | (μ Å) | |
| | | Min | Typ ^[2] | Max | | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62126EV30LL | Industrial | 2.2 | 3.0 | 3.6 | 45 | 1.3 | 2 | 11 | 16 | 1 | 4 |
| CY62126EV30LL | Automotive-A | 2.2 | 3.0 | 3.6 | 45 | 1.3 | 2 | 11 | 16 | 1 | 4 |
| CY62126EV30LL | Automotive-E | 2.2 | 3.0 | 3.6 | 55 | 1.3 | 4 | 11 | 35 | 1 | 30 |

Notes

NC pins are not connected on the die.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.



Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

| Storage temperature –65 °C to +150 °C |
|---|
| Ambient temperature with power applied |
| Supply voltage to ground potential $^{[3, 4]}$ –0.3 V to 3.6 V (V _{CCmax} + 0.3 V) |
| DC voltage applied to outputs in High Z state $^{[3, 4]}$ 0.3 V to 3.6 V (V _{CCmax} + 0.3 V) |

| DC input voltage $^{[3, 4]}$ –0.3 V to 3.6 V (V _{CCma} | _{ix} + 0.3 V) |
|---|------------------------|
| Output current into outputs (LOW) | 20 mA |
| Static discharge voltage (MIL-STD-883, Method 3015) | > 2001 V |
| Latch up current | > 200 mA |

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[5] |
|---------------|------------------------------|------------------------|--------------------------------------|
| CY62126EV30LL | Industrial / Automotive-A | –40 °C to +85 °C | 2.2 V to 3.6 V |
| | Automotive-E | –40 °C to +125 °C | |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns (Industrial / Automotive-A) | | | 55 ns | Unit | | | |
|---------------------------------|--|--|---|--------------------------------------|---------------------------|-----------------------|-------|---------------------------|-----------------------|----|--|
| | | | | | Typ ^[6] | Max | Min | Typ ^[6] | Max | | |
| V _{OH} | Output high voltage | I _{OH} = -0.1 mA | | 2.0 | - | - | 2.0 | - | - | V | |
| | | I _{OH} = -1.0 mA, \ | / _{CC} ≥ 2.70 V | 2.4 | - | - | 2.4 | - | - | V | |
| V _{OL} | Output low voltage | I _{OL} = 0.1 mA | | - | - | 0.4 | - | | 0.4 | V | |
| | | I _{OL} = 2.1 mA, V _C | _{CC} <u>></u> 2.70 V | I | - | 0.4 | - | - | 0.4 | V | |
| V _{IH} | Input high voltage | $V_{\rm CC}$ = 2.2 V to 2 | .7 V | 1.8 | - | V _{CC} + 0.3 | 1.8 | - | V _{CC} + 0.3 | V | |
| | | V _{CC} = 2.7 V to 3 | .6 V | 2.2 | - | V _{CC} + 0.3 | 2.2 | - | V _{CC} + 0.3 | V | |
| V _{IL} | Input low voltage | $V_{\rm CC}$ = 2.2 V to 2 | .7 V | -0.3 | - | 0.6 | -0.3 | - | 0.6 | V | |
| | | V _{CC} = 2.7 V to 3 | .6 V | -0.3 | - | 0.8 | -0.3 | - | 0.8 | V | |
| I _{IX} | Input leakage current | $GND \leq V_{I} \leq V_{CC}$ | | -1 | - | +1 | -4 | - | +4 | μA | |
| I _{OZ} | Output leakage current | $GND \leq V_O \leq V_{CO}$ Disabled | _C , Output | –1 | - | +1 | -4 | - | +4 | μA | |
| I _{CC} | V _{CC} operating supply | $f = f_{max} = 1/t_{RC}$ | $V_{CC} = V_{CCmax}$ | - | 11 | 16 | - | 11 | 35 | mA | |
| | current | f = 1 MHz | I _{OUT} = 0 mA CMOS levels | - | 1.3 | 2.0 | - | 1.3 | 4.0 | | |
| I _{SB1} ^[7] | Automatic CE power down current —CMOS inputs | $\label{eq:constraint} \begin{split} \overline{CE} &\geq V_{CC} - 0.2 \ V_{IN} \geq V_{CC} - 0.2 \ f = f_{max} (Address f = 0 \ (\overline{OE}, \overline{BHE}, V_{CC} = 3.60 \ V \end{split}$ | V, V _{IN} <u>≤</u> 0.2 V, and Data Only), | _ | 1 | 4 | _ | 1 | 35 | μA | |
| I _{SB2} ^[7] | Automatic CE power down current —CMOS inputs | $\frac{\overline{CE} \ge V_{CC} - 0.2}{V_{IN} \ge V_{CC} - 0.2}$ f = 0, V _{CC} = 3.60 | V or V _{IN} <u>≤</u> 0.2 V, | - | 1 | 4 | - | 1 | 30 | μA | |

Notes

- Notes
 3. V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
 4. V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
 5. Full device AC operation assumes a 100 μs ramp time from 0 to V_{cc}(min) and 200 μs wait time after V_{cc} stabilization.
 6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
 7. Chip enable (CE) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.



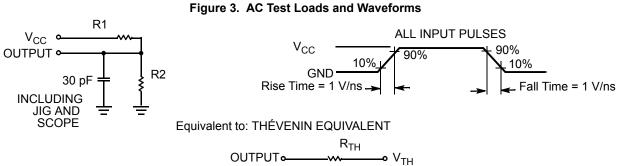
Capacitance

| Parameter [8] | Description | Test Conditions | Max | Unit |
|------------------|--------------------|--|-----|------|
| C _{IN} | Input capacitance | $T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = V_{CC(typ)}$ | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter [8] | Description | Test Conditions | 48-ballVFBGA Package | 44-pin TSOP II Package | Unit |
|-----------------|--|--|-------------------------|---------------------------|------|
| Θ_{JA} | | Still Air, soldered on a 4.25 × 1.125 inch, two-layer printed circuit board | 58.85 | 28.2 | °C/W |
| Θ ^{JC} | Thermal resistance (junction to case) | | 17.01 | 3.4 | °C/W |

AC Test Loads and Waveforms



| Parameters | 2.2 V–2.7 V | 2.7 V–3.6 V | Unit |
|-----------------|-------------|-------------|------|
| R1 | 16600 | 1103 | Ω |
| R2 | 15400 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.2 | 1.75 | V |



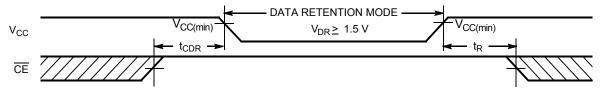
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conc | Min | Тур ^[9] | Max | Unit | |
|-----------------------------------|--------------------------------------|--|------------------------------|--------------------|-----|------|----|
| V _{DR} | V_{CC} for data retention | | | 1.5 | - | - | V |
| I _{CCDR} ^[10] | Data retention current | $V_{CC} = V_{DR},$ | Industrial / Automotive-A | _ | - | 3 | μA |
| | | $\label{eq:central_constraint} \begin{split} \overline{CE} &\geq V_{CC} - 0.2 \text{ V}, \\ V_{IN} &\geq V_{CC} - 0.2 \text{ V} \text{ or } \\ V_{IN} &\leq 0.2 \text{ V} \end{split}$ | Automotive-E | - | - | 30 | μΑ |
| t _{CDR} ^[11] | Chip deselect to data retention time | | | 0 | - | - | ns |
| t _R ^[12] | Operation recovery time | | CY62126EV30LL-45 | 45 | - | - | ns |
| | | | CY62126EV30LL-55 | 55 | _ | - | |

Data Retention Waveform





Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

10. Chip enable $\overline{(CE)}$ needs to be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating. 11. Tested initially and after any design or process changes that may affect these parameters. 12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} > 100 µs.



Switching Characteristics

Over the Operating Range

| Parameter ^[13, 14] | Description | | 45 ns (Industrial / Automotive-A) | | 55 ns (Automotive-E) | |
|-------------------------------|---------------------------------------|-----|--------------------------------------|-----|----------------------|----|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t _{RC} | Read cycle time | 45 | - | 55 | - | ns |
| t _{AA} | Address to data valid | - | 45 | - | 55 | ns |
| t _{OHA} | Data hold from address change | 10 | - | 10 | - | ns |
| t _{ACE} | CE LOW to data valid | - | 45 | - | 55 | ns |
| t _{DOE} | OE LOW to data valid | - | 22 | - | 25 | ns |
| t _{LZOE} | OE LOW to Low Z ^[15] | 5 | _ | 5 | _ | ns |
| t _{HZOE} | OE HIGH to High Z ^[15, 16] | - | 18 | - | 20 | ns |
| t _{LZCE} | CE LOW to Low Z ^[15] | 10 | _ | 10 | _ | ns |
| t _{HZCE} | CE HIGH to High Z ^[15, 16] | - | 18 | _ | 20 | ns |
| t _{PU} | CE LOW to power up | 0 | _ | 0 | _ | ns |
| t _{PD} | CE HIGH to power down | - | 45 | _ | 55 | ns |
| t _{DBE} | BHE / BLE LOW to data valid | - | 22 | _ | 25 | ns |
| t _{LZBE} | BHE / BLE LOW to Low Z [15] | 5 | _ | 5 | _ | ns |
| t _{HZBE} | BHE / BLE HIGH to High Z [15, 16] | - | 18 | _ | 20 | ns |
| Write Cycle [17, 18 | 3] | | | | | |
| t _{WC} | Write cycle time | 45 | _ | 55 | _ | ns |
| t _{SCE} | CE LOW to write end | 35 | - | 40 | - | ns |
| t _{AW} | Address setup to write end | 35 | - | 40 | - | ns |
| t _{HA} | Address hold from write end | 0 | - | 0 | - | ns |
| t _{SA} | Address setup to write start | 0 | - | 0 | - | ns |
| t _{PWE} | WE pulse width | 35 | - | 40 | - | ns |
| t _{BW} | BHE / BLE pulse width | 35 | - | 40 | - | ns |
| t _{SD} | Data setup to write end | 25 | - | 25 | - | ns |
| t _{HD} | Data hold from write end | 0 | - | 0 | - | ns |
| t _{HZWE} | WE LOW to High Z ^[15, 16] | - | 18 | - | 20 | ns |
| t _{LZWE} | WE HIGH to Low Z ^[15] | 10 | _ | 10 | - | ns |

Notes

- 13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance. 14. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.

15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device. 16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

17. The internal write time of the memory is defined by the overlap of WE, $\overline{CE} = V_{|L}$, \overline{BHE} , \overline{BLE} or both = $V_{|L}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.

18. The minimum write cycle pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be equal to sum of t_{SD} and t_{HZWE}.



Switching Waveforms

Figure 5. Read Cycle No. 1 (Address transition controlled) ^[19, 20]

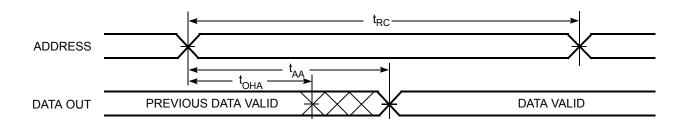
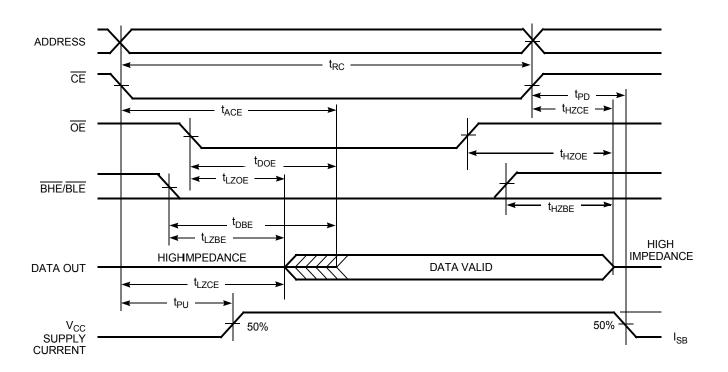


Figure 6. Read Cycle No. 2 (OE controlled) ^[20, 21]



Notes

19. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} .

20. $\overline{\text{WE}}$ is high for read cycle.

21. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.





Switching Waveforms (continued)

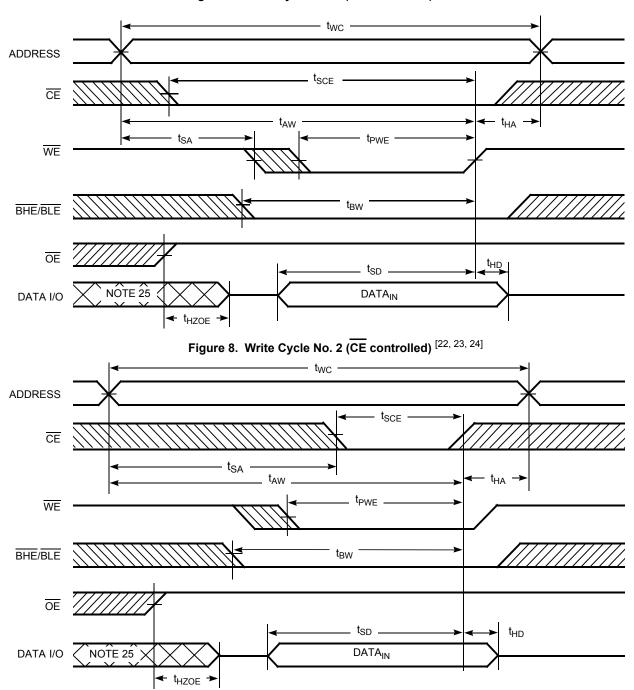


Figure 7. Write Cycle No. 1 (WE controlled) ^[22, 23, 24]

Notes

22. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{\parallel L}$, \overline{BHE} , \overline{BLE} or both = $V_{\parallel L}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.

23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

- 24. If \overline{CE} goes high simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state. 25. During this period, the I/Os are in output state. Do not apply input signals.





Switching Waveforms (continued)

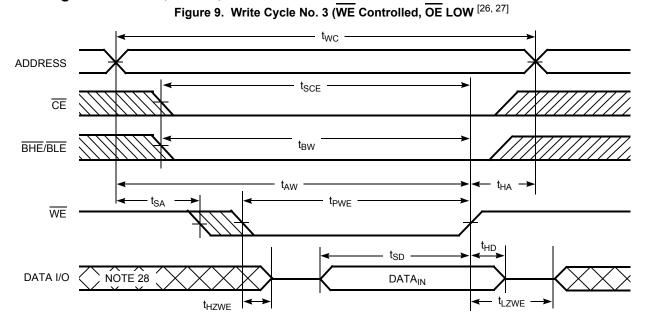
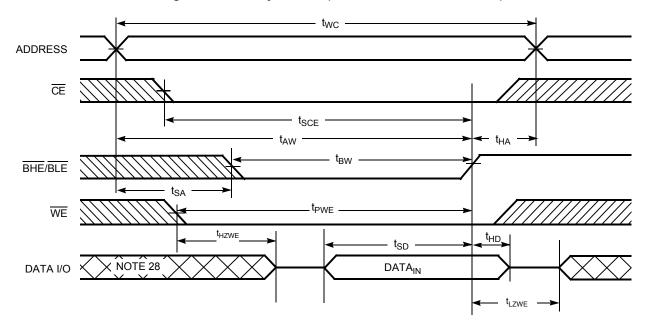


Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ controlled, \overline{OE} LOW) [26]



Notes

26. If \overline{CE} goes high simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state. 27. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE} . 28. During this period, the I/Os are in output state. Do not apply input signals.





Truth Table

| CE ^[29] | WE | OE | BHE | BLE | Inputs/Outputs | Mode | Power |
|---------------------------|----|----|-----|-----|--|---------------------|----------------------------|
| Н | Х | Х | Х | Х | High Z | Deselect/power down | Standby (I _{SB}) |
| L | Х | Х | Н | Н | High Z | Output disabled | Active (I _{CC}) |
| L | Н | L | L | L | Data out (I/O ₀ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | Н | L | Н | L | Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z | Read | Active (I _{CC}) |
| L | Н | L | L | Н | Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z | Read | Active (I _{CC}) |
| L | Н | Н | L | L | High Z | Output disabled | Active (I _{CC}) |
| L | Н | Н | Н | L | High Z | Output disabled | Active (I _{CC}) |
| L | Н | Н | L | Н | High Z | Output disabled | Active (I _{CC}) |
| L | L | Х | L | L | Data in (I/O ₀ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | L | Х | Н | L | Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z | Write | Active (I _{CC}) |
| L | L | Х | L | Н | Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z | Write | Active (I _{CC}) |

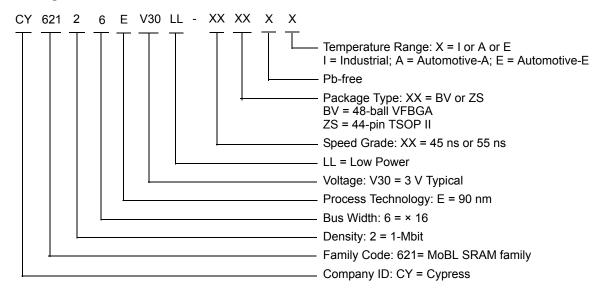


Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---------------|----------------------|--------------------|--------------------------|--------------------|
| 45 | CY62126EV30LL-45BVXI | 51-85150 | 48-ball VFBGA (Pb-free) | Industrial |
| | CY62126EV30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | Industrial |
| | CY62126EV30LL-45ZSXA | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-A |
| 55 | CY62126EV30LL-55BVXE | 51-85150 | 48-ball VFBGA (Pb-free) | Automotive-E |
| | CY62126EV30LL-55ZSXE | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-E |

Contact your local Cypress sales representative for availability of other parts.

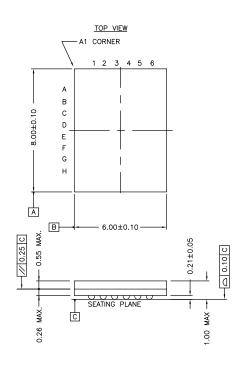
Ordering Code Definitions

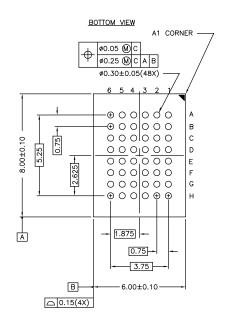




Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150





NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H



Package Diagrams (continued)

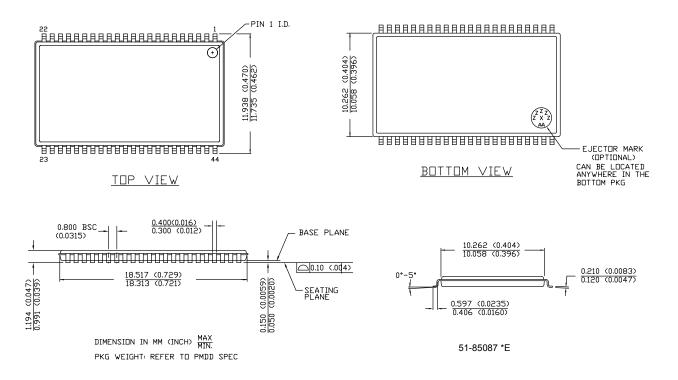


Figure 12. 44-pin TSOP II Package Outline, 51-85087



Acronyms

| Acronym | Description |
|---------|---|
| CE | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| OE | Output Enable |
| RAM | Random Access Memory |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| WE | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |



Document History Page

| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
|------|---------|--------------------|--------------------|--|
| ** | 202760 | See ECN | AJU | New data sheet. |
| *A | 300835 | See ECN | SYT | Converted from Advance Information to Preliminary Specified Typical standby power in the Features Section Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package and removed the footnote associated with it on page #2 Changed t _{OHA} from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively Changed t _{DOE} , t _{SD} from 15 to 18 ns for 35-ns speed bin Changed t _{HZOE} , t _{HZBE} , t _{HZWE} from 12 and 15 ns to 15 and 18 ns for the 35 n and 45 ns speed bins, respectively Changed t _{HZCE} from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively Changed t _{SCE} ,t _{BW} from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed bins, respectively Changed t _{AW} from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bin respectively Changed t _{DBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Changed t _{BBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Changed t _{BBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Changed t _{BBE} from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Removed footnote that read "BHE.BLE is the AND of both BHE and BLE. Ch can <u>be deselected</u> by either disabling the chip enable signals or by disablir both BHE and BLE" on page # 4 Removed footnote that read "If both BHE and BLE are toggled together, the t _{LZBE} is 10 ns" on page # 5 Added Pb-free package information |
| *B | 461631 | See ECN | NXR | Converted from Preliminary to Final Removed 35 ns Speed Bin Removed "L" version of CY62126EV30 Changed I _{CC (Typ)} from 8 mA to 11 mA and I _{CC (max)} from 12 mA to 16 mA f f = f _{max} Changed I _{CC (max)} from 1.5 mA to 2.0 mA for f = 1 MHz, I _{SB1} , I _{SB2 (max)} fro 1 μ A to 4 μ A, I _{SB1} , I _{SB2 (Typ)} from 0.5 μ A to 1 μ A, I _{CCDR (max)} from 1.5 μ A to 3 μ A, AC Test load Capacitance value from 50 pF to 30 pF, t _{LZOE} from 3 to 5 ns, t _{LZCE} from 6 to 10 ns, t _{HZCE} from 22 to 18 ns, t _{LZBE} from 6 to 5 ns, t _{PV} from 30 to 35 ns, t _{SD} from 22 to 25 ns, t _{LZWE} from 6 to 10 ns, and updated th Ordering Information table. |
| *C | 925501 | See ECN | VKN | Added footnote #7 related to I _{SB2} and I _{CCDR} Added footnote #11 related AC timing parameters |
| *D | 1045260 | See ECN | VKN | Added Automotive information Updated Ordering Information table |
| *E | 2631771 | 01/07/09 | | Changed $\overrightarrow{\text{CE}}$ condition from X to L in Truth table for Output Disable mode Updated template |
| *F | 2944332 | 06/04/2010 | VKN | Added Contents Removed byte enable from footnote #2 in Electrical Characteristics Added footnote related to chip enable in Truth Table Updated Package Diagrams Updated links in Sales, Solutions, and Legal Information |
| *G | 2996166 | 07/29/2010 | AJU | Added CY62126EV30LL-45ZSXA part in Ordering Information. Added Ordering Code Definitions. Modified table footnote format. |
| *H | 3113864 | 12/17/2010 | PRAS | Updated Figure 1 and Package Diagram, and fixed Typo in Figure 3. |



Document History Page (continued)

| Dei | FOUNT | Submission | Orig. of | Description of Olympic |
|------|---------|------------|----------|--|
| Rev. | ECN No. | Date | Change | Description of Change |
| * | 3270487 | 05/31/2011 | RAME | Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated Electrical Characteristics. Updated Data Retention Characteristics. Added Acronyms and Units of Measure. Updated to new template. |
| *J | 4205722 | 11/29/2013 | MEMJ | Updated Features: Added Automotive-A range information. Updated Product Portfolio: Added Automotive-A range information. Updated Operating Range: Segregated Automotive-A and Automotive-E ranges. Updated Electrical Characteristics: Added Automotive-A with Industrial for 45 ns speed bin. Renamed Automotive as Automotive-E for 55 ns speed bin. Updated Data Retention Characteristics: Segregated Automotive-A and Automotive-E in conditions for I _{CCDR} parameter. Updated Switching Characteristics: Added Automotive-A with Industrial for 45 ns speed bin. Renamed Automotive-A with Industrial for 45 ns speed bin. Renamed Automotive as Automotive-E for 55 ns speed bin. Renamed Automotive as Automotive-E for 55 ns speed bin. Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E. Updated to new template. |
| *K | 4211675 | 12/12/2013 | MEMJ | No technical updates. Removed the border lines in Package Diagram specs. |
| *L | 4410948 | 06/17/2014 | VINI | Updated Switching Characteristics: Added Note 18 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 27 and referred the same note in Figure 9. Completing Sunset Review. |
| *M | 4576475 | 11/21/2014 | VINI | Updated Functional Description: Added "For a complete list of related documentation, click here." at the end |
| *N | 4612072 | 01/05/2015 | VINI | Updated Maximum Ratings: Referred Notes 3, 4 in "Supply voltage to ground potential". |
| *0 | 4797476 | 06/15/2015 | VINI | Updated to new template. Completing Sunset Review. |
| *P | 5975641 | 11/24/2017 | AESATMP9 | Updated logo and Copyright. |



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