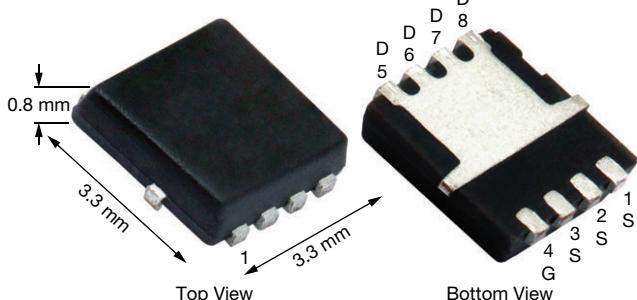


## P-Channel 30 V (D-S) MOSFET

<b>PRODUCT SUMMARY</b>			
<b>V<sub>DS</sub> (V)</b>	<b>R<sub>DS(on)</sub> (Ω) MAX.</b>	<b>I<sub>D</sub> (A) <sup>d</sup></b>	<b>Q<sub>g</sub> (TYP.)</b>
<b>-30</b>	0.021 at V <sub>GS</sub> = -10 V	-20 <sup>e</sup>	15 nC
	0.034 at V <sub>GS</sub> = -4.5 V	-18.7	

**Thin PowerPAK® 1212-8 Single**

**Ordering Information:**

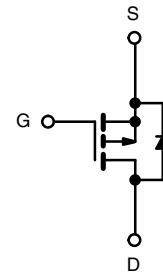
SiS429DNT-T1-GE3 (Lead (Pb)-free and Halogen-free)

**FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Thin 0.8 mm profile
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**
**APPLICATIONS**

- Notebook PC
  - Load switch
  - Battery switch
  - Adaptor switch



P-Channel MOSFET

**ABSOLUTE MAXIMUM RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	-20 <sup>e</sup>	A
		-20 <sup>e</sup>	
		-10.5 <sup>a, b</sup>	
		-8.3 <sup>a, b</sup>	
Pulsed Drain Current (t = 100 µs)	I <sub>DM</sub>	-50	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	-20 <sup>e</sup>	
		-2.9 <sup>a, b</sup>	
Avalanche Current	I <sub>AS</sub>	-20	mJ
Single-Pulse Avalanche Energy	E <sub>AS</sub>	20	
Maximum Power Dissipation	P <sub>D</sub>	27.8	W
		17.8	
		3.5 <sup>a, b</sup>	
		2.2 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>f, g</sup>		260	

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient <sup>a, c</sup>	R <sub>thJA</sub>	29	36	°C/W
Maximum Junction-to-Case	R <sub>thJC</sub>	3.6	4.5	

**Notes**

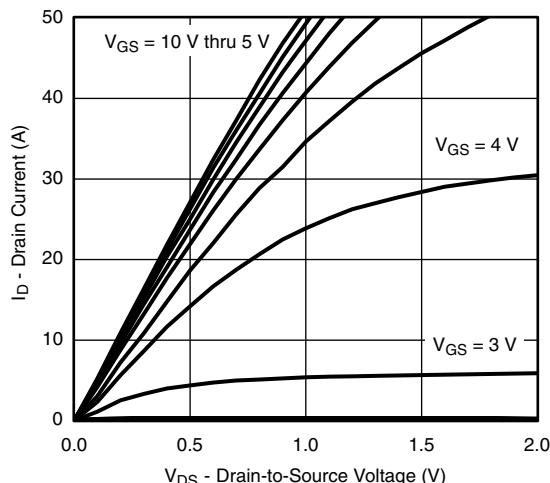
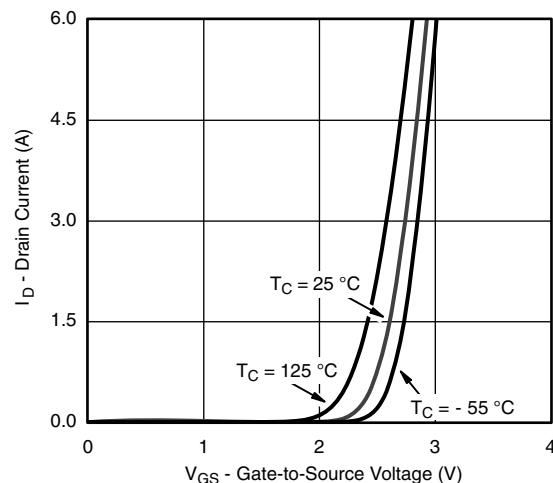
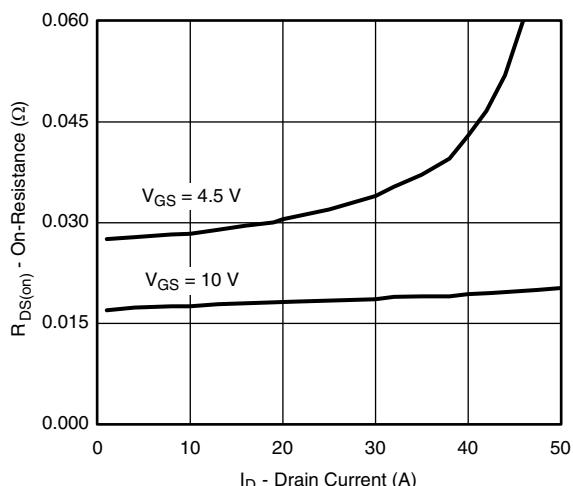
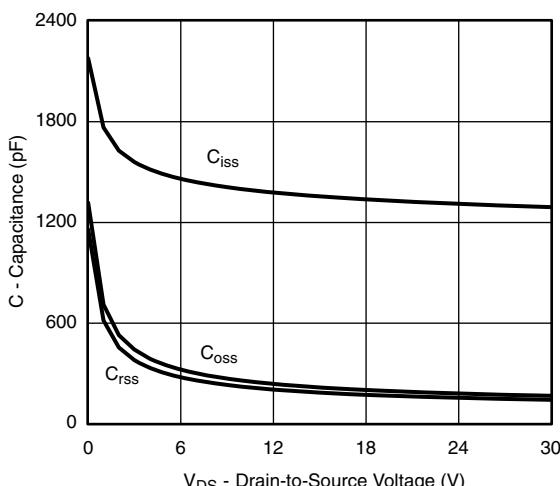
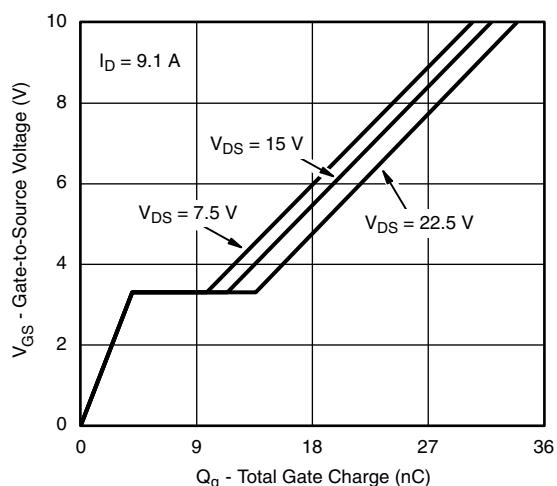
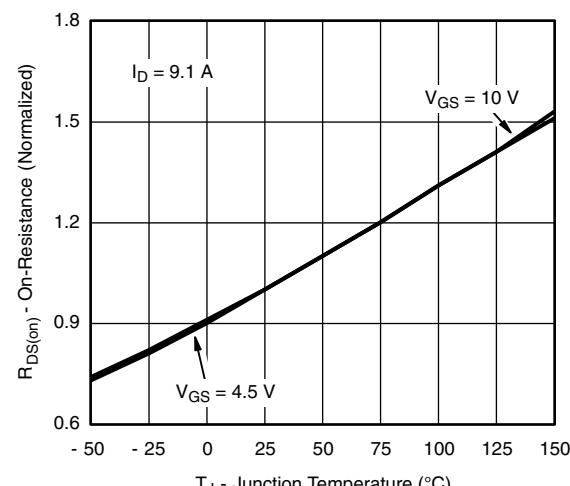
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 81 °C/W.
- Based on T<sub>C</sub> = 25 °C.
- Package limited.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The Thin PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

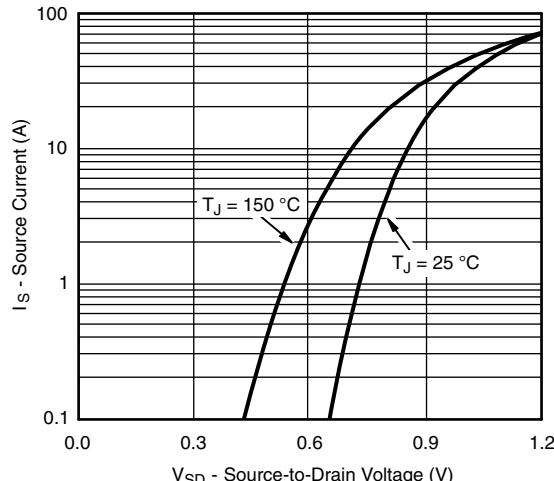
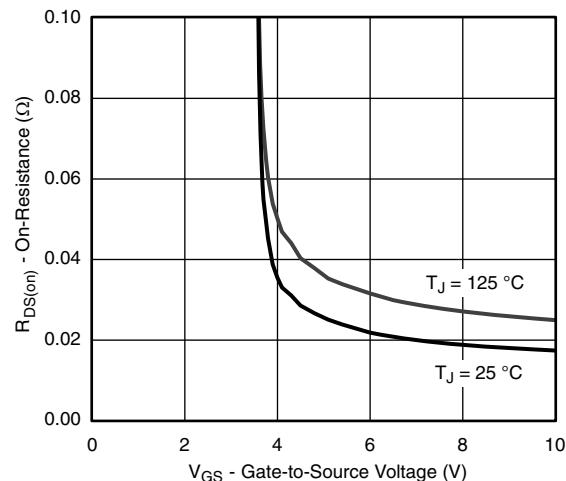
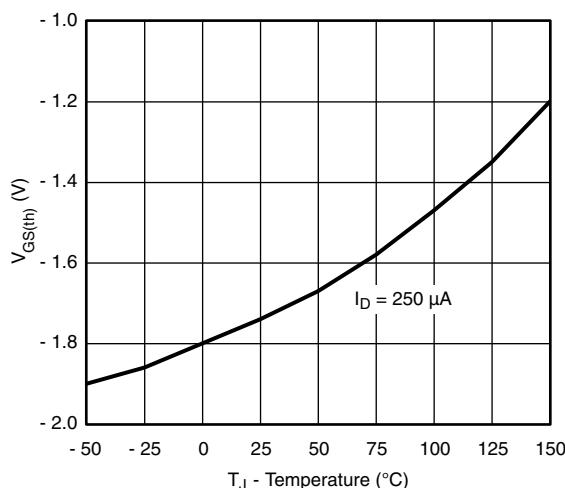
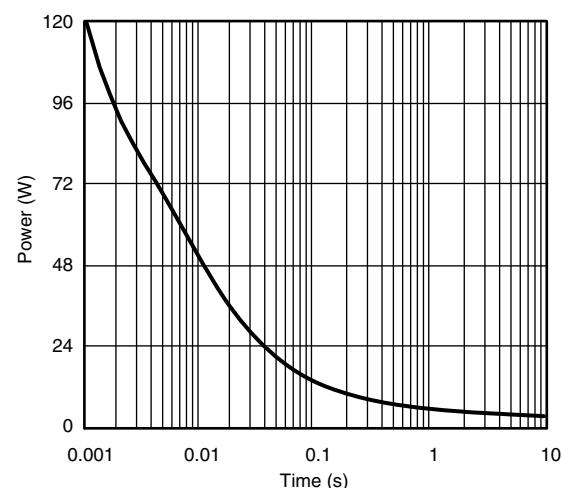
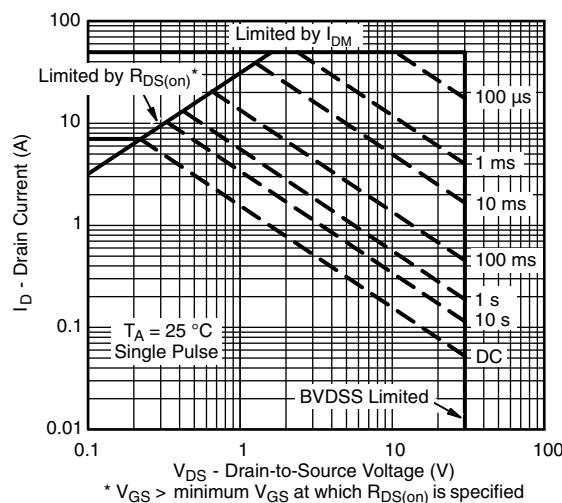
<b>SPECIFICATIONS</b> ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = -250 \mu\text{A}$	-30	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$	-	-31	-	mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	4.5	-	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = -250 \mu\text{A}$	-1	-	-3	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$	-	-	-5	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq -10 \text{ V}$ , $V_{GS} = -10 \text{ V}$	-30	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}$ , $I_D = -10.5 \text{ A}$	-	0.0175	0.0210	$\Omega$
		$V_{GS} = -4.5 \text{ V}$ , $I_D = -8.3 \text{ A}$	-	0.0283	0.0340	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10 \text{ V}$ , $I_D = -10.5 \text{ A}$	-	23	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	-	1350	-	pF
Output Capacitance	$C_{oss}$		-	215	-	
Reverse Transfer Capacitance	$C_{rss}$		-	185	-	
Total Gate Charge	$Q_g$	$V_{DS} = -15 \text{ V}$ , $V_{GS} = -10 \text{ V}$ , $I_D = -10.5 \text{ A}$	-	32	50	nC
			-	15	25	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}$ , $V_{GS} = -4.5 \text{ V}$ , $I_D = -10.5 \text{ A}$	-	4	-	
Gate-Drain Charge	$Q_{gd}$		-	7.5	-	
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$	1.2	5.8	11.6	$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -15 \text{ V}$ , $R_L = 1.8 \Omega$ $I_D \equiv -8.4 \text{ A}$ , $V_{GEN} = -10 \text{ V}$ , $R_g = 1 \Omega$	-	10	15	ns
Rise Time	$t_r$		-	8	15	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	45	70	
Fall Time	$t_f$		-	12	25	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = -15 \text{ V}$ , $R_L = 1.8 \Omega$ $I_D \equiv -8.4 \text{ A}$ , $V_{GEN} = -4.5 \text{ V}$ , $R_g = 1 \Omega$	-	42	70	
Rise Time	$t_r$		-	35	60	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	40	70	
Fall Time	$t_f$		-	16	30	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	-20	A
Pulse Diode Forward Current ( $t = 100 \mu\text{s}$ )	$I_{SM}$		-	-	-50	
Body Diode Voltage	$V_{SD}$	$I_S = -8.4 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-	-0.85	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -8.4 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$	-	34	60	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	22	40	
Reverse Recovery Fall Time	$t_a$		-	11	-	
Reverse Recovery Rise Time	$t_b$		-	23	-	

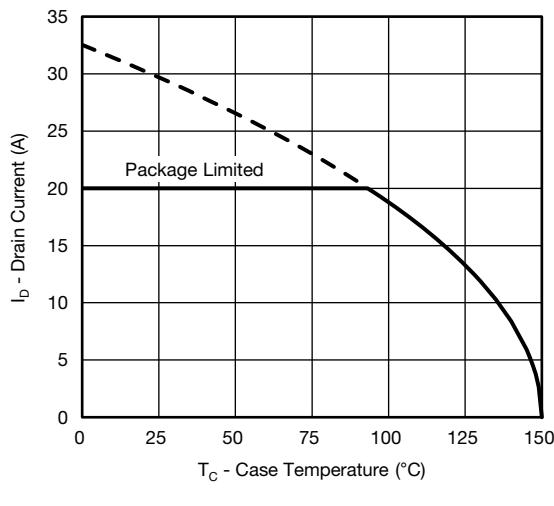
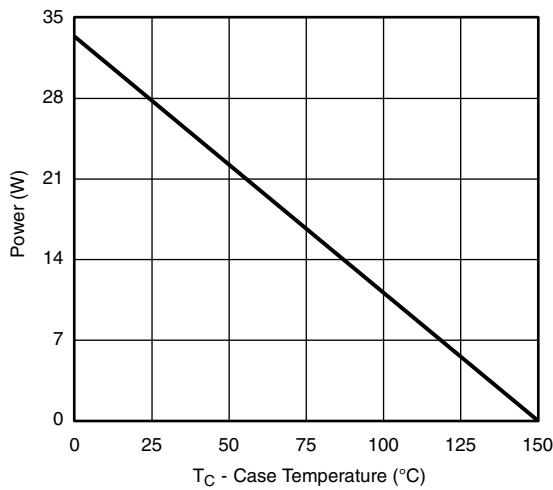
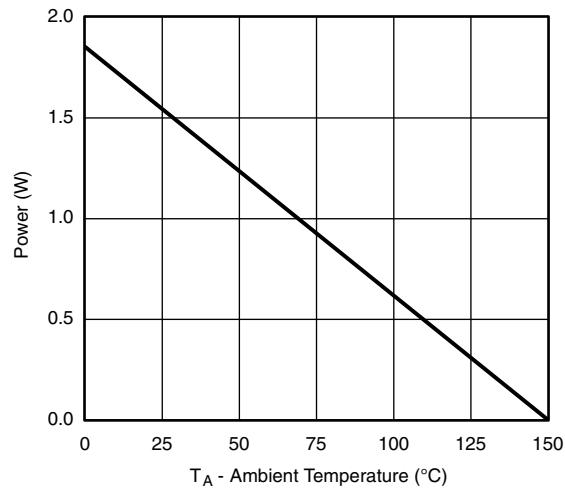
**Notes**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2 \%$ .
- b. Guaranteed by design, not subject to production testing.

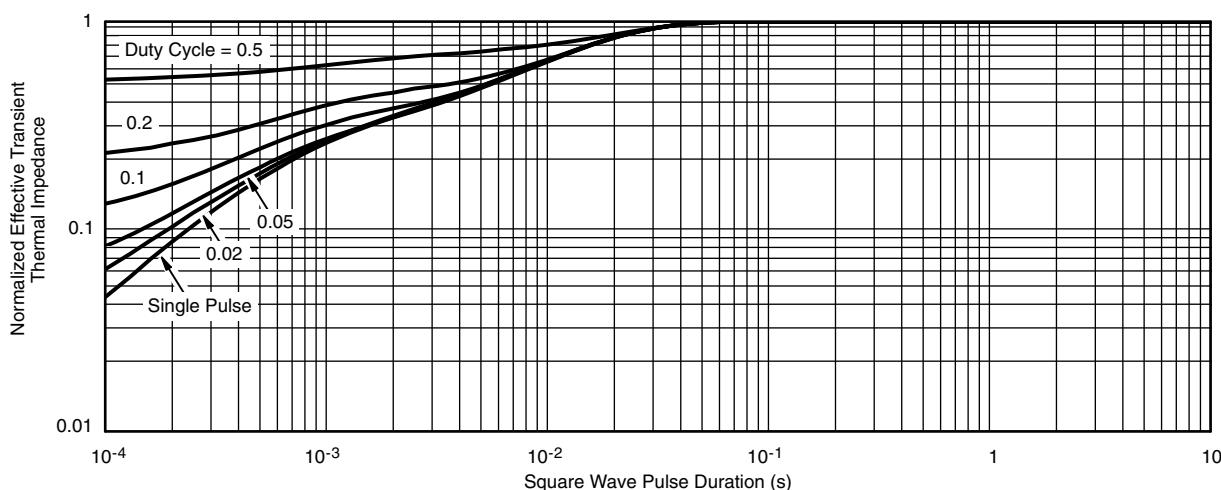
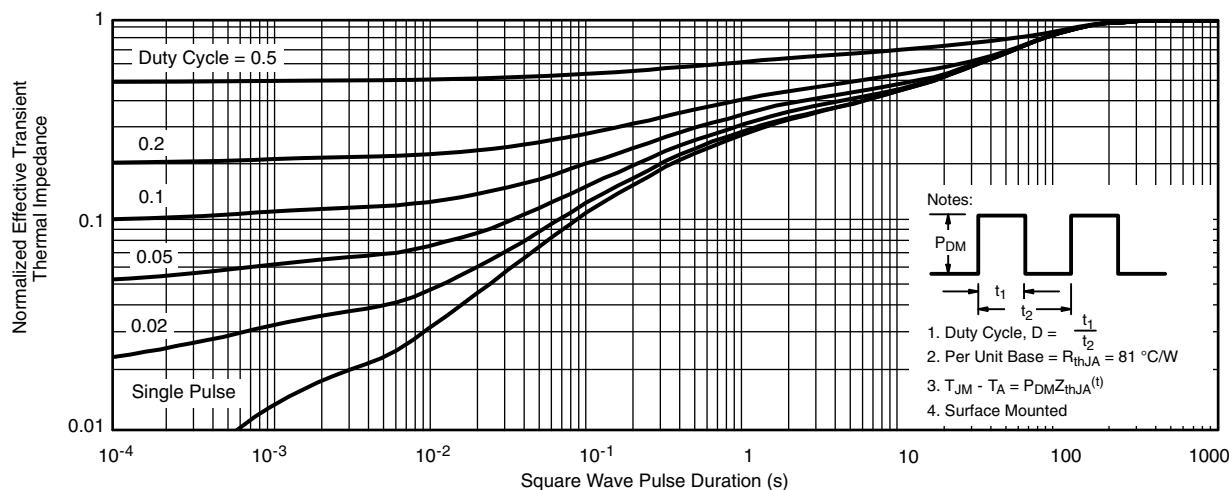
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Single Pulse Power, Junction-to-Ambient**

**Safe Operating Area**

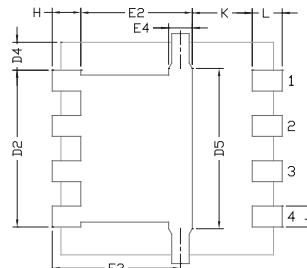
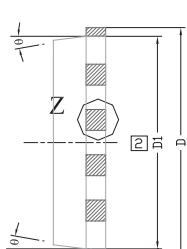
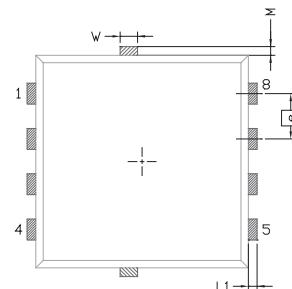
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power, Junction-to-Case**

**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_J(\max.) = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

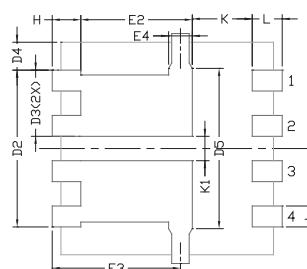
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62964](http://www.vishay.com/ppg?62964).

### PowerPAK® 1212-8T



BACKSIDE VIEW OF SINGLE PAD



BACKSIDE VIEW OF DUAL PAD

NOTE:  
 1. MILLIMETER WILL GOVERN  
 2. DIMENSIONS EXCLUSIVE OF MOLD  
 GATE BURRS.  
 3. DIMENSIONS EXCLUSIVE OF MOLD  
 FLASH AND CUTTING BURRS.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D3	0.48	-	0.89	0.019	-	0.035
D4	0.47 TYP.			0.0185 TYP.		
D5	2.3 TYP.			0.090 TYP.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 TYP.			0.013 TYP.		
e	0.65 BSC			0.026 BSC		
K	0.86 TYP.			0.034 TYP.		
K1	0.35	-	-	0.014	-	-
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
$\theta$	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 TYP.			0.005 TYP.		

ECN: T13-0056-Rev. A, 18-Feb-13

DWG: 6012

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## Material Category Policy

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**