19-2044; Rev 1, 2/05

Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

General Description

The MAX4695 is a low-voltage, dual single-pole/double-throw (SPDT) analog switch that operates from a single +1.8V to +5.5V supply. The MAX4695 features break-before-make switching action with a t_{ON} = 30ns and t_{OFF} = 18ns at +3V.

When powered from a +2.7V supply, the device has a 60Ω (max) on-resistance (R_{ON}), with 3Ω (max) R_{ON} matching and 10Ω (max) R_{ON} flatness. The digital logic inputs are 1.8V-logic compatible from a +2.7V to +3.3V supply. The MAX4695 is available in both a space-saving 3mm x 3mm 12-pin TQFN package and a 10-pin µMAX® package.

Applications

MP3 Players
Battery-Operated Equipment
Relay Replacement
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
PCMCIA Cards
Cellular Phones
Modems

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Features

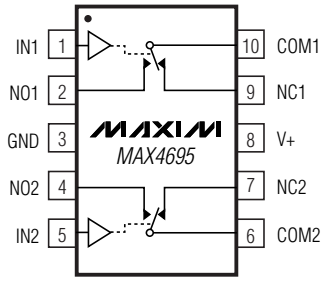
- **3mm x 3mm 12-Pin Thin QFN Package**
- **Guaranteed On-Resistance:**
  60Ω (max) (+2.7V supply)
  25Ω (typ) (+5V supply)
- **Guaranteed Match Between Channels: 3Ω (max)**
- **Guaranteed Flatness Over Signal Range:**
  10Ω (max)
- **Guaranteed Low Leakage Currents:**
  100pA (max) at +25°C
- **Switching Time: t_{ON} = 30ns, t_{OFF} = 18ns**
- **+1.8V to +5.5V Single-Supply Operation**
- **Rail-to-Rail Signal Handling**
- **-3dB Bandwidth: >300MHz**
- **Low Crosstalk: -82dB (1MHz)**
- **High Off-Isolation: -75dB (1MHz)**
- **Low 4pC Charge Injection**
- **THD: 0.03%**
- **+1.8V CMOS-Logic Compatible**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4695ETC	-40°C to 85°C	12 TQFN
MAX4695EUB	-40°C to 85°C	10 µMAX

Pin Configurations

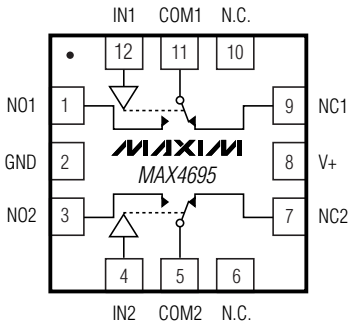
TOP VIEW



µMAX

MAX4695		
IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT



THIN QFN

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V to +6V
All Other Pins (Note 1) ..... -0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_ .....±20mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle) .....±40mA
ESD per Method 3015.7 .....2kV

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 4.7mW/°C above +70°C) 330mW
12-Pin Thin QFN (derate 16.7mW/°C above +70°C) 1333.3mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Note 1: Signals on IN_, COM_, NO_, and NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = +3V and T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +2.7V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +1.4V	+25°C		40	60	Ω
			T_{MIN} to T_{MAX}			70	
On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = +2.7V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +1.4V	+25°C		0.5	3	Ω
			T_{MIN} to T_{MAX}			4	
On-Resistance Flatness (Note 4)	$R_{FLAT\ (ON)}$	V+ = +2.7V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +1V, +1.4V, +1.8V	+25°C		6	10	Ω
			T_{MIN} to T_{MAX}			15	
NO_, NC_ Off-Leakage Current (Note 5)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = +3.3V, $V_{COM_}$ = +0.3V, +3V $V_{NO_}$ or $V_{NC_}$ = +3V, +0.3V	+25°C	-0.1	±0.01	+0.1	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 5)	$I_{COM_(ON)}$	V+ = +3.3V, $V_{COM_}$ = +0.3V, +3V $V_{NO_}$ or $V_{NC_}$ = +0.3V, +3V, or floating	+25°C	-0.2	±0.01	+0.2	nA
			T_{MIN} to T_{MAX}	-2		+2	
DYNAMIC							
Turn-On Time	t_{ON}	V_{NO} or $V_{NC_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		24	30	ns
			T_{MIN} to T_{MAX}			40	
Turn-Off Time	t_{OFF}	V_{NO} or $V_{NC_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		12	18	ns
			T_{MIN} to T_{MAX}			20	
Break-Before-Make Time (Note 6)	t_{BBM}	V_{NO} or $V_{NC_}$ = +1.5V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		12		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 4			4		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out, Figure 5			300		MHz
Off-Isolation (Note 7)	V_{ISO}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5			-75		dB

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.3V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = +3V and T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Crosstalk (Note 8)	V_{CT}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5			-82		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 2Vp-p, R_L = 600Ω			0.03		%
NO_, NC_ Off-Capacitance	$C_{NO_(OFF)}$, $C_{NC_(OFF)}$	f = 1MHz, $V_{NO_}$ or $V_{NC_}$ = GND, Figure 6			7		pF
COM_ On-Capacitance	$C_{COM_(ON)}$	f = 1MHz, $V_{NO_}$ or $V_{NC_}$ = GND, Figure 6			19		pF
DIGITAL I/O							
Input Logic High	V_{IH}			1.4			V
Input Logic Low	V_{IL}					0.5	V
Input Leakage Current	I_{IH}, I_{IL}	$V_{IN_}$ = 0 or V+		-1		+1	µA
SUPPLY							
Power-Supply Range	V+			1.8		5.5	V
Power-Supply Current	I+	V+ = +5.5V, $V_{IN_}$ = 0 or V+				1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = +5V and T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$			0		V+	V
On-Resistance	R_{ON}	V+ = +4.5V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +3.5V	+25°C		25	35	Ω
			T_{MIN} to T_{MAX}			40	
On-Resistance Match Between Channels (Note 3)	ΔR_{ON}	V+ = +4.5V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +3.5V	+25°C		0.5	2	Ω
			T_{MIN} to T_{MAX}			3	
On-Resistance Flatness (Note 4)	$R_{FLAT\ (ON)}$	V+ = +4.5V, $I_{COM_}$ = 1mA, $V_{NO_}$ or $V_{NC_}$ = +1V, +2.5V, +3.5V	+25°C		4	8	Ω
			T_{MIN} to T_{MAX}			10	
NO_, NC_ Off-Leakage Current (Note 5)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = +5.5V, $V_{COM_}$ = +1V, +4.5V $V_{NO_}$ or $V_{NC_}$ = +4.5V, +1V	+25°C	-0.1	±0.01	+0.1	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 5)	$I_{COM\ _(ON)}$	V+ = +5.5V, $V_{COM_}$ = +1V, +4.5V $V_{NO_}$ or $V_{NC_}$ = +1V, +4.5V, or floating	+25°C	-0.2	±0.01	+0.2	nA
			T_{MIN} to T_{MAX}	-2		+2	
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO_}$, $V_{NC_}$ = +3V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		17	25	ns
			T_{MIN} to T_{MAX}			30	
Turn-Off Time	t_{OFF}	$V_{NO_}$, $V_{NC_}$ = +3V, R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		8	15	ns
			T_{MIN} to T_{MAX}			20	

Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = +5V and T_A = +25°C.) (Notes 2, 9)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Break-Before-Make Time (Note 6)	t_{BBM}	$V_{NO_}$, $V_{NC_}$ = +3V, R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		9		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1.0nF, Figure 4			8		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, 50Ω in and out, Figure 5			300		MHz
Off-Isolation (Note 7)	V_{ISO}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5			-75		dB
Crosstalk (Note 8)	V_{CT}	f = 1MHz, R_L = 50Ω, C_L = 5pF, Figure 5			-82		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, 2Vp-p, R_L = 600Ω			0.02		%
DIGITAL I/O							
Input Logic High	V_{IH}			2.0			V
Input Logic Low	V_{IL}					0.8	V
Input Leakage Current	I_{IH}, I_{IL}	$V_{IN_}$ = 0 or V+		-1		+1	µA
SUPPLY							
Power-Supply Range	V+			1.8		5.5	V
Positive Supply Current	I+	V+ = +5.5V, V_{IN} = 0 or V+				1	µA

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: $\Delta_{RON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 5: Leakage currents are 100% tested at T_A = +85°C. Limits across the full temperature range are guaranteed by correlation.

Note 6: Guaranteed by design.

Note 7: Off-Isolation = $20\log_{10}(V_{COM_} / V_{NO_})$, $V_{COM_}$ = output, $V_{NO_}$ = input to off switch.

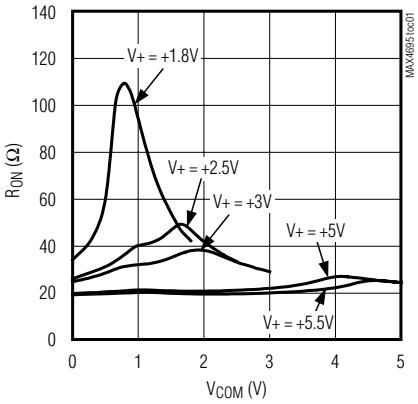
Note 8: Between any two switches.

Note 9: -40°C specifications are guaranteed by design.

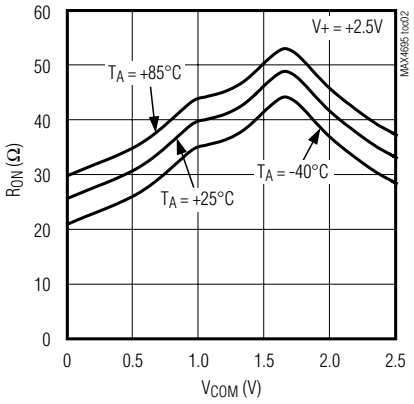
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

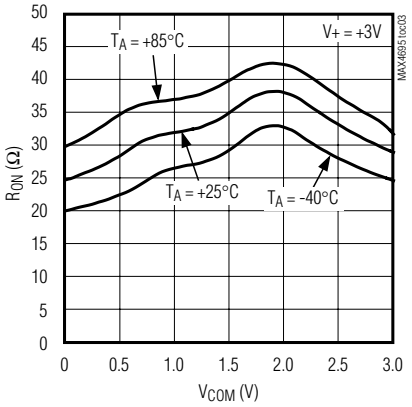
ON-RESISTANCE vs. V_{COM}



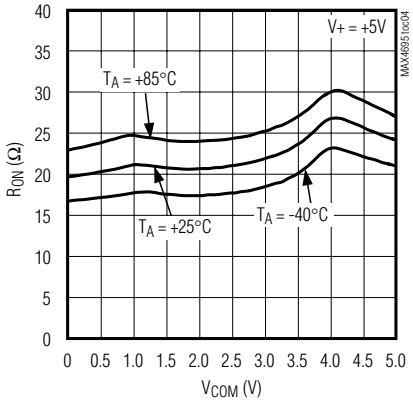
ON-RESISTANCE vs. V_{COM}



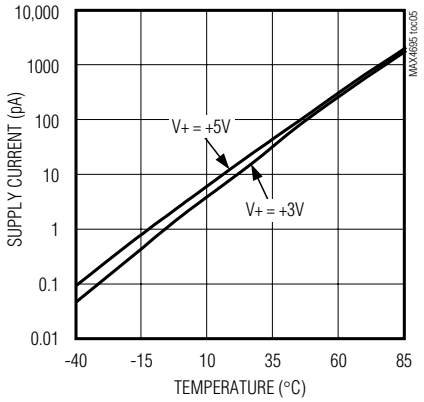
ON-RESISTANCE vs. V_{COM}



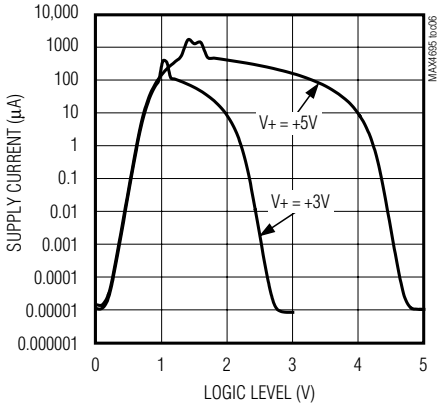
ON-RESISTANCE vs. V_{COM}



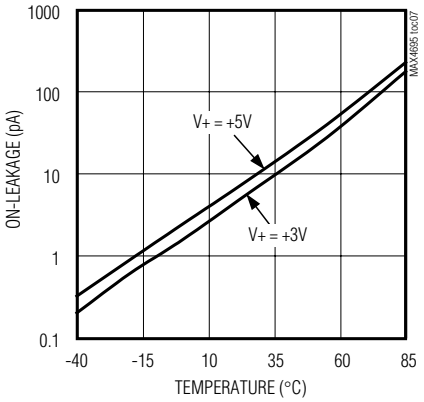
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



ON-LEAKAGE CURRENT vs. TEMPERATURE

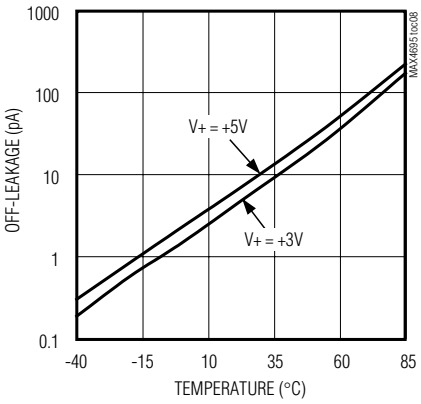


Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

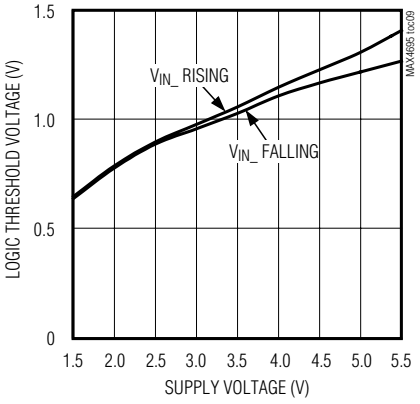
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

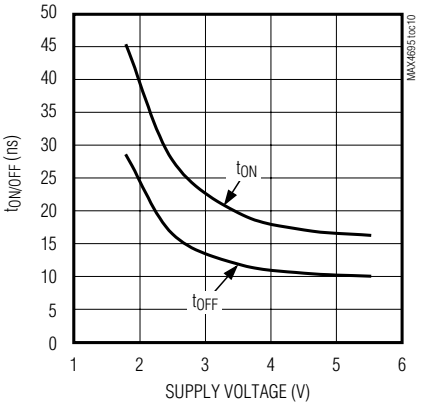
OFF-LEAKAGE CURRENT vs. TEMPERATURE



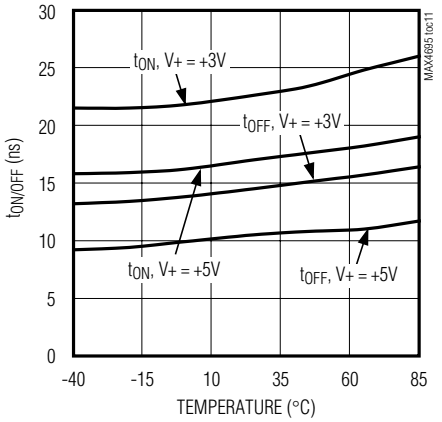
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



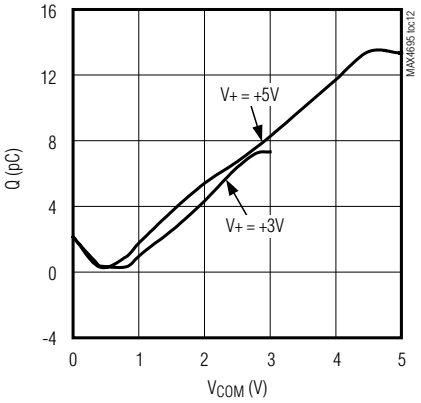
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



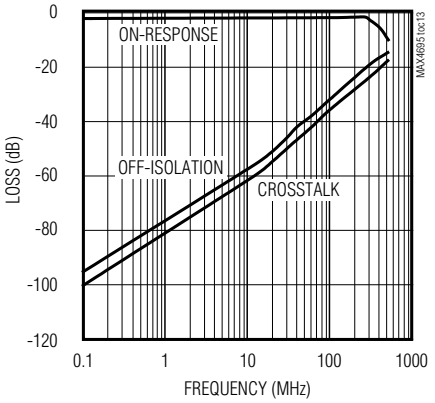
TURN-ON/OFF TIME vs. TEMPERATURE



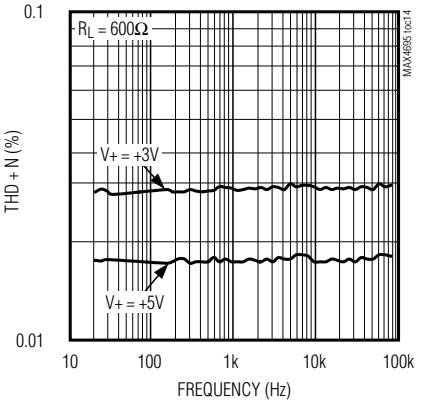
CHARGE INJECTION vs. V_{COM}



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
µMAX	TQFN		
1	12	IN1	Digital Control Input Switch 1
2	1	NO1	Analog Switch 1—Normally Open Terminal
3	2	GND	Ground
4	3	NO2	Analog Switch 2—Normally Open Terminal
5	4	IN2	Digital Control Input Switch 2
6	5	COM2	Analog Switch 2—Common Terminal
—	6, 10	N.C.	No Connection. Not internally connected.
7	7	NC2	Analog Switch 2—Normally Closed Terminal
8	8	V+	Positive Supply Voltage Input
9	9	NC1	Analog Switch 1—Normally Closed Terminal
10	11	COM1	Analog Common Switch 1

Detailed Description

The MAX4695 is a low-voltage, dual single-pole/double-throw (SPDT) analog switch that operates from a single +1.8V to +5.5V supply. When powered from a +2.7V supply, the device has a 60Ω (max) on-resistance (R_{ON}), with 3Ω (max) R_{ON} matching and 10Ω (max) R_{ON} flatness. The digital logic inputs are 1.8V-logic compatible from a +2.7V to +3.3V supply.

Applications Information

Digital Control Inputs

The MAX4695 logic inputs are 1.8V CMOS logic compatible for 3V operation and TTL compatible for 5V operation of V+. Driving IN_ rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) are passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add a small signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog range to a diode drop (about 0.7V) below V+ (for D1), and a diode drop above ground (for D2). On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V.

Adding protection diode D2 causes the logic threshold to be shifted relative to GND. TTL compatibility is not guaranteed when D2 is added.

Protection diodes D1 and D2 also protect against some overvoltage situations. In the circuit in Figure 1, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

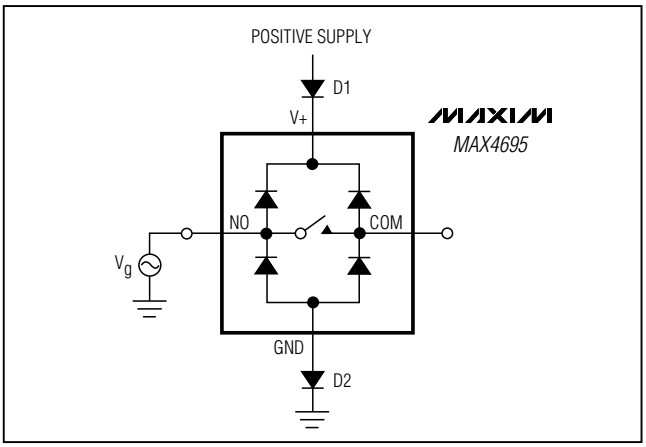


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

Test Circuits/Timing Diagrams

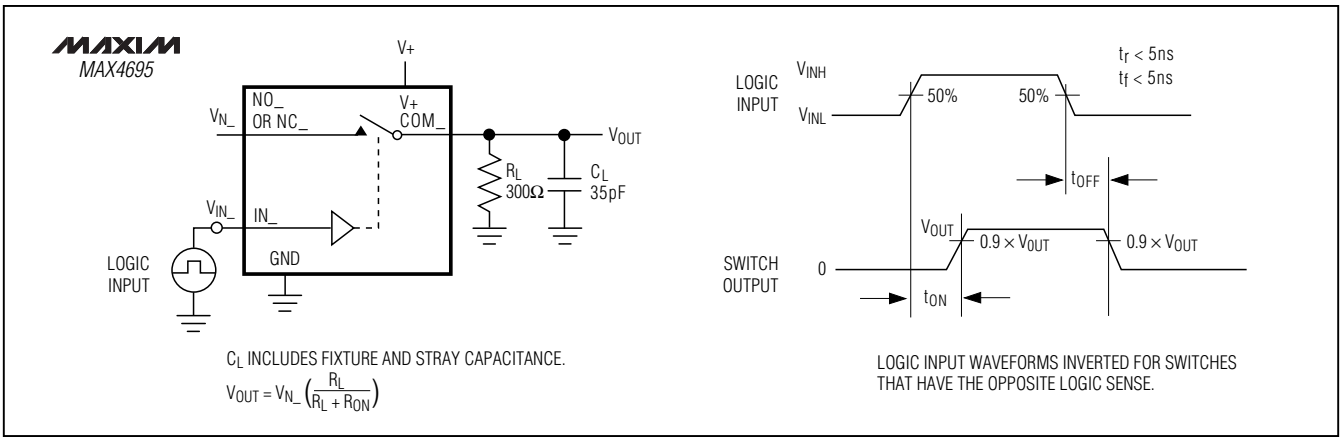


Figure 2. Switching Time

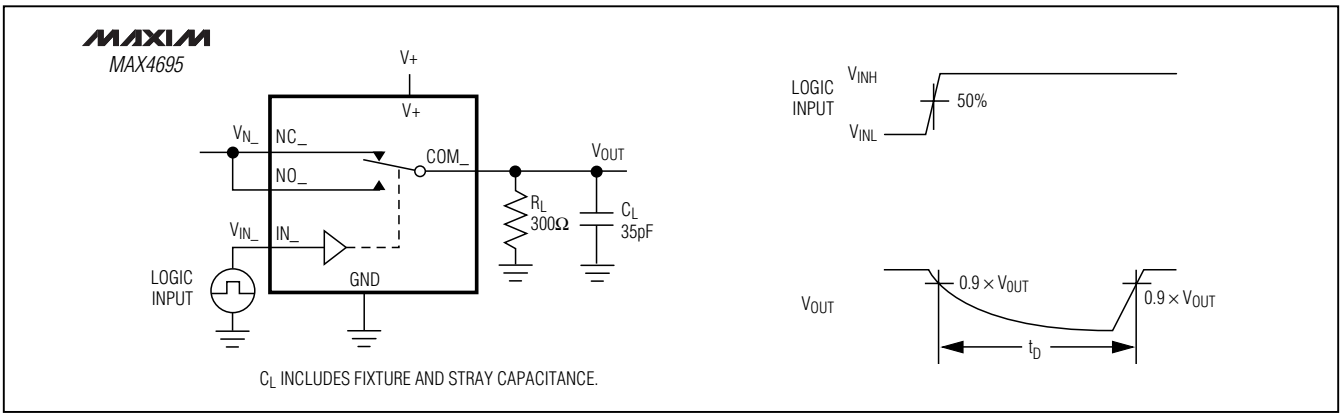


Figure 3. Break-Before-Make Interval

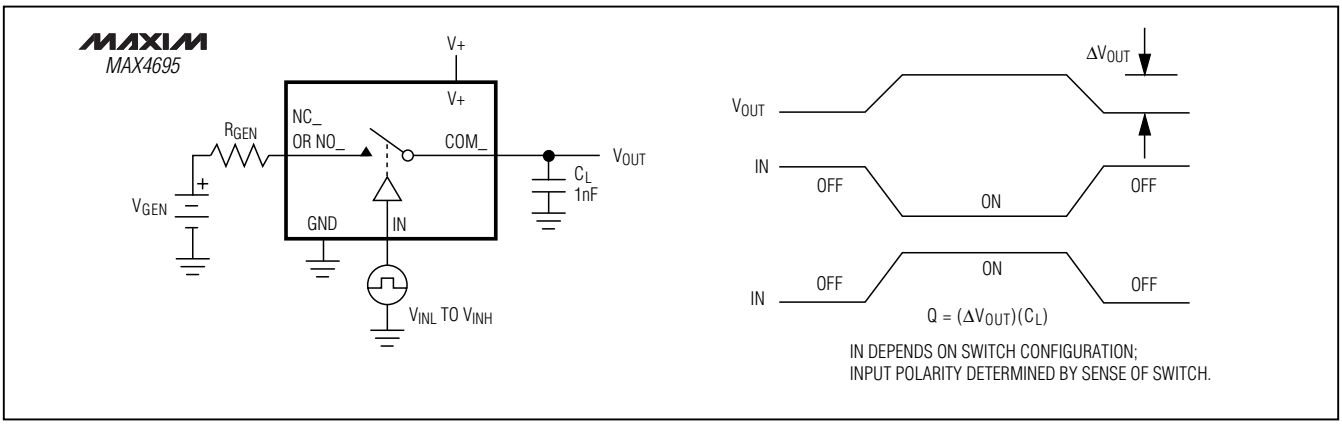


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

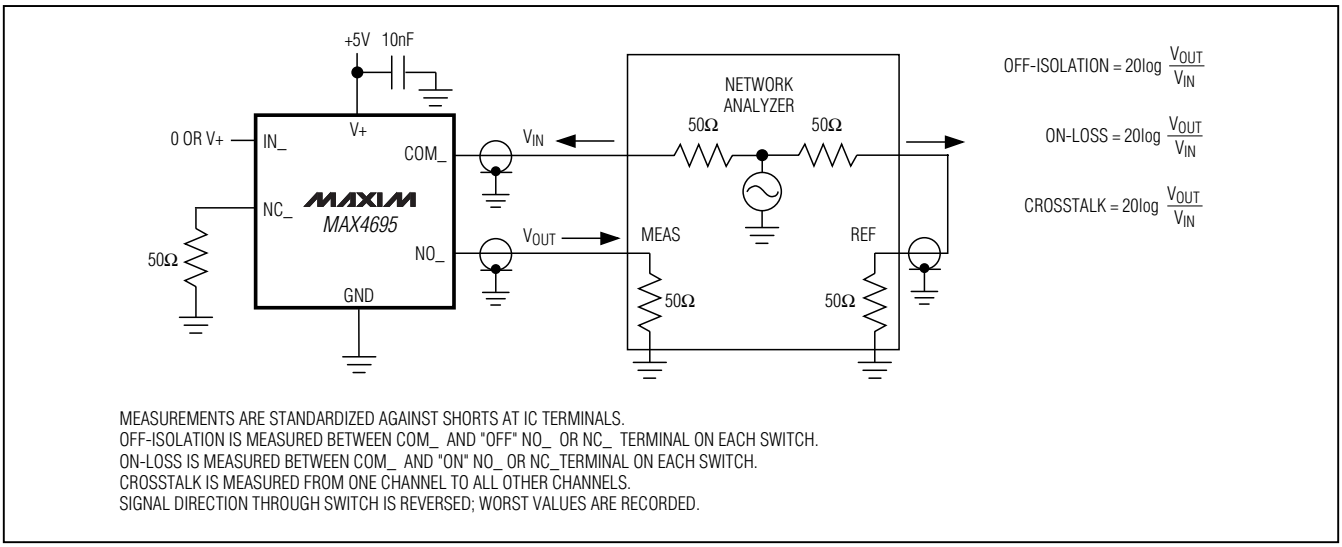


Figure 5. Off-Isolation/On-Channel Bandwidth, Crosstalk

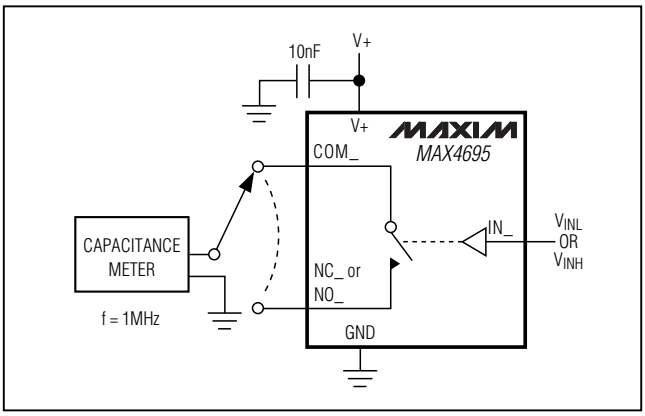


Figure 6. Channel Off/On-Capacitance

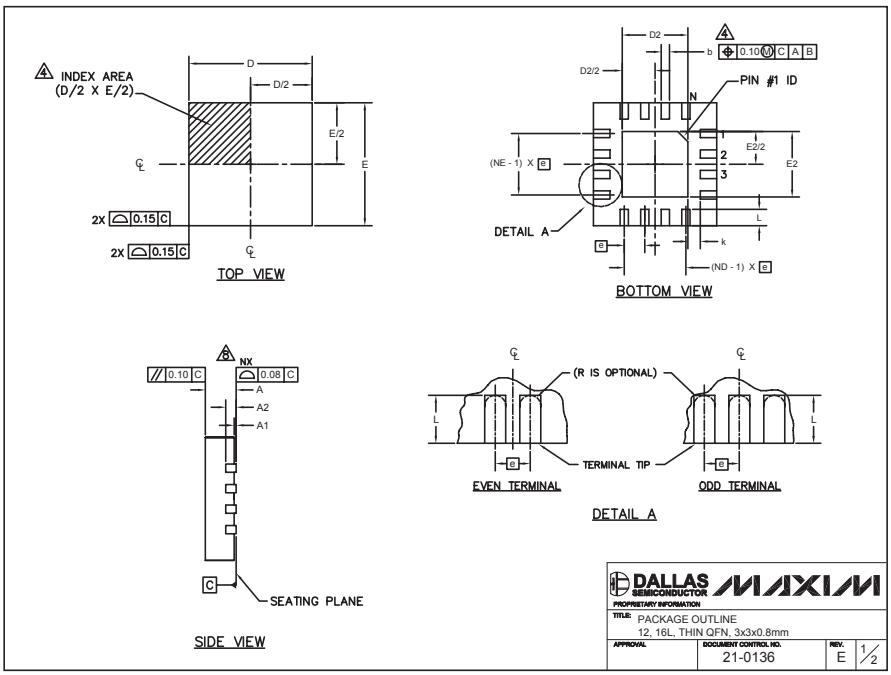
Chip Information

TRANSISTOR COUNT: 130

Low-Voltage, 60Ω Dual SPDT Analog Switch in Thin QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45∞	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45∞	WEED-2	NO

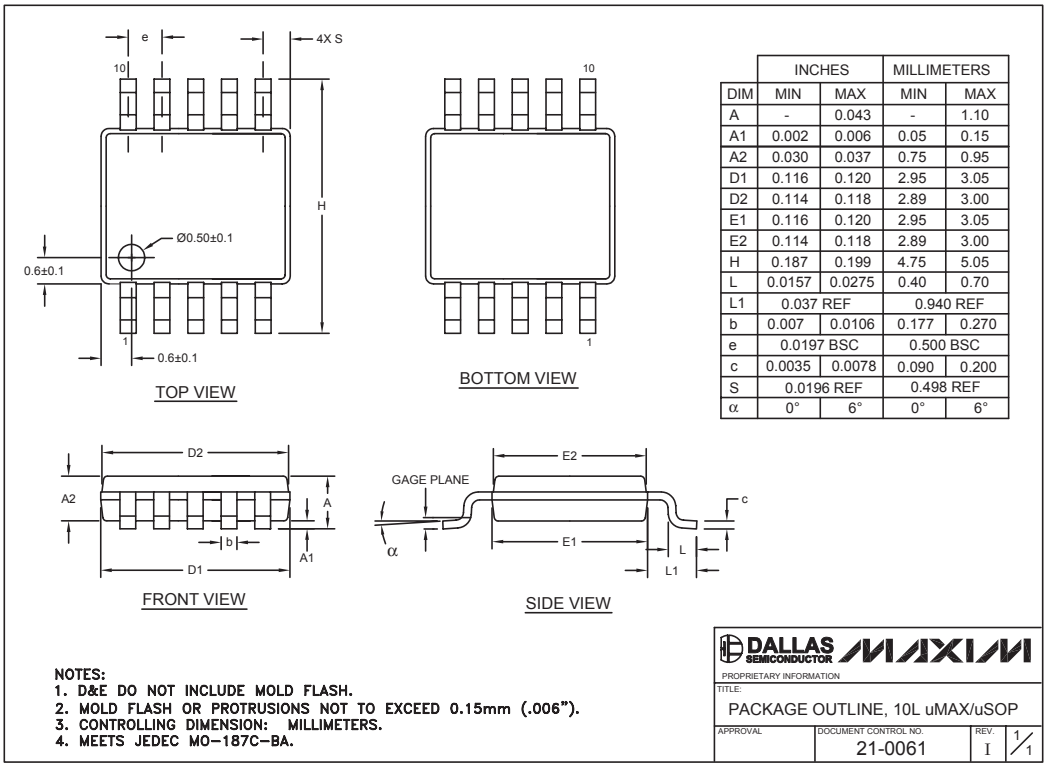
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12, 16L, THIN QFN, 3x3x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. E | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

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