Serial 16-Bit Multiplying DACs

FEATURES

- **SO-8 Package (LTC1595)**
- **DNL and INL: 1LSB Max**
- **Low Glitch Impulse: 1nV-s Typ**
- **Fast Settling to 1LSB: 2µs (with LT1468)**
- Pin Compatible with Industry Standard 12-Bit DACs: DAC8043 and DAC8143/AD7543
- 4-Quadrant Multiplication
- Low Supply Current: 10µA Max
- Power-On Reset
  - LTC1595/LTC1596: Resets to Zero-Scale
  - LTC1596-1: Resets to Mid-Scale
- 3-Wire SPI and MICROWIRE Compatible Serial Interface
- Daisy-Chain Serial Output (LTC1596)
- Asynchronous Clear Input
  - LTC1596: Clears to Zero-Scale
  - LTC1596-1: Clears to Mid-Scale

APPLICATIONS

- Process Control and Industrial Automation
- Software Controlled Gain Adjustment
- Digitally Controlled Filter and Power Supplies
- Automatic Test Equipment

DESCRIPTION

The LTC®1595/LTC1596/LTC1596-1 are serial input, 16-bit multiplying current output DACs. The LTC1595 is pin and hardware compatible with the 12-bit DAC8043 and comes in 8-pin PDIP and SO packages. The LTC1596 is pin and hardware compatible with the 12-bit DAC8143/AD7543 and comes in the 16-pin SO wide package.

Both are specified over the industrial temperature range. Sensitivity of INL to op amp V_{OS} is reduced by five times compared to the industry standard 12-bit DACs, so most systems can be easily upgraded to true 16-bit resolution and linearity without requiring more precise op amps.

These DACs include an internal deglitching circuit that reduces the glitch impulse by more than ten times to less than 1nV-s typ.

The DACs have a clear input and a power-on reset. The LTC1595 and LTC1596 reset to zero-scale. The LTC1596-1 is a version of the LTC1596 that resets to mid-scale.

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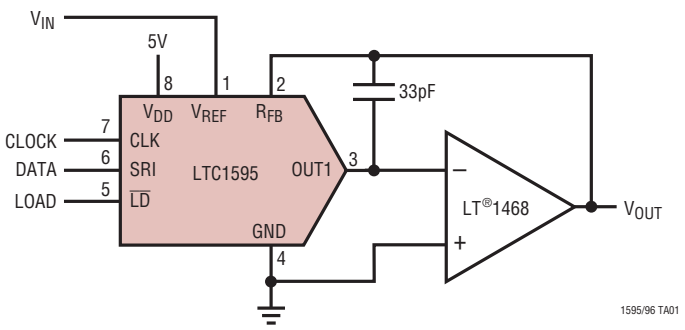
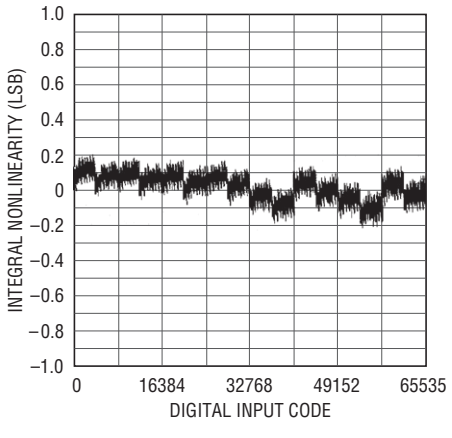
TYPICAL APPLICATION

SO-8 Multiplying 16-Bit DAC Has Easy 3-Wire Serial Interface



Integral Nonlinearity

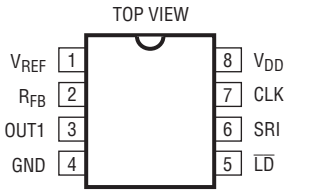


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{DD} to AGND ..... –0.5V to 7V
V_{DD} to DGND ..... –0.5V to 7V
AGND to DGND ..... V_{DD} + 0.5V
DGND to AGND ..... V_{DD} + 0.5V
V_{REF} to AGND, DGND ..... ±25V
R_{FB} to AGND, DGND ..... ±25V
Digital Inputs to DGND ..... –0.5V to (V_{DD} + 0.5V)
V_{OUT1}, V_{OUT2} to AGND ..... –0.5V to (V_{DD} + 0.5V)
Maximum Junction Temperature ..... 150°C
Operating Temperature Range
LTC1595C/LTC1596C/LTC1596-1C ..... 0°C to 70°C
LTC1595I/LTC1596I/LTC1596-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

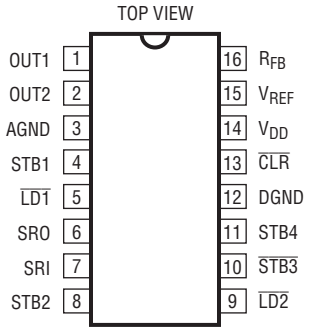
PIN CONFIGURATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S)



SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (SW)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1595ACN8#PBF	LTC1595ACN8#TRPBF	LTC1595ACN8	8-Lead PDIP	0°C to 70°C
LTC1595ACS8#PBF	LTC1595ACS8#TRPBF	1595A	8-Lead Plastic SO	0°C to 70°C
LTC1595BCN8#PBF	LTC1595BCN8#TRPBF	LTC1595BCN8	8-Lead PDIP	0°C to 70°C
LTC1595BCS8#PBF	LTC1595BCS8#TRPBF	1595B	8-Lead Plastic SO	0°C to 70°C
LTC1595CCN8#PBF	LTC1595CCN8#TRPBF	LTC1595CCN8	8-Lead PDIP	0°C to 70°C
LTC1595CCS8#PBF	LTC1595CCS8#TRPBF	1595C	8-Lead Plastic SO	0°C to 70°C
LTC1595AIN8#PBF	LTC1595AIN8#TRPBF	LTC1595AIN8	8-Lead PDIP	–40°C to 85°C
LTC1595AIS8#PBF	LTC1595AIS8#TRPBF	1595AI	8-Lead Plastic SO	–40°C to 85°C
LTC1595BIN8#PBF	LTC1595BIN8#TRPBF	LTC1595BIN8	8-Lead PDIP	–40°C to 85°C
LTC1595BIS8#PBF	LTC1595BIS8#TRPBF	1595BI	8-Lead Plastic SO	–40°C to 85°C
LTC1595CIN8#PBF	LTC1595CIN8#TRPBF	LTC1595CIN8	8-Lead PDIP	–40°C to 85°C
LTC1595CIS8#PBF	LTC1595CIS8#TRPBF	1595CI	8-Lead Plastic SO	–40°C to 85°C
LTC1596ACSW#PBF	LTC1596ACSW#TRPBF	LTC1596ACSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596BCSW#PBF	LTC1596BCSW#TRPBF	LTC1596BCSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596CCSW#PBF	LTC1596CCSW#TRPBF	LTC1596CCSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596AISW#PBF	LTC1596AISW#TRPBF	LTC1596AISW	16-Lead Plastic SO Wide	–40°C to 85°C
LTC1596BISW#PBF	LTC1596BISW#TRPBF	LTC1596BISW	16-Lead Plastic SO Wide	–40°C to 85°C
LTC1596CISW#PBF	LTC1596CISW#TRPBF	LTC1596CISW	16-Lead Plastic SO Wide	–40°C to 85°C
LTC1596-1ACSW#PBF	LTC1596-1ACSW#TRPBF	LTC1596-1ACSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596-1BCSW#PBF	LTC1596-1BCSW#TRPBF	LTC1596-1BCSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596-1CCSW#PBF	LTC1596-1CCSW#TRPBF	LTC1596-1CCSW	16-Lead Plastic SO Wide	0°C to 70°C
LTC1596-1AISW#PBF	LTC1596-1AISW#TRPBF	LTC1596-1AISW	16-Lead Plastic SO Wide	–40°C to 85°C
LTC1596-1BISW#PBF	LTC1596-1BISW#TRPBF	LTC1596-1BISW	16-Lead Plastic SO Wide	–40°C to 85°C
LTC1596-1CISW#PBF	LTC1596-1CISW#TRPBF	LTC1596-1CISW	16-Lead Plastic SO Wide	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1595A/96A/96-1A MIN	LTC1595A/96A/96-1A TYP	LTC1595A/96A/96-1A MAX	LTC1595B/96B/96-1B MIN	LTC1595B/96B/96-1B TYP	LTC1595B/96B/96-1B MAX	LTC1595C/96C/96-1C MIN	LTC1595C/96C/96-1C TYP	LTC1595C/96C/96-1C MAX	UNITS
Accuracy													
	Resolution		●	16			16			16			Bits
	Monotonicity		●	16			16			15			Bits
INL	Integral Nonlinearity	(Note 2) T_A = 25°C			±0.25	±1			±2			±4	LSB
		T_{MIN} to T_{MAX}	●		±0.35	±1			±2			±4	LSB
DNL	Differential Nonlinearity	T_A = 25°C			±0.2	±1			±1			±2	LSB
		T_{MIN} to T_{MAX}	●		±0.2	±1			±1			±2	LSB
GE	Gain Error	(Note 3) T_A = 25°C			2	±16			±16			±32	LSB
		T_{MIN} to T_{MAX}	●		3	±16			±32			±32	LSB

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Temperature Coefficient	(Note 4) ΔGain/ΔTemperature	●		1	2	ppm/°C
$I_{LEAKAGE}$	OUT1 Leakage Current	(Note 5) T_A = 25°C				±3	nA
		T_{MIN} to T_{MAX}	●			±15	nA
	Zero-Scale Error	T_A = 25°C				±0.2	LSB
		T_{MIN} to T_{MAX}	●			±1	LSB
PSRR	Power Supply Rejection	V_{DD} = 5V ±10%	●		±1	±2	LSB/V
Reference Input							
R_{REF}	V_{REF} Input Resistance	(Note 6)	●	5	7	10	kΩ
AC Performance							
	Output Current Settling Time	(Notes 7, 8)			1		µs
	Mid-Scale Glitch Impulse	Using LT1122 Op Amp, $C_{FEEDBACK}$ = 33pF			1		nV-s
	Digital-to-Analog Glitch Impulse	Full-Scale Transition, V_{REF} = 0V, Using LT1122 Op Amp, $C_{FEEDBACK}$ = 33pF			2		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 9)			108		dB
	Equivalent DAC Thermal Noise Voltage Density	(Note 10) f = 1kHz			11		$nV/\sqrt{Hz}$
Analog Outputs (Note 4)							
C_{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s, C_{OUT1}	●		115	130	pF
		DAC Register Loaded to All 0s, C_{OUT1}	●		70	80	pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 4) V_{IN} = 0V	●			8	pF
Digital Outputs: SRO (LTC1596/LTC1596-1)							
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = 1.6mA	●			0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1595)							
t_{DS}	Serial Input to CLK Setup Time		●	30	5		ns
t_{DH}	Serial Input to CLK Hold Time		●	30	5		ns
t_{SRI}	Serial Input Data Pulse Width		●	60			ns
t_{CH}	Clock Pulse Width High		●	60			ns
t_{CL}	Clock Pulse Width Low		●	60			ns
t_{LD}	Load Pulse Width		●	60			ns
t_{ASB}	LSB Clocked into Input Register to DAC Register Load Time		●	0			ns

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Timing Characteristics (LTC1596/LTC1596-1)							
t_{DS1}	Serial Input to Strobe Setup Time	STB1 Used as the Strobe	●	30	5		ns
t_{DS2}		STB2 Used as the Strobe	●	20	–5		ns
t_{DS3}		$\overline{STB3}$ Used as the Strobe	●	25	0		ns
t_{DS4}		STB4 Used as the Strobe	●	20	–5		ns
t_{DH1}	Serial Input to Strobe Hold Time	STB1 Used as the Strobe	●	30	5		ns
t_{DH2}		STB2 Used as the Strobe	●	40	15		ns
t_{DH3}		$\overline{STB3}$ Used as the Strobe	●	35	10		ns
t_{DH4}		STB4 Used as the Strobe	●	40	15		ns
t_{SRI}	Serial Input Data Pulse Width		●	60			ns
t_{STB1} to t_{STB4}	Strobe Pulse Width	(Note 11)	●	60			ns
$t_{\overline{STB1}}$ to $t_{\overline{STB4}}$	$\overline{Strobe}$ Pulse Width	(Note 12)	●	60			ns
$t_{\overline{LD1}}$, $t_{\overline{LD2}}$	$\overline{LD}$ Pulse Width		●	60			ns
t_{ASB}	LSB Strobed Into Input Register to Load DAC Register Time		●	0			ns
t_{CLR}	Clear Pulse Width		●	100			ns
t_{PD1}	STB1 to SRO Propagation Delay	C_L = 50pF	●	30		150	ns
t_{PD}	STB2, $\overline{STB3}$, STB4 to SRO Propagation Delay	C_L = 50pF	●	30		200	ns
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD}	●		1.5	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ±1LSB = ±0.0015% of full-scale = ±15.3ppm of full-scale.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: I_{OUT1} with DAC register loaded with all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: OUT1 load = 100Ω in parallel with 13pF.

Note 8: To 0.0015% for a full-scale change, measured from the falling edge of $\overline{LD1}$, $\overline{LD2}$ or $\overline{LD}$.

Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s; op amp = LT1007.

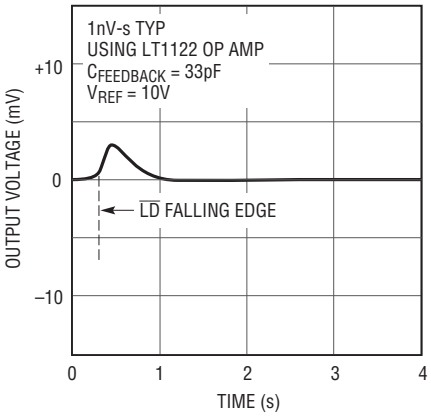
Note 10: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K); R = resistance (Ω); T = temperature (°K); B = bandwidth (Hz).

Note 11: Minimum high time for STB1, STB2, STB4. Minimum low time for $\overline{STB3}$.

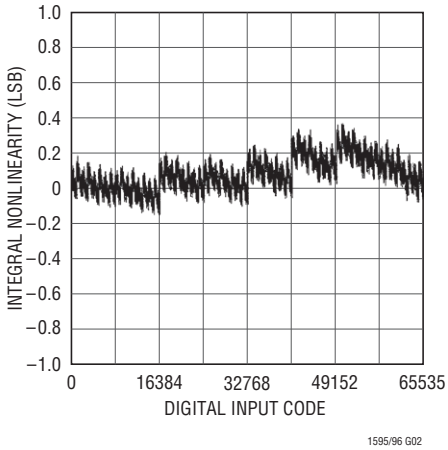
Note 12: Minimum low time for STB1, STB2, STB4. Minimum high time for $\overline{STB3}$.

TYPICAL PERFORMANCE CHARACTERISTICS

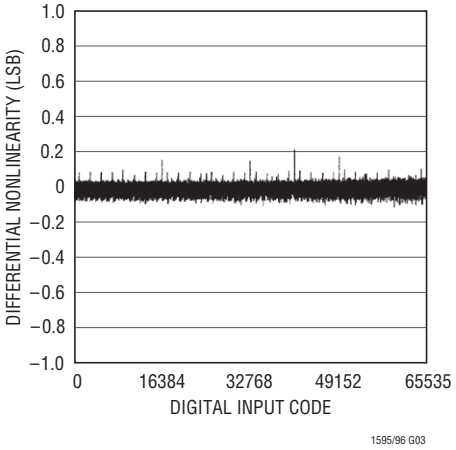
Mid-Scale Glitch Impulse



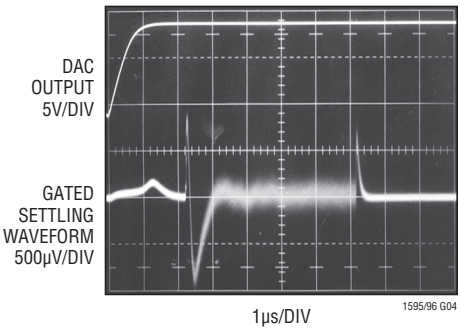
Integral Nonlinearity (INL)



Differential Nonlinearity (INL)

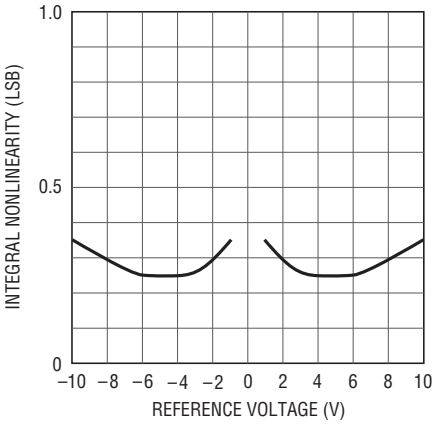


Full-Scale Settling Waveform

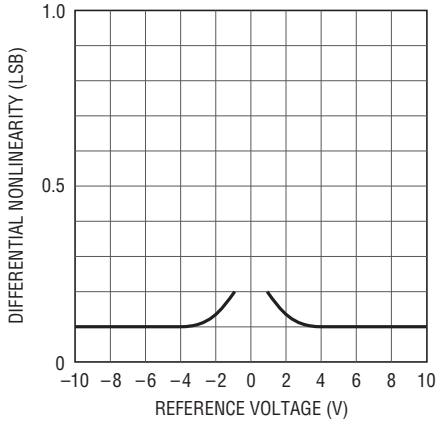


USING LT1122 OP AMP
$C_{FEEDBACK}$ = 33pF

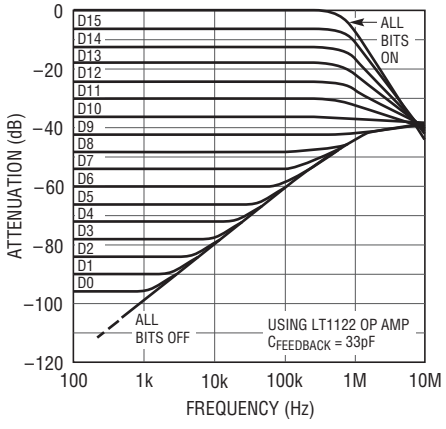
Integral Nonlinearity vs Reference Voltage



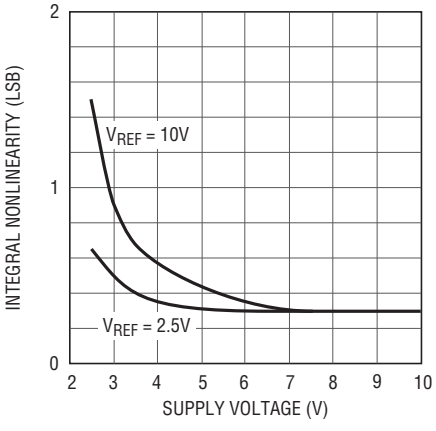
Differential Nonlinearity vs Reference Voltage



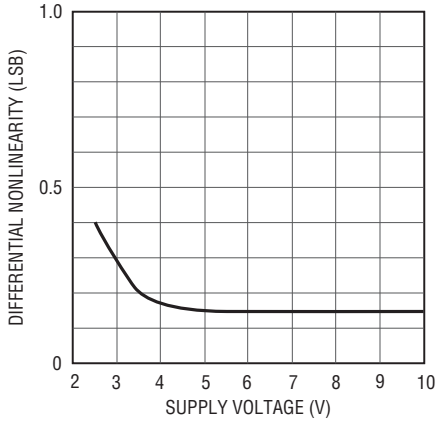
Multiplying Mode Frequency Response vs Digital Code



Integral Nonlinearity vs Supply Voltage

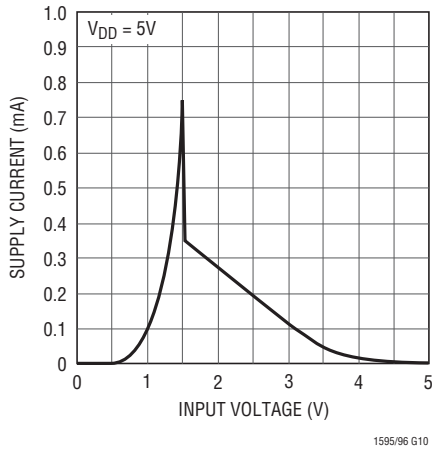


Differential Nonlinearity vs Supply Voltage

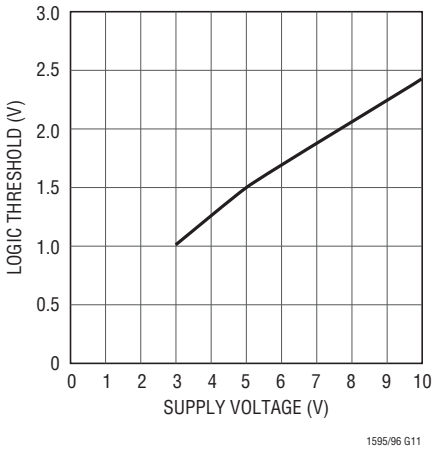


TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Logic Input Voltage



Logic Threshold vs Supply Voltage



PIN FUNCTIONS

LTC1595

V_{REF} (Pin 1): Reference Input.

R_{FB} (Pin 2): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

OUT1 (Pin 3): Current Output Pin. Tie to inverting input of current to voltage converter op amp.

GND (Pin 4): Ground Pin.

$\overline{LD}$ (Pin 5): The Serial Interface Load Control Input. When $\overline{LD}$ is pulled low, data is loaded from the shift register into the DAC register, updating the DAC output.

SRI (Pin 6): The Serial Data Input. Data on the SRI pin is latched into the shift register on the rising edge of the serial clock. Data is loaded MSB first.

CLK (Pin 7): The Serial Interface Clock Input.

V_{DD} (Pin 8): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

LTC1596/LTC1596-1

OUT1 (Pin 1): True Current Output Pin. Tie to inverting input of current to voltage converter op amp.

OUT2 (Pin 2): Complement Current Output Pin. Tie to analog ground.

AGND (Pin 3): Analog Ground Pin.

STB1, STB2, $\overline{STB3}$, STB4 (Pins 4, 8, 10, 11): Serial Interface Clock Inputs. STB1, STB2 and STB4 are rising edge triggered inputs. $\overline{STB3}$ is a falling edge triggered input (see Truth Tables).

$\overline{LD1}$, $\overline{LD2}$ (Pins 5, 9): Serial Interface Load Control Inputs. When $\overline{LD1}$ and $\overline{LD2}$ are pulled low, data is loaded from the shift register into the DAC register, updating the DAC output (see Truth Tables).

SRO (Pin 6): The Output of the Shift Register. Becomes valid on the active edge of the serial clock.

SRI (Pin 7): The Serial Data Input. Data on the SRI pin is latched into the shift register on the active edge of the serial clock. Data is loaded MSB first.

DGND (Pin 12): Digital Ground Pin.

$\overline{CLR}$ (Pin 13): The Clear Pin for the DAC. Clears DAC to zero-scale when pulled low on LTC1596. Clears DAC to mid-scale when pulled low on LTC1596-1. This pin should be tied to V_{DD} for normal operation.

V_{DD} (Pin 14): The Positive Supply Input. $4.5V \leq V_{DD} \leq 5.5V$. Requires a bypass capacitor to ground.

V_{REF} (Pin 15): Reference Input.

R_{FB} (Pin 16): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

TRUTH TABLES

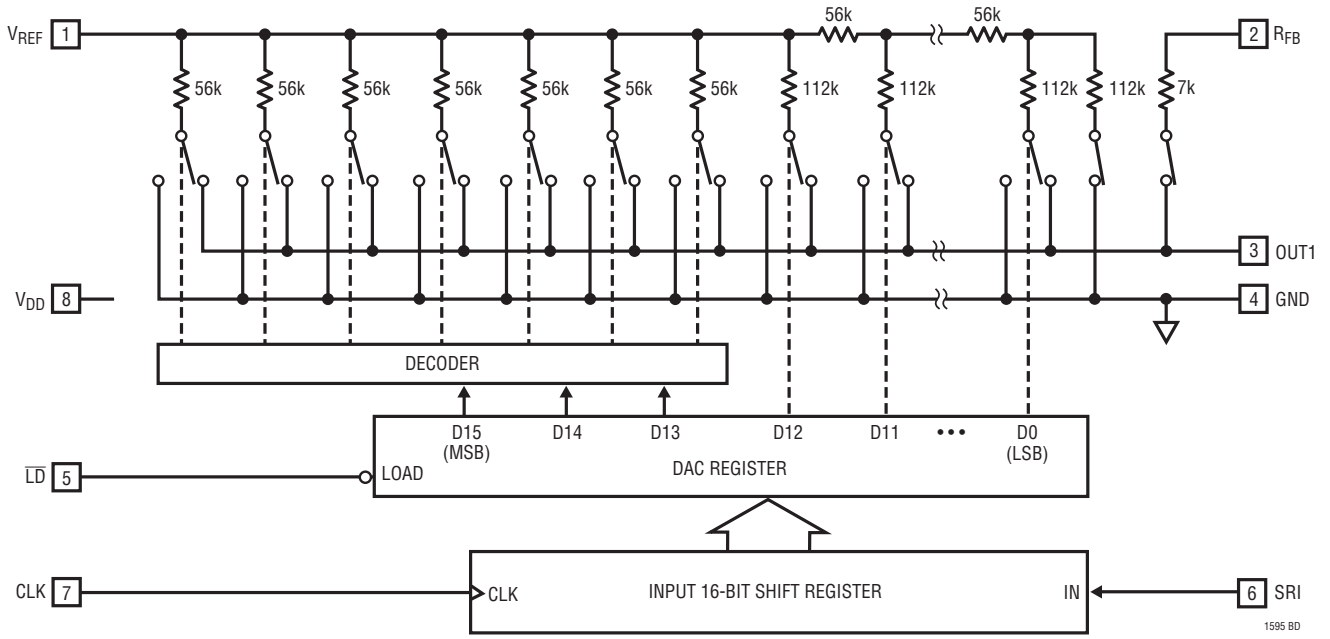
Table 1. LTC1596/LTC1596-1 Input Register

CONTROL INPUTS				
STB1	STB2	$\overline{STB3}$	STB4	INPUT REGISTER AND SRO OPERATION
↑	0	1	0	Serial Data Bit on SRI Loaded Into Input Register, MSB First Data Bit or SRI Appears on SRO Pin After 16 Clocked Bits
0	↑	1	0	
0	0	↓	0	
0	0	1	↑	
1	X	X	X	No Input Register Operation No SRO Operation
X	1	X	X	
X	X	0	X	
X	X	X	1	

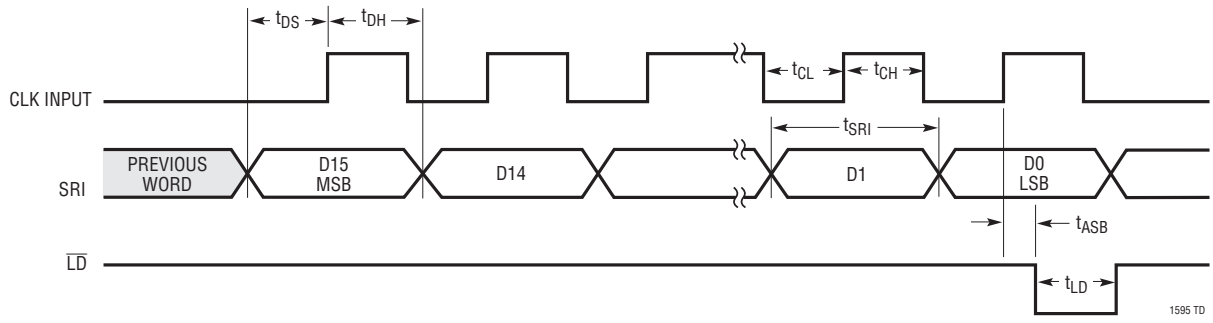
Table 2. LTC1596/LTC1596-1 DAC Register

CONTROL INPUTS			
$\overline{CLR}$	$\overline{LD1}$	$\overline{LD2}$	DAC Register Operation
0	X	X	Reset DAC Register and Input Register to All 0s (LTC1596) or to Mid-Scale (LTC1596-1) (Asynchronous Operation)
1	1	X	No DAC Register Operation
1	X	1	
1	0	0	Load DAC Register with the Contents of Input Register

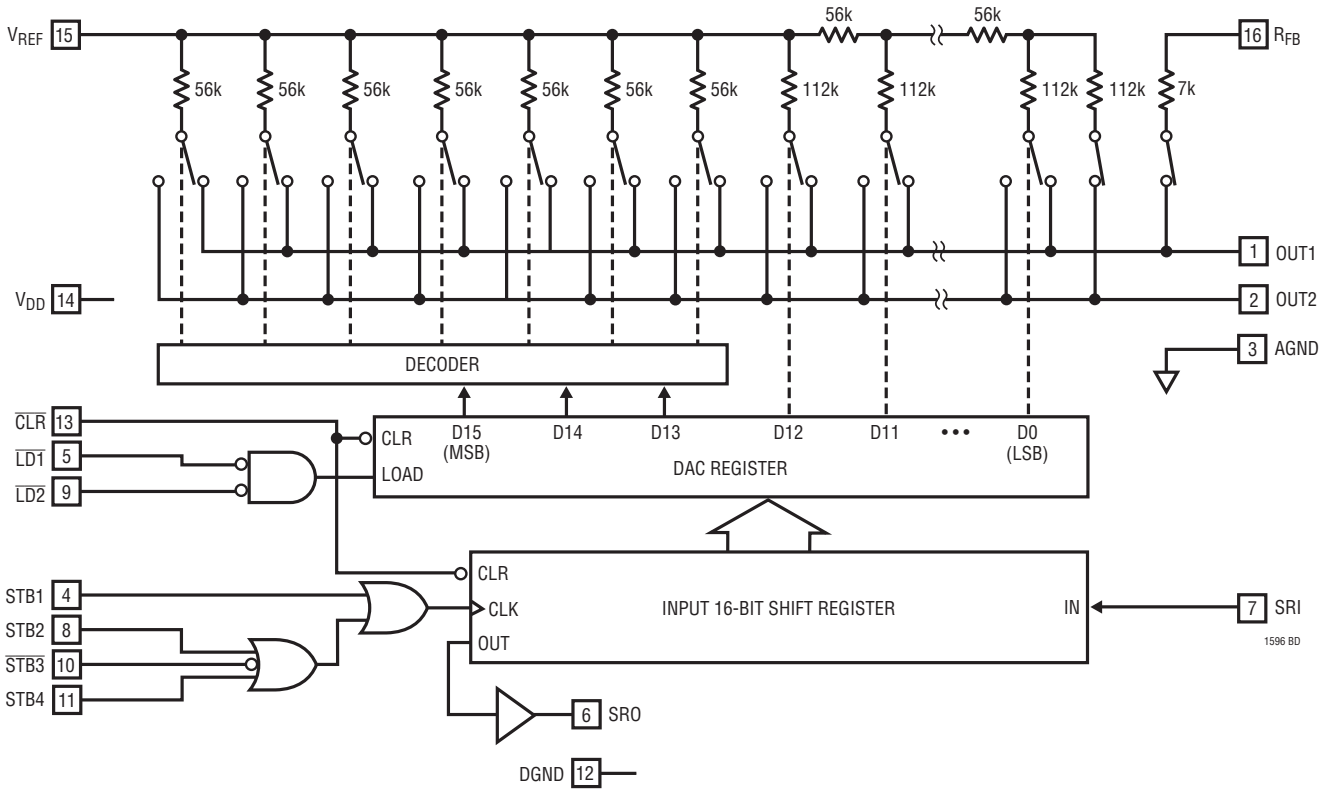
BLOCK DIAGRAM (LTC1595)



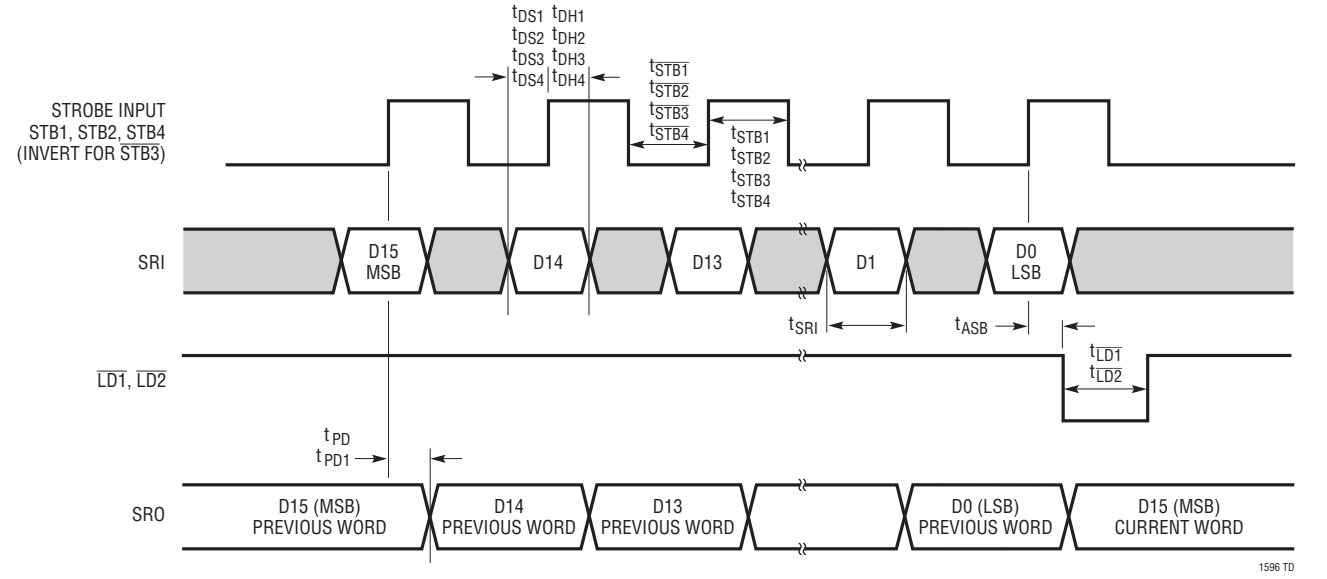
TIMING DIAGRAM (LTC1595)



BLOCK DIAGRAM (LTC1596/LTC1596-1)



TIMING DIAGRAM (LTC1596/LTC1596-1)



APPLICATIONS INFORMATION

Description

The LTC1595/LTC1596 are 16-bit multiplying DACs which have serial inputs and current outputs. They use precision R/2R technology to provide exceptional linearity and stability. The devices operate from a single 5V supply and provide ±10V reference input and voltage output ranges when used with an external op amp. These devices have a proprietary deglitcher that reduces glitch impulse to 1nV-s over a 0V to 10V output range.

Serial I/O

The LTC1595/LTC1596 have SPI/MICROWIRE compatible serial ports that accept 16-bit serial words. Data is accepted MSB first and loaded with a load pin.

The 8-pin LTC1595 has a 3-wire interface. Data is shifted into the SRI data input on the rising edge of the CLK pin. At the end of the data transfer, data is loaded into the DAC register by pulling the $\overline{LD}$ pin low (see LTC1595 Timing Diagram).

The 16-pin LTC1596 can operate in identical fashion to the LTC1595 but offers additional pins for flexibility. Four clock pins are available STB1, STB2, $\overline{STB3}$ and STB4. STB1, STB2 and STB4 operate like the CLK pin of the LTC1595, capturing data on their rising edges. $\overline{STB3}$ captures data on its falling edge (see Truth Table 1).

The LTC1596 has two load pins, $\overline{LD1}$ and $\overline{LD2}$. To load data, both pins must be taken low. If one of the pins is grounded, the other pin will operate identically to LTC1595's $\overline{LD}$ pin. An asynchronous clear input ($\overline{CLR}$) resets the LTC1596 to zero-scale (and the LTC1596-1 to mid-scale) when pulled low (see Truth Table 2).

The LTC1596 also has a data output pin SRO that can be connected to the SRI input of another DAC to daisy chain multiple DACs on one 3-wire interface (see LTC1596 Timing Diagram).

Unipolar (2-Quadrant Multiplying) Mode (V_{OUT} = 0V to $-V_{REF}$)

The LTC1595/LTC1596 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuits shown give a precision unipolar 0V to 10V output swing.

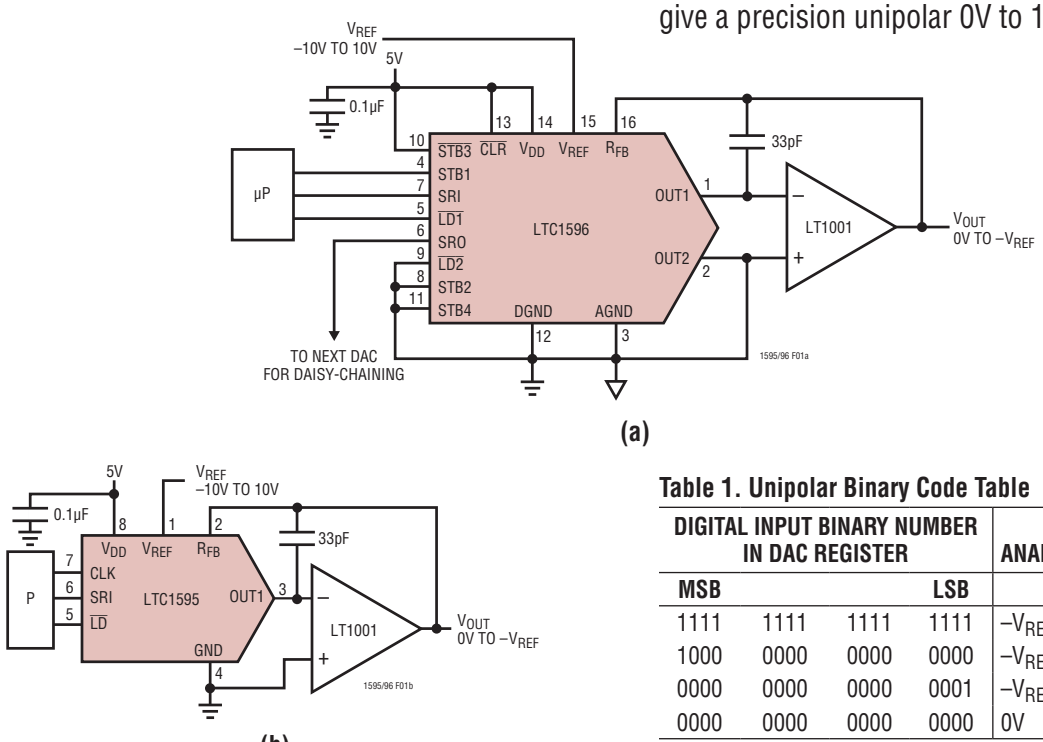


Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	$-V_{REF}$ (65,535/65,536)
1000	0000	0000	0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000	0000	0000	0001	$-V_{REF}$ (1/65,536)
0000	0000	0000	0000	0V

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$

APPLICATIONS INFORMATION

Bipolar (4-Quadrant Multiplying) Mode ($V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1595/LTC1596 can be used with a dual op amp and three external resistors to provide 4-quadrant multiplying operation as shown in Figure 2 (last page). With a fixed 10V reference, the circuits shown give a precision bipolar –10V to 10V output swing. Using the LTC1596-1 will cause the power-on reset and clear pin to reset the DAC to mid-scale (bipolar zero).

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC1595/LTC1596, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For example, a 500µV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For example, the same 500µV op amp offset will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}) = I_{BIAS}(R_{REF}) = I_{BIAS}(7k)$. Table 2 shows a selection of LTC op amps which are suitable for use with the LTC1595/LTC1596. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74, "*Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*"

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. I_{OUT2} (LTC1596) and GND (LTC1595) must be tied to the star ground with as low a resistance as possible.

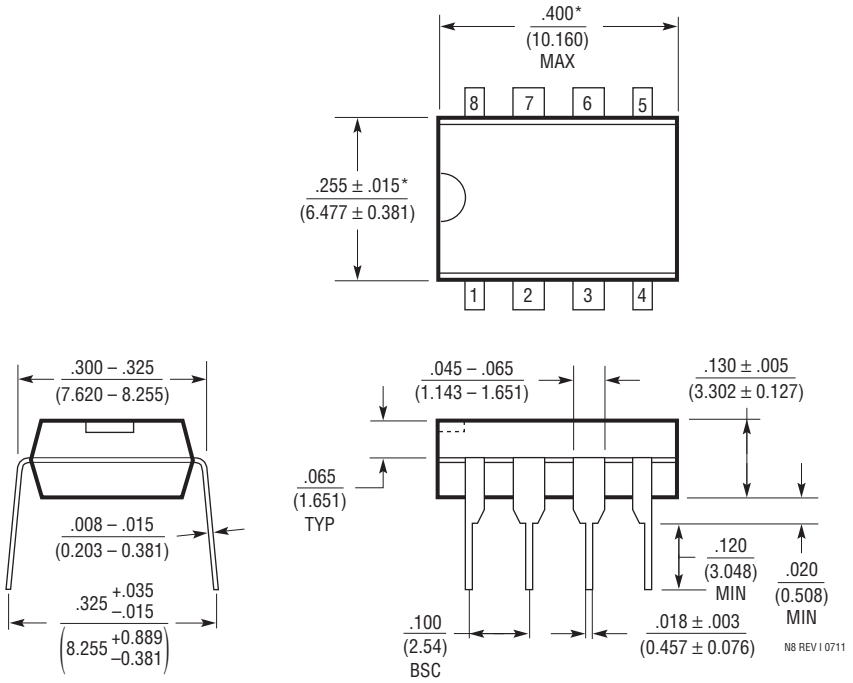
Table 2. 16-Bit Settling Time for Various Amplifiers Driven by the LT1595 DAC. LT1468 (Shaded) Offers Fastest Settling Time While Maintaining Accuracy Over Temperature

AMPLIFIER	CONSERVATIVE SETTLING TIME AND COMPENSATION VALUE		COMMENTS
LT1001	120µs	100pF	Good Low Speed Choice
LT1007	19µs	100pF	I_B Gives ≈1LSB Error at 25°C
LT1013	75µs	150pF	≈1LSB Error Due to V_{OS} Over Temperature
LT1077	200µs	100pF	
LT1097	120µs	75pF	Good Low Speed Choice
LT1112	120µs	100pF	Good Low Speed Choice Dual
LT1178	450µs	100pF	Low Power Dual
LT1468	2.5µs	30pF	Fastest Settling with 16-Bit Performance

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



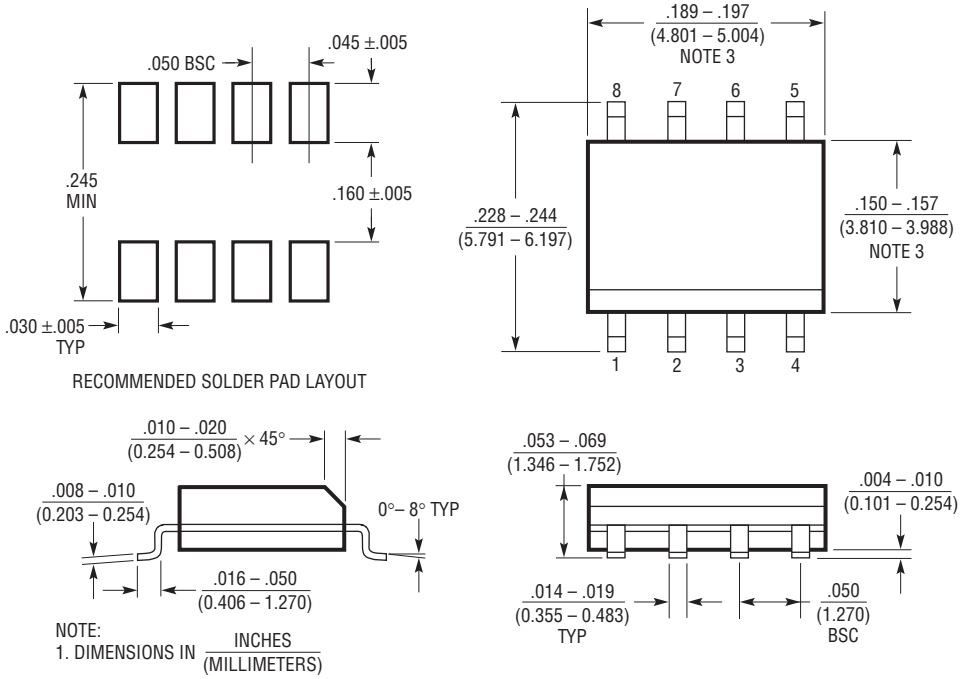
NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



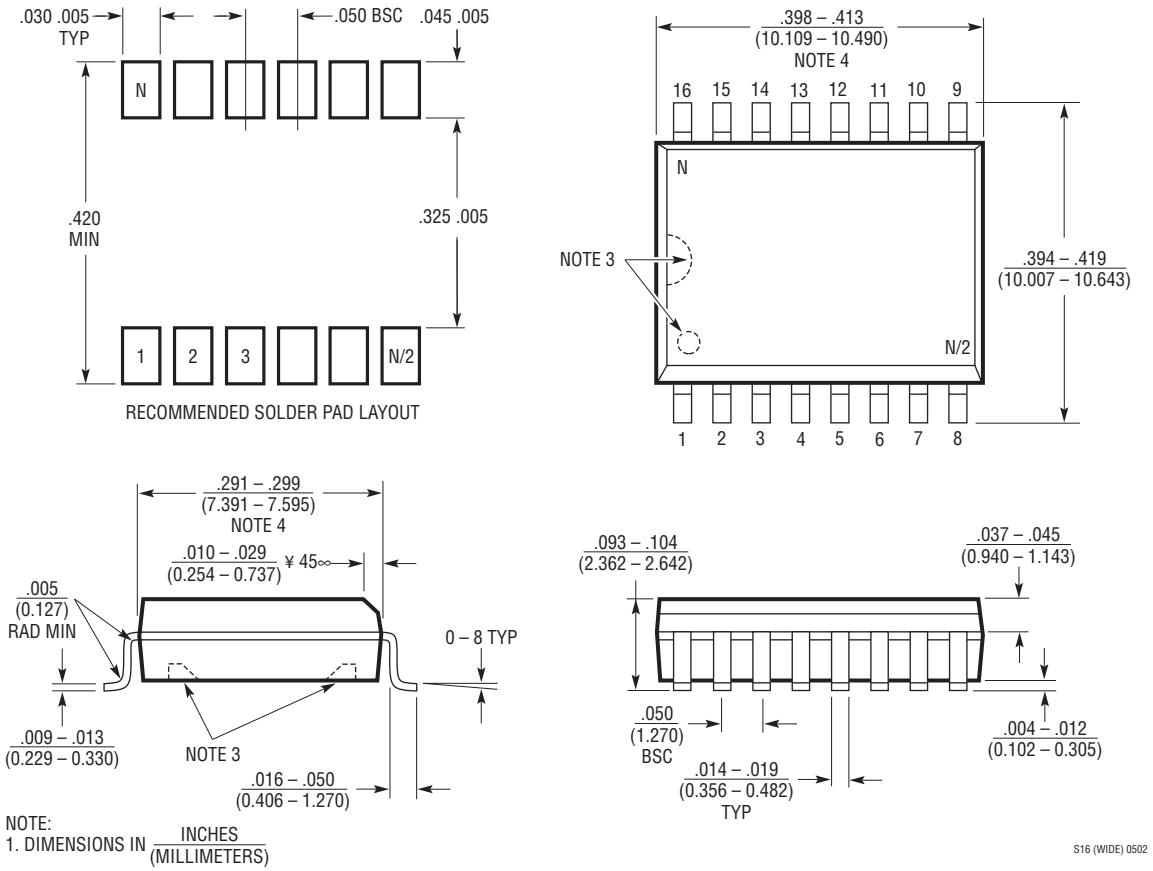
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

SO8 REV G 0212

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

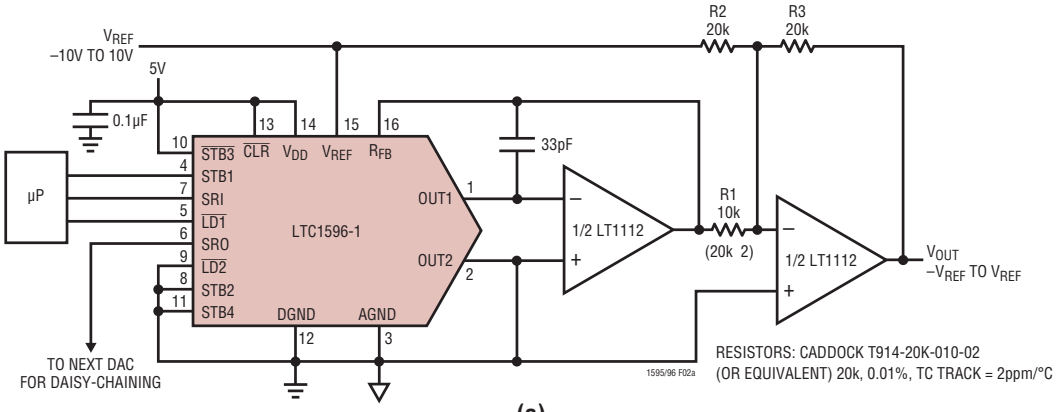
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/12	Removed 16-Lead PDIP	1, 2
C	8/15	Fixed errors in Table 3	16

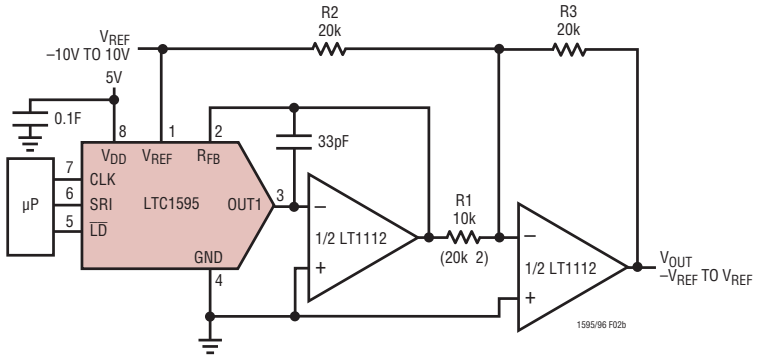
LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



(a)



(b)

Table 3. Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB			LSB	
1111	1111	1111	1111	V_{REF} (32,767/32,768)
1000	0000	0000	0001	V_{REF} (1/32,768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	$-V_{REF}$ (1/32,768)
0000	0000	0000	0000	$-V_{REF}$

Figure 2. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
DACs		
LTC1590	Dual Serial I/O Multiplying I_{OUT} 12-Bit DAC	16-Pin SO and PDIP, SPI Interface
LTC1597	Parallel 16-Bit Current Output DAC	Low Glitch, ±1LSB Maximum INL, DNL
LTC1650	Serial 16-Bit Voltage Output DAC	Low Noise and Glitch Rail-to-Rail V_{OUT}
LTC1658	Serial 14-Bit Voltage Output DAC	Low Power, 8-Lead MSOP Rail-to-Rail V_{OUT}
LTC7543/LTC8143/LTC8043	Serial I/O Multiplying I_{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
ADCs		
LTC1418	14-Bit, 200ksps 5V Sampling ADC	16mW Dissipation, Serial and Parallel Outputs
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = 100dB
LTC1605	Single 5V, 16-Bit 100ksps ADC	Low Power, ±10V Inputs
LTC2400	24-Bit, ΔΣ ADC in SO-8	1ppm (4ppm) Offset (Full-Scale), Internal 50Hz/60Hz Notches
Op Amps		
LT1001	Precision Operational Amplifier	Low Offset, Low Drift
LT1112	Dual Low Power, Precision Picoamp Input Op Amp	Low Offset, Low Drift
LT1468	90MHz, 22V/µs, 16-Bit Accurate Op Amp	Precise, 1µs Settling to 0.0015%
References		
LT1236	Precision Reference	Ultralow Drift, 5ppm/°C, High Accuracy 0.05%
LT1634	Micropower Reference	Ultralow Drift, 10ppm/°C, High Accuracy 0.05%

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