

# 2-Mbit (64K × 32) Pipelined Sync SRAM

#### **Features**

- Registered inputs and outputs for pipelined operation
- 64K × 32 common I/O architecture
- 3.3 V core power supply
- 2.5 V/3.3 V I/O operation
- Fast clock-to-output times

  □ 4.0 ns (for 133 MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel<sup>®</sup> Pentium<sup>®</sup> interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Offered in JEDEC-standard lead-free 100-pin TQFP package
- "ZZ" Sleep Mode Option

# **Functional Description**

The CY7C1329H SRAM integrates  $64K \times 32$  SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter

for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include <u>all</u> addresses, all data inputs, address-pipelining <u>Chip</u> Enable ( $\overline{\text{CE}}_1$ ), depth-expansion <u>Chip</u> Enables ( $\overline{\text{CE}}_2$  and  $\overline{\text{CE}}_3$ ), <u>Burst</u> Control inputs ( $\overline{\text{ADSC}}$ , ADSP, <u>and</u>  $\overline{\text{ADV}}$ ), Write Enables ( $\overline{\text{BW}}_{[A:D]}$  and  $\overline{\text{BWE}}$ ), and Global <u>Write</u> ( $\overline{\text{GW}}$ ). Asynchronous inputs include the Output Enable ( $\overline{\text{OE}}$ ) and the ZZ pin.

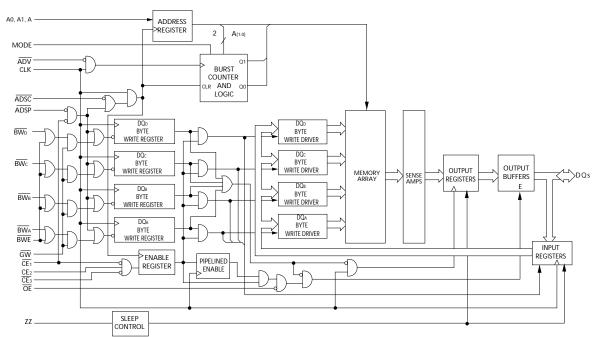
Addresses and chip enables are registered<u>at rising</u> edge of clock when either Address Strobe Processor (ADSP) or Address Strobe Controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. This part supports Byte Write operations (see Pin Definitions on page 4 and Truth Table on page 7 for further details). Write cycles can be one to <u>four</u> bytes wide as controlled by the Byte Write control inputs. GW when active LOW causes all bytes to be written.

The CY7C1329H operates from a +3.3 V core power supply while all outputs operate with either a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click here.

# **Logic Block Diagram**





# **Contents**

Selection Guide	3
Pin Configurations	3
Pin Definitions	4
Functional Overview	5
Single Read Accesses	5
Single Write Accesses Initiated by ADSP	5
Single Write Accesses Initiated by ADSC	5
Burst Sequences	5
Sleep Mode	5
Interleaved Burst Address Table	6
Linear Burst Address Table	6
ZZ Mode Electrical Characteristics	6
Truth Table	7
Truth Table for Read/Write	8
Maximum Ratings	9
Operating Range	9
Electrical Characteristics	9
Capacitance	10

Thermal Resistance	10
AC Test Loads and Waveforms	10
Switching Characteristics	11
Switching Waveforms	12
Ordering Information	16
Ordering Code Definitions	
Package Diagram	17
Acronyms	18
Document Conventions	18
Units of Measure	18
Document History Page	19
Sales, Solutions, and Legal Information	21
Worldwide Sales and Design Support	
Products	
PSoC® Solutions	21
Cypress Developer Community	21
Technical Support	

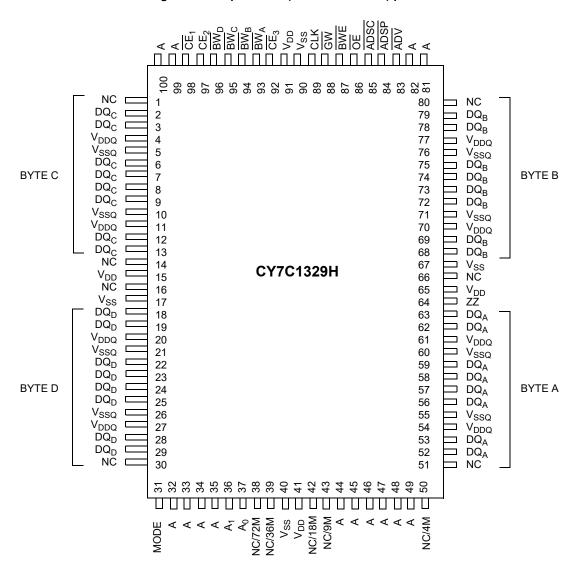


## **Selection Guide**

Description	133 MHz	Unit
Maximum Access Time	4.0	ns
Maximum Operating Current	225	mA
Maximum CMOS Standby Current	40	mA

## **Pin Configurations**

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout





# **Pin Definitions**

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input- Synchronous	Address Inputs used to select one of the 64K address locations. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$ , $\overline{CE}_2$ , and $\overline{CE}_3$ are sampled active. A1:A0 feed the 2-bit counter.
$\overline{BW}_A$ , $\overline{BW}_B$ , $\overline{BW}_C$ , $\overline{BW}_D$	Input- Synchronous	Byte Write Select Inputs, active LOW. Qualified with BWE to conduct Byte Writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input- Synchronous	<b>Global Write Enable Input, active LOW</b> . When asserted LOW on the rising edge of CLK, a global Write is conducted (All bytes are written, regardless of the values on BW <sub>[A:D]</sub> and BWE).
BWE	Input- Synchronous	<b>Byte Write Enable Input, active LOW</b> . Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a Byte Write.
CLK	Input- Clock	<b>Clock Input</b> . <u>Used</u> to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
CE <sub>1</sub>	Input- Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $CE_3$ to select/deselect the device. ADSP is ignored if $CE_1$ is HIGH. $CE_1$ is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input- Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{CE}}_2$ is sampled only when a new external address is loaded.
CE <sub>3</sub>	Input- Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}_1}$ and $\text{CE}_2$ to select/deselect the device. $\overline{\text{CE}_3}$ is sampled only when a new external address is loaded.
ŌĒ	Input- Asynchronou s	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a Read cycle when emerging from a deselected state.
ADV	Input- Synchronous	Advance Input signal, sampled on the rising edge of CLK, active LOW. When asserted, it automatically increments the address in a burst cycle.
ADSP	Input- Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK, active LOW. When as serted LOW, A is captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $CE_1$ is deasserted HIGH.
ADSC	Input- Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK, active LOW. When as serted LOW, A is captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input- Asynchronou s	<b>ZZ</b> "sleep" Input, active HIGH. This input, when HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ <sub>A</sub> , DQ <sub>B</sub> DQ <sub>C</sub> , DQ <sub>D</sub>	I/O- Synchronous	<b>Bidirectional Data I/O lines</b> . As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by "A" during the previous clock rise of the Read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ are placed in a tri-state condition.
$V_{DD}$	Power Supply	Power supply inputs to the core of the device.
$V_{SS}$	Ground	Ground for the core of the device.
$V_{\mathrm{DDQ}}$	I/O Power Supply	Power supply for the I/O circuitry.
$V_{SSQ}$	I/O Ground	Ground for the I/O circuitry.
MODE	Input- Static	<b>Selects Burst Order</b> . When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode Pin has an internal pull-up.
NC	-	<b>No Connects</b> . Not internally connected to the die. 4M, 9M, 18M, 72M, 144M, 288M, 576M and 1G are address expansion pins and are not internally connected to the die.



### **Functional Overview**

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1329H supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte Write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select (BW $_{[A:D]}$ ) inputs. A Global Write Enable (GW) overrides all Byte Write inputs and writes data to all four bytes. All Writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Selects  $(\overline{CE}_1, CE_2, \overline{CE}_3)$  and an asynchronous Output Enable  $(\overline{OE})$  provide for easy bank selection and output tri-state control. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub> are all asserted active, and (3) the Write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if CE1 is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within t<sub>CO</sub> if  $\overline{\text{OE}}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will tri-state immediately.

### Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2)  $CE_1$ ,  $CE_2$ ,  $CE_3$  are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the RAM array. The Write signals (GW, BWE, and  $BW_{[A:D]}$ ) and ADV inputs are ignored during this first cycle.

ADSP-trigge<u>red</u> Write accesses require two clock cycles to complete. If  $\overline{GW}$  is asserted LOW on the second clock rise, the data presented to the DQ inputs is written <u>into</u> the corresponding address location in the memory array. If  $\overline{GW}$  is HIGH, then the

Write operation is controlled by  $\overline{BWE}$  and  $\overline{BW}_{[A:D]}$  signals. The CY7C1329H provides Byte Write capability that is described in the Write Cycle Descriptions table. Asserting the Byte Write Enable input ( $\overline{BWE}$ ) with the selected Byte Write ( $\overline{BW}_{[A:D]}$ ) input, will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1329H is a common I/O device, the Output Enable  $(\overline{OE})$  must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub> are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and BW<sub>[A:D]</sub>) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered Write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to DQ is written into the corresponding address location in the memory core. If a Byte Write is conducted, only the selected bytes are written. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1329H is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQ inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

#### **Burst Sequences**

The CY7C1329H provides a two-bit wraparound counter, fed by A1:A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

#### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub>, ADSP, and ADSC must remain inactive for the duration of t<sub>ZZREC</sub> after the ZZ input returns LOW.



## **Interleaved Burst Address Table**

(MODE = Floating or  $V_{DD}$ )

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

## **Linear Burst Address Table**

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

# **ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
I <sub>DDZZ</sub>	Sleep mode standby current	$ZZ \ge V_{DD} - 0.2 \text{ V}$	_	40	mA
t <sub>ZZS</sub>	Device operation to ZZ	$ZZ \ge V_{DD} - 0.2 \text{ V}$	_	2t <sub>CYC</sub>	ns
t <sub>ZZREC</sub>	ZZ recovery time	ZZ ≤ 0.2 V	2t <sub>CYC</sub>	_	ns
$t_{ZZI}$	ZZ Active to sleep current	This parameter is sampled	_	2t <sub>CYC</sub>	ns
t <sub>RZZI</sub>	ZZ Inactive to exit sleep current	This parameter is sampled	0	_	ns



## **Truth Table**

The Truth Table for part CY7C1329H is as follows. [1, 2, 3, 4, 5, 6]

Next Cycle	Add. Used	CE <sub>1</sub>	CE <sub>2</sub>	CE <sub>3</sub>	ZZ	ADSP	ADSC	ADV	WRITE	OE	CLK	DQ
Deselect cycle, power-down	None	Н	Х	Х	L	Х	L	Х	Х	Х	L–H	Tristate
Deselect cycle, power-down	None	L	L	Х	L	L	Х	Х	Х	Х	L–H	Tristate
Deselect cycle, power-down	None	L	Х	Н	L	L	Х	Х	Х	Х	L–H	Tristate
Deselect cycle, power-down	None	L	L	Х	L	Н	L	Х	Х	Х	L–H	Tristate
Deselect cycle, power-down	None	L	Х	Н	L	Н	L	Х	Х	Х	L–H	Tristate
Snooze mode, power-down	None	Х	Х	Х	Н	Х	Х	Х	Х	Х	Х	Tristate
Read Cycle, Begin Burst	External	L	Н	L	L	L	Х	Х	Х	L	L–H	Q
Read Cycle, Begin Burst	External	L	Н	L	L	L	Х	Х	Х	Н	L–H	Tristate
Write Cycle, Begin Burst	External	L	Н	L	L	Н	L	Х	L	Х	L–H	D
Read Cycle, Begin Burst	External	L	Н	L	L	Н	L	Х	Н	L	L–H	Q
Read Cycle, Begin Burst	External	L	Н	L	L	Н	L	Х	Н	Н	L–H	Tristate
Read Cycle, Continue Burst	Next	Х	Х	Х	L	Н	Н	L	Н	Н	L–H	Tristate
Read Cycle, Continue Burst	Next	Х	Х	Х	L	Н	Н	L	Н	L	L–H	Q
Read Cycle, Continue Burst	Next	Н	Х	Х	L	Х	Н	L	Н	L	L–H	Q
Read Cycle, Continue Burst	Next	Н	Х	Х	L	Х	Н	L	Н	Н	L–H	Tristate
Write cycle, continue burst	Next	Х	Х	Х	L	Н	Н	L	L	Х	L–H	D
Write cycle, continue burst	Next	Н	Х	Х	L	Х	Н	L	L	Х	L–H	D
Read cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	Н	L	L–H	Q
Read cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	Н	Н	L–H	Tristate
Read cycle, suspend burst	Current	Н	Х	Х	L	Х	Н	Н	Н	L	L–H	Q
Read cycle, suspend burst	Current	Н	Х	Х	L	Х	Н	Н	Н	Н	L–H	Tristate
Write cycle, suspend burst	Current	Х	Х	Х	L	Н	Н	Н	L	Χ	L–H	D
Write cycle, suspend burst	Current	Н	Х	Χ	L	Х	Н	Н	L	Χ	L–H	D

#### Notes

Notes
 X = "Don't Care." H = Logic HIGH, L = Logic LOW.
 WRITE = L when any one or more Byte Write Enable signals (BWA, BWB, BWC, BWD) and BWE = L or GW = L. WRITE = H when all Byte Write Enable signals (BWA, BWB, BWC, BWD), BWE, GW = H.
 The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
 CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub> are available only in the TQFP package.
 The SRAM always initiates a read\_cycle when ADSP is asserted, regardless of the state of GW, BWE, or BW<sub>[A:D]</sub>. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, OE must be driven HIGH prior to the start of the Write cycle to allow the outputs to Tri-State. OE is a don't care for the remainder of the Write cycle.
 OE is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle all data bits are Tri-State when OE is inactive or when the device is deselected, and all data bits behave as output when OE is active (LOW).



## **Truth Table for Read/Write**

The Truth Table for read or write for part CY7C1329H is as follows.  $^{[7,\ 8]}$ 

Function	GW	BWE	BW <sub>D</sub>	BW <sub>C</sub>	BW <sub>B</sub>	BW <sub>A</sub>
Read	Н	Н	Х	Х	Х	Х
Read	Н	L	Н	Н	Н	Н
Write Byte A - DQ <sub>A</sub>	Н	L	Н	Н	Н	L
Write Byte B – DQ <sub>B</sub>	Н	L	Н	Н	L	Н
Write Bytes B, A	Н	L	Н	Н	L	L
Write Byte C – DQ <sub>C</sub>	Н	L	Н	L	Н	Н
Write Bytes C, A	Н	L	Н	L	Н	L
Write Bytes C, B	Н	L	Н	L	L	Н
Write Bytes C, B, A	Н	L	Н	L	L	L
Write Byte D – DQ <sub>D</sub>	Н	L	L	Н	Н	Н
Write Bytes D, A	Н	L	L	Н	Н	L
Write Bytes D, B	Н	L	L	Н	L	Н
Write Bytes D, B, A	Н	L	L	Н	L	L
Write Bytes D, C	Н	L	L	L	Н	Н
Write Bytes D, C, A	Н	L	L	L	Н	L
Write Bytes D, C, B	Н	L	L	L	L	Н
Write All Bytes	Н	L	L	L	L	L
Write All Bytes	L	Х	Х	Х	Х	Х

Page 8 of 21 Document Number: 38-05673 Rev. \*J

<sup>7.</sup> X = "Don't Care." H = Logic HIGH, L = Logic LOW.
8. WRITE = L when any one or more Byte Write Enable signals (BWA, BWB, BWC, BWD) and BWE = L or GW = L. WRITE = H when all Byte Write Enable signals (BWA, BWB, BWC, BWD), BWE, GW = H.



# **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested. Storage Temperature ......-65 °C to +150 °C Ambient Temperature with Supply Voltage on  $V_{DD}$  Relative to GND .....-0.5 V to +4.6 V Supply Voltage on  $V_{DDQ}$  Relative to GND .... -0.5~V to  $+V_{DD}$ DC Voltage Applied to Outputs in Tri-State ......-0.5 V to V<sub>DDQ</sub> + 0.5 V

DC Input Voltage0.5	V to V <sub>DD</sub> + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001 V
Latch-up Current	> 200 mA

# **Operating Range**

Range	Ambient Temperature	V <sub>DD</sub>	$V_{\mathrm{DDQ}}$
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>

## **Electrical Characteristics**

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions		Min	Max	Unit
$V_{DD}$	Power Supply Voltage			3.135	3.6	V
$V_{DDQ}$	I/O Supply Voltage	for 3.3 V I/O		3.135	$V_{DD}$	V
		for 2.5 V I/O		2.375	2.625	V
V <sub>OH</sub>	Output HIGH Voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA		2.4	_	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA		2.0	_	V
V <sub>OL</sub>	Output LOW Voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	_	0.4	V	
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA				
V <sub>IH</sub>	Input HIGH Voltage <sup>[9]</sup>	or 3.3 V I/O		2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O		1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW Voltage [9]	for 3.3 V I/O	-0.3	0.8	V	
		for 2.5 V I/O	-0.3	0.7	V	
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	$GND \le V_I \le V_{DDQ}$		<b>–</b> 5	5	μА
	Input Current of MODE	Input = V <sub>SS</sub>		-30	_	μА
		Input = V <sub>DD</sub>		_	5	μА
V <sub>IL</sub> Ir  Ix  Ir  Ir  Iv  Iv  Iv  Iv  Iv  Iv  Iv  Iv	Input Current of ZZ	Input = V <sub>SS</sub>	-5	_	μА	
		Input = V <sub>DD</sub>		-	30	μА
I <sub>OZ</sub>	Output Leakage Current	$GND \le V_I \le V_{DDQ}$ , Output Disable	ed	<b>–</b> 5	5	μА
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply Current	$V_{DD}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/ $t_{CYC}$	7.5-ns cycle, 133 MHz	_	225	mA
I <sub>SB1</sub>	Automatic CS Power-down Current – TTL Inputs	$V_{DD}$ = Max, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ , $f = f_{MAX} = 1/t_{CYC}$	7.5-ns cycle, 133 MHz	_	90	mA
I <sub>SB2</sub>	Automatic CS Power-down Current – CMOS Inputs	$V_{DD}$ = Max, Device Deselected, $V_{IN} \le 0.3 \text{ V or } V_{IN} \ge V_{DDQ} - 0.3 \text{ V},$ f = 0		-	40	mA

<sup>9.</sup> Overshoot:  $V_{IH(AC)} < V_{DD} + 1.5 \text{ V}$  (Pulse width less than  $t_{CYC}/2$ ), undershoot:  $V_{IL(AC)} > -2 \text{ V}$  (Pulse width less than  $t_{CYC}/2$ ). 10.  $T_{Power-up}$ : Assumes a linear ramp from 0 V to  $V_{DD(min)}$  within 200 ms. During this time  $V_{IH} < V_{DD}$  and  $V_{DDQ} \le V_{DD}$ .



# **Electrical Characteristics** (continued)

Over the Operating Range

Parameter [9, 10]	Description	Test Conditions		Min	Max	Unit
I <sub>SB3</sub>	Automatic CS Power-down Current – CMOS Inputs	$V_{DD}$ = Max, Device Deselected, $V_{IN} \le 0.3  \text{V or}  V_{IN} \ge V_{DDQ} - 0.3  \text{V}$ , $f = f_{MAX} = 1/t_{CYC}$	7.5-ns cycle, 133 MHz	_	75	mA
I <sub>SB4</sub>	Automatic CS Power-down Current – TTL Inputs	, ,	7.5-ns cycle, 133 MHz	_	45	mA

# Capacitance

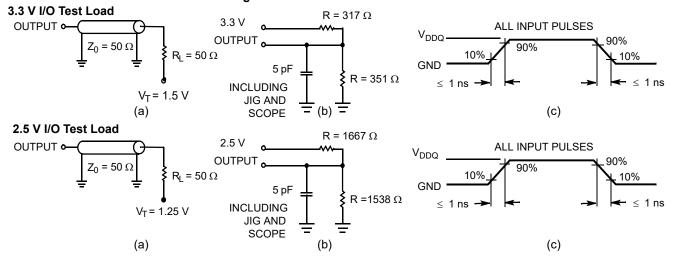
Parameter [11]	Description	Test Conditions	100-pin TQFP Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25  ^{\circ}\text{C}$ , $f = 1  \text{MHz}$ , $V_{DD} = 3.3  \text{V}$ , $V_{DDQ} = 2.5  \text{V}$	5	pF
C <sub>CLK</sub>	Clock input capacitance		5	pF
C <sub>I/O</sub>	Input/Output capacitance		5	pF

## **Thermal Resistance**

Parameter [11]	Description	Test Conditions	100-pin TQFP Package	Unit
$\Theta_{\sf JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per		°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)	EIA/JESD51.	6.85	°C/W

# **AC Test Loads and Waveforms**

#### Figure 2. AC Test Loads and Waveforms



#### Note

<sup>11.</sup> Tested initially and after any design or process change that may affect these parameters.



# **Switching Characteristics**

Over the Operating Range

Parameter [12, 13]	Description	133	133 MHz		
Parameter [12, 10]	Description	Min	Max	Unit	
t <sub>POWER</sub>	V <sub>DD</sub> (typical) to the First Access <sup>[14]</sup>	1	_	ms	
Clock			•		
t <sub>CYC</sub>	Clock Cycle Time	7.5	_	ns	
t <sub>CH</sub>	Clock HIGH	3.0	_	ns	
t <sub>CL</sub>	Clock LOW	3.0	_	ns	
Output Times			•		
t <sub>CO</sub>	Data Output Valid after CLK Rise	_	4.0	ns	
t <sub>DOH</sub>	Data Output Hold after CLK Rise	1.5	_	ns	
t <sub>CLZ</sub>	Clock to Low Z [15, 16, 17]	0	_	ns	
t <sub>CHZ</sub>	Clock to High Z [15, 16, 17]	_	4.0	ns	
t <sub>OEV</sub>	OE LOW to Output Valid	_	4.5	ns	
t <sub>OELZ</sub>	OE LOW to Output Low Z [15, 16, 17]	0	_	ns	
t <sub>OEHZ</sub>	OE HIGH to Output High Z [15, 16, 17]	_	4.0	ns	
Set-up Times		1		I.	
t <sub>AS</sub>	Address Set-up before CLK Rise	1.5	_	ns	
t <sub>ADS</sub>	ADSC, ADSP Set-up before CLK Rise	1.5	_	ns	
t <sub>ADVS</sub>	ADV Set-up before CLK Rise	1.5	_	ns	
t <sub>WES</sub>	GW, BWE, BW <sub>[A:D]</sub> Set-up before CLK Rise	1.5	_	ns	
t <sub>DS</sub>	Data Input Set-up before CLK Rise	1.5	_	ns	
t <sub>CES</sub>	Chip Enable Set-Up before CLK Rise	1.5	_	ns	
Hold Times		1		I.	
t <sub>AH</sub>	Address Hold after CLK Rise	0.5	_	ns	
t <sub>ADH</sub>	ADSP, ADSC Hold after CLK Rise	0.5	_	ns	
t <sub>ADVH</sub>	ADV Hold after CLK Rise 0.5			ns	
t <sub>WEH</sub>	GW, BWE, BW [A:D]   Hold after CLK Rise     0.5				
t <sub>DH</sub>	Data Input Hold after CLK Rise 0.5				
t <sub>CEH</sub>	Chip Enable Hold after CLK Rise	0.5	-	ns	

<sup>12.</sup> Timing reference level is 1.5 V when  $V_{DDQ}$  = 3.3 V and is 1.25 V when  $V_{DDQ}$  = 2.5 V. 13. Test conditions shown in (a) ofFigure 2 on page 10 unless otherwise noted.

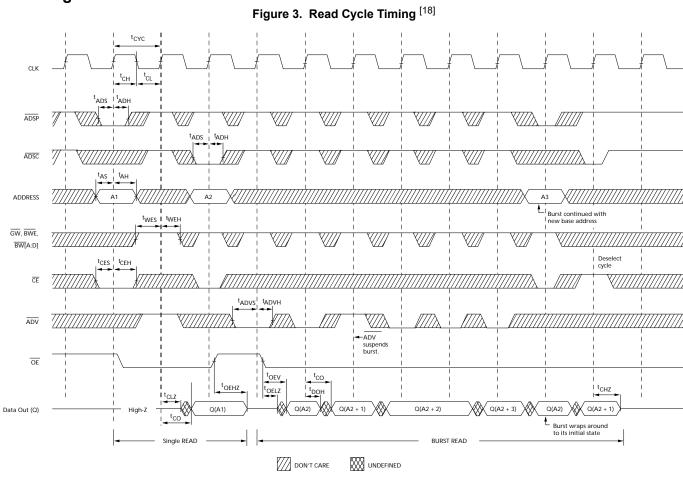
<sup>14.</sup> This part has a voltage regulator internally; tpower is the time that the power needs to be supplied above V<sub>DD(minimum)</sub> initially before a Read or Write operation can

<sup>15.</sup> t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC test conditions shown in part (b) of Figure 2 on page 10. Transition is measured ± 200 mV from steady-state voltage. 16. At any given voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.

<sup>17.</sup> This parameter is sampled and not 100% tested.



# **Switching Waveforms**



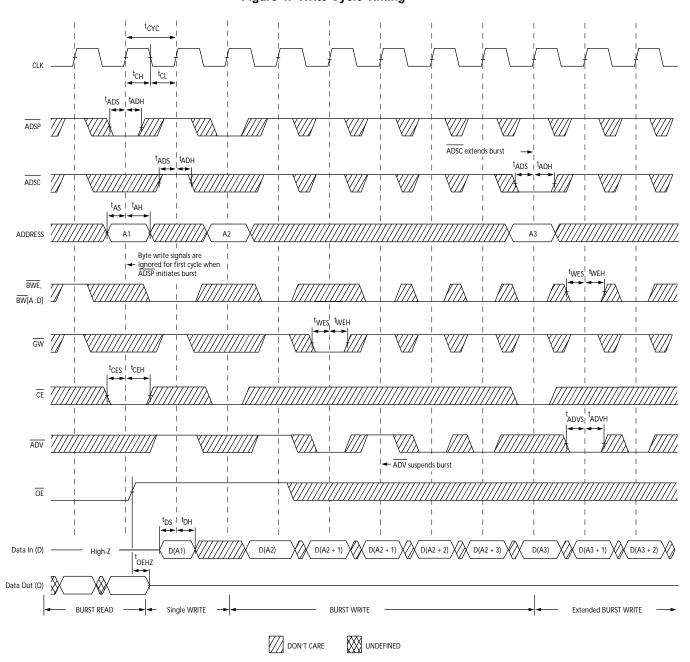
Note

<sup>18.</sup> On this diagram, when  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.



# Switching Waveforms (continued)

Figure 4. Write Cycle Timing [19, 20]



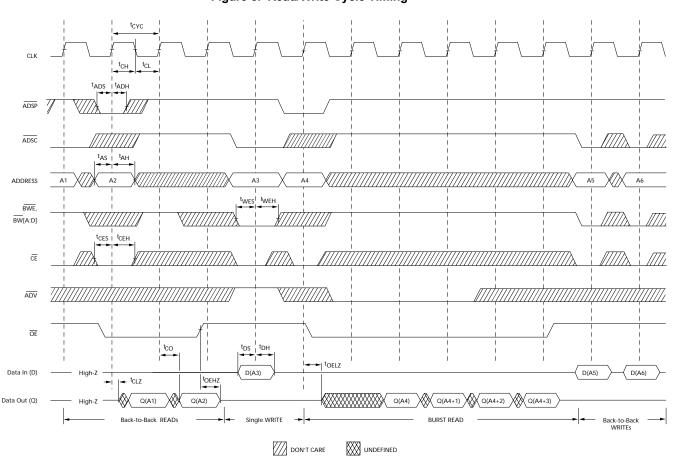
## Notes

<sup>19.</sup> On this diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE}}_1$  is LOW,  $\overline{\text{CE}}_2$  is HIGH and  $\overline{\text{CE}}_3$  is LOW. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE}}_1$  is HIGH or  $\overline{\text{CE}}_2$  is LOW or  $\overline{\text{CE}}_3$  is HIGH. 20. Full width Write can be initiated by either  $\overline{\text{GW}}$  LOW; or by  $\overline{\text{GW}}$  HIGH,  $\overline{\text{BWE}}$  LOW and  $\overline{\text{BW}}_{[A:D]}$  LOW.



# Switching Waveforms (continued)

Figure 5. Read/Write Cycle Timing  $^{[21,\ 22,\ 23]}$ 



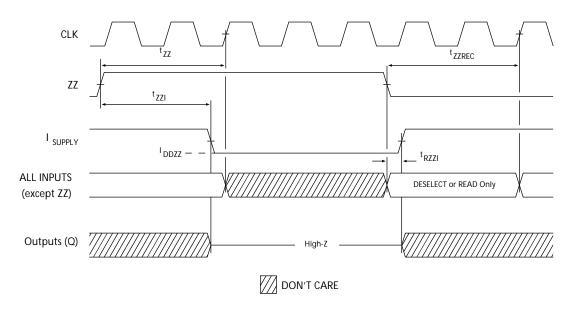
<sup>21.</sup> On this diagram, when  $\overline{\text{CE}}$  is LOW,  $\overline{\text{CE}}_1$  is LOW,  $\overline{\text{CE}}_2$  is HIGH and  $\overline{\text{CE}}_3$  is LOW. When  $\overline{\text{CE}}$  is HIGH,  $\overline{\text{CE}}_1$  is HIGH or  $\overline{\text{CE}}_2$  is LOW or  $\overline{\text{CE}}_3$  is HIGH. 22. The data bus (Q) remains in High Z following a Write cycle unless an  $\overline{\text{ADSP}}$ ,  $\overline{\text{ADSC}}$ , or  $\overline{\text{ADV}}$  cycle is performed.

<sup>23.</sup> GW is HIGH.



# Switching Waveforms (continued)

Figure 6. ZZ Mode Timing  $^{[24,\ 25]}$ 



Notes
24. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
25. DQs are in High Z when exiting ZZ sleep mode.



# **Ordering Information**

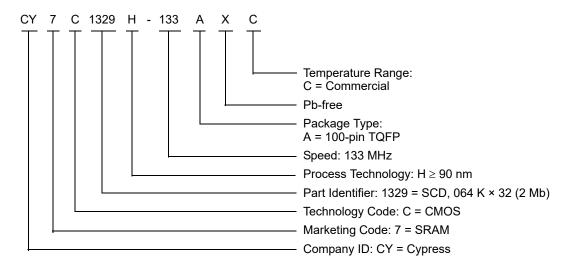
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at <a href="http://www.cypress.com/products">www.cypress.com/products</a> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1329H-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

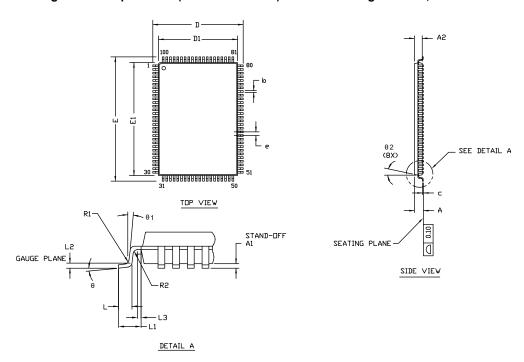
### **Ordering Code Definitions**





# **Package Diagram**

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS			
STIMBUL	MIN.	NOM.	MAX.	
Α	_	_	1.60	
A1	0.05	_	0.15	
A2	1.35	1.40	1.45	
D	15.80	16.00	16.20	
D1	13.90	14.00	14.10	
Е	21.80	22.00	22.20	
E1	19.90	20.00	20.10	
R1	0.08	_	0.20	
R2	0.08	_	0.20	
θ	0°	_	7°	
θ1	0°	_	_	
θ2	11°	12°	13°	
С	_	_	0.20	
b	0.22	0.30	0.38	
L	0.45	0.60	0.75	
L1	1.	.00 RE	F	
L2	0	.25 BS	С	
L3	0.20	_	_	
е	0.	.65 TY	P	

#### NOTE:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH.

  MOLD PROTRUSION/END FLASH SHALL

  NOT EXCEED 0.0098 in (0.25 mm) PER SIDE.

  BODY LENGTH DIMENSIONS ARE MAX PLASTIC

  BODY SIZE INCLUDING MOLD MISMATCH.
- 3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 \*G



# **Acronyms**

Acronym	Description		
CE	Chip Enable		
CMOS	Complementary Metal Oxide Semiconductor		
EIA	Electronic Industries Alliance		
I/O	Input/Output		
JEDEC	Joint Electron Devices Engineering Council		
OE	Output Enable		
SRAM	Static Random Access Memory		
TQFP	Thin Quad Flat Pack		
TTL	Transistor-Transistor Logic		

# **Document Conventions**

# **Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nm	nanometer
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



# **Document History Page**

Document Title: CY7C1329H, 2-Mbit (64K × 32) Pipelined Sync SRAM Document Number: 38-05673				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	347357	PCI	04/15/2005	New data sheet.
*A	424820	RXU	02/06/2006	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court". Updated Pin Definitions (Changed Three-State to Tri-State). Updated Functional Overview (Changed Three-State to Tri-State). Updated Truth Table (Updated Note 6 (Changed Three-State to Tri-State)). Updated Maximum Ratings (Changed Three-State to Tri-State). Updated Electrical Characteristics (Updated Note 10 (Changed test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ ); changed "Input Load Current except ZZ and MODE" to "Input Leakage Current except ZZ and MODE"). Updated Ordering Information (Updated part numbers; removed Package Name column; added Package Diagram column in the table). Updated Package Diagram: spec 51-85050 — Changed revision from *A to *B. Updated to new template.
*B	433014	NXR	03/27/2006	Updated Features (Included 3.3 V I/O option). Updated Functional Description (Included 3.3 V I/O option). Updated Electrical Characteristics (Included 3.3 V I/O option). Updated AC Test Loads and Waveforms (Updated Figure 2 (Included 3.3 V I/O option)). Updated Switching Characteristics (Updated Note 12 (Included 3.3 V I/O option)). Updated Ordering Information (Updated part numbers).
*C	2896585	NJY	03/20/2010	Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 51-85050 – Changed revision from *B to *C.
*D	3052882	NJY	10/08/2010	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions.
*E	3293640	NJY	06/27/2011	Updated Package Diagram: spec 51-85050 – Changed revision from *C to *D. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*F	3613761	NJY	05/10/2012	Updated Features (Removed 166 MHz frequency related information). Updated Functional Description (Removed the Note "For best-practices recommendations, please refer to the Cypress application note System Design Guidelines on www.cypress.com." and its reference). Updated Selection Guide (Removed 166 MHz frequency related information Updated Pin Definitions (Removed BGA related information). Updated Operating Range (Removed Industrial Temperature Range). Updated Electrical Characteristics (Removed 166 MHz frequency related information). Updated Switching Characteristics (Removed 166 MHz frequency related information). Completing Sunset Review.
*G	4081869	PRIT	07/30/2013	Updated Truth Table: Updated entire table. Updated to new template.



# **Document History Page**

Document Document	Document Title: CY7C1329H, 2-Mbit (64K × 32) Pipelined Sync SRAM Document Number: 38-05673					
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change		
*H	4575272	PRIT	11/20/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Package Diagram: spec 51-85050 – Changed revision from *D to *E.		
*	4811048	PRIT	06/25/2015	Updated to new template. Completing Sunset Review.		
*J	6045185	CNX	01/25/2018	Updated Package Diagram: spec 51-85050 – Changed revision from *E to *G. Updated to new template.		



# Sales, Solutions, and Legal Information

### **Worldwide Sales and Design Support**

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

#### **Products**

Arm® Cortex® Microcontrollers cypress.com/arm Automotive cypress.com/automotive Clocks & Buffers cypress.com/clocks Interface cypress.com/interface Internet of Things cypress.com/iot Memory cypress.com/memory Microcontrollers cypress.com/mcu **PSoC** cypress.com/psoc

Power Management ICs cypress.com/pmic
Touch Sensing cypress.com/touch
USB Controllers cypress.com/usb
Wireless Connectivity cypress.com/wireless

## PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

### **Cypress Developer Community**

Community | Projects | Video | Blogs | Training | Components

### **Technical Support**

cypress.com/support

© Cypress Semiconductor Corporation, 2005-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems of the medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the aliure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.