



**2.5V/3.3V HIGH-PERFORMANCE, DUAL 1:10  
OR LVPECL CLOCK DRIVER w/ INTERNAL  
TERMINATION AND REDUNDANT SWITCHOVER**

**Precision Edge®  
SY89829U**

## FEATURES

- Dual 1:10 fanout buffer/translator
- Accepts LVPECL or LVDS inputs
- Multiplexed inputs ideal for redundant clock switchover
- Guaranteed AC parameters:
  - > 2GHz  $f_{MAX}$  (toggle)
  - < 50ps ch-ch skew
- LVDS input includes 100Ω internal termination
- Low supply voltage: 2.5V, 3.3V
- -40°C to +85°C temperature range
- Output enable (OE) pin
- Available in 64 EPAD-TQFP

## APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications
- Redundant LVPECL or LVDS bus clock switchover



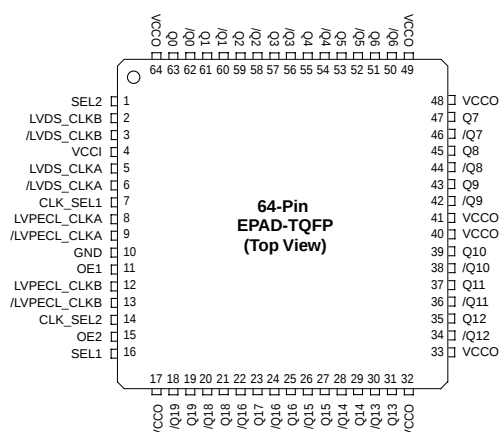
Precision Edge®

## DESCRIPTION

The SY89829U is a High Performance dual 1:10 or single 1:20 LVPECL Clock Driver. The part is designed for use in low voltage (2.5V/3.3V) applications which require a large number of outputs to drive precisely aligned, ultra low skew signals to their destination. The input is multiplexed from either LVDS or LVPECL by the CLK\_SEL pin. The LVDS inputs include a 100Ω internal termination across the input pair, thus eliminating any need for external termination. The 2:1 input mux makes this device an ideal choice for redundant clock applications that need to switch between two reference clocks. The output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This eliminates any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89829U features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89829U is available in a single space saving package which provides a lower overall cost solution. In addition, a single chip solution improves timing budgets by eliminating the multiple device solution with their corresponding large part-to-part skew.

## PACKAGE/ORDERING INFORMATION



64-Pin TQFP (H64-1)

Ordering Information<sup>(1)</sup>

| Part Number                    | Package Type | Operating Range | Package Marking                            | Lead Finish      |
|--------------------------------|--------------|-----------------|--------------------------------------------|------------------|
| SY89829UHI                     | H64-1        | Industrial      | SY89829UHI                                 | Sn-Pb            |
| SY89829UHITR <sup>(2)</sup>    | H64-1        | Industrial      | SY89829UHI                                 | Sn-Pb            |
| SY89829UHY <sup>(3)</sup>      | H64-1        | Industrial      | SY89829UHY with Pb-Free bar-line indicator | Pb-Free Matte-Sn |
| SY89829UHYTR <sup>(2, 3)</sup> | H64-1        | Industrial      | SY89829UHY with Pb-Free bar-line indicator | Pb-Free Matte-Sn |

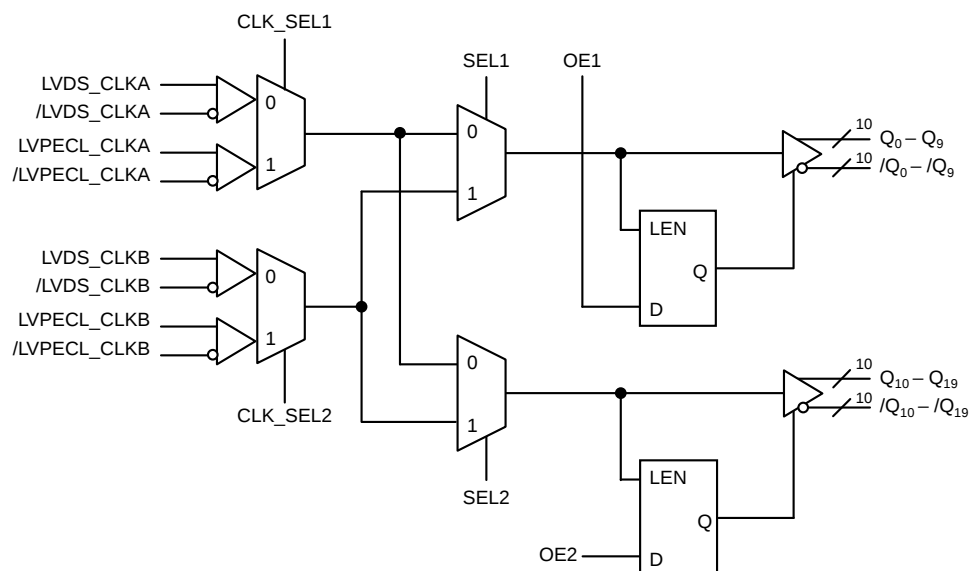
## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

## PIN NAMES

| Pin                                                          | Function                                                                                                                                                                                                                 |
|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LVDS_CLKA,<br>/LVDS_CLKA,<br>LVDS_CLKB,<br>/LVDS_CLKB        | Differential LVDS Inputs with Internal 100Ω Termination.                                                                                                                                                                 |
| LVPECL_CLKA,<br>/LVPECL_CLKA<br>LVPECL_CLKB,<br>/LVPECL_CLKB | Differential LVPECL Inputs. For DC-coupled input signals, terminate the input signal with 50Ω to $V_{CC} - 2V$ . For AC-coupled to $V_{CC} - 2V$ . For AC-coupled terminate the input signal with 50Ω to $V_{CC} - 3V$ . |
| CLK_SEL1,<br>CLK_SEL2                                        | Input CLK Select (LVTTL).                                                                                                                                                                                                |
| SEL1, SEL2                                                   | Input Select (LVTTL).                                                                                                                                                                                                    |
| OE1, OE2                                                     | Output Enable (LVTTL).                                                                                                                                                                                                   |
| $Q_0 - Q_{19}$ , $/Q_0 - /Q_{19}$                            | Differential LVPECL Outputs. Normally terminated with 50Ω to $V_{CC} - 2V$ . Unused output pairs can be left floating.                                                                                                   |
| GND                                                          | Ground.                                                                                                                                                                                                                  |
| $V_{CCI}$                                                    | Power Supply for Output Drivers.                                                                                                                                                                                         |

## LOGIC SYMBOL



## TRUTH TABLE

| OE | CLK_SEL1 | CLK_SEL2 | SEL1 | SEL2 | Q <sub>0</sub> - Q <sub>9</sub> | /Q <sub>0</sub> - /Q <sub>9</sub> | Q <sub>10</sub> - Q <sub>19</sub> | /Q <sub>10</sub> - /Q <sub>19</sub> |
|----|----------|----------|------|------|---------------------------------|-----------------------------------|-----------------------------------|-------------------------------------|
| 1  | 0        | 0        | 0    | 0    | LVDS_CLKA                       | /LVDS_CLKA                        | LVDS_CLKA                         | /LVDS_CLKA                          |
| 1  | 0        | 0        | 0    | 1    | LVDS_CLKA                       | /LVDS_CLKA                        | LVDS_CLKB                         | /LVDS_CLKB                          |
| 1  | 0        | 0        | 1    | 0    | LVDS_CLKB                       | /LVDS_CLKB                        | LVDS_CLKA                         | /LVDS_CLKA                          |
| 1  | 0        | 0        | 1    | 1    | LVDS_CLKB                       | /LVDS_CLKB                        | LVDS_CLKB                         | /LVDS_CLKB                          |
| 1  | 0        | 1        | 0    | 0    | LVDS_CLKA                       | /LVDS_CLKA                        | LVDS_CLKA                         | /LVDS_CLKA                          |
| 1  | 0        | 1        | 0    | 1    | LVDS_CLKA                       | /LVDS_CLKA                        | LVPECL_CLKB                       | /LVPECL_CLKB                        |
| 1  | 0        | 1        | 1    | 0    | LVPECL_CLKB                     | /LVPECL_CLKB                      | LVDS_CLKA                         | /LVDS_CLKA                          |
| 1  | 0        | 1        | 1    | 1    | LVPECL_CLKB                     | /LVPECL_CLKB                      | LVPECL_CLKB                       | /LVPECL_CLKB                        |
| 1  | 1        | 0        | 0    | 0    | LVPECL_CLKA                     | /LVPECL_CLKA                      | LVPECL_CLKA                       | /LVPECL_CLKA                        |
| 1  | 1        | 0        | 0    | 1    | LVPECL_CLKA                     | /LVPECL_CLKA                      | LVDS_CLKB                         | /LVDS_CLKB                          |
| 1  | 1        | 0        | 1    | 0    | LVDS_CLKB                       | /LVDS_CLKB                        | LVPECL_CLKA                       | /LVPECL_CLKA                        |
| 1  | 1        | 0        | 1    | 1    | LVDS_CLKB                       | /LVDS_CLKB                        | LVDS_CLKB                         | /LVDS_CLKB                          |
| 1  | 1        | 1        | 0    | 0    | LVPECL_CLKA                     | /LVPECL_CLKA                      | LVPECL_CLKA                       | /LVPECL_CLKA                        |
| 1  | 1        | 1        | 0    | 1    | LVPECL_CLKA                     | /LVPECL_CLKA                      | LVPECL_CLKB                       | /LVPECL_CLKB                        |
| 1  | 1        | 1        | 1    | 0    | LVPECL_CLKB                     | /LVPECL_CLKB                      | LVPECL_CLKA                       | /LVPECL_CLKA                        |
| 1  | 1        | 1        | 1    | 1    | LVPECL_CLKB                     | /LVPECL_CLKB                      | LVPECL_CLKB                       | /LVPECL_CLKB                        |
| 0  | X        | X        | X    | X    | LOW                             | HIGH                              | LOW                               | HIGH                                |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol              | Rating                                           | Value             | Unit |
|---------------------|--------------------------------------------------|-------------------|------|
| $V_{CCI} / V_{CCO}$ | $V_{CC}$ Pin Potential to Ground Pin             | –0.5 to +4.0      | V    |
| $V_{IN}$            | Input Voltage                                    | –0.5 to $V_{CCI}$ | V    |
| $I_{OUT}$           | DC Output Current (Output HIGH)                  | –50               | mA   |
| $T_{LEAD}$          | Lead Temperature (soldering, 20sec.)             | 260               | °C   |
| $T_{store}$         | Storage Temperature                              | –65 to +150       | °C   |
| $\theta_{JA}$       | Package Thermal Resistance (Junction-to-Ambient) |                   |      |
|                     | <u>With</u> exposed pad soldered to GND          |                   |      |
|                     | – Still-Air (multi-layer PCB)                    | 23                | °C/W |
|                     | – 200lfpm (multi-layer PCB)                      | 18                | °C/W |
|                     | – 500lfpm (multi-layer PCB)                      | 15                | °C/W |
|                     | Exposed pad <u>not</u> soldered to GND           |                   |      |
|                     | – Still-Air (multi-layer PCB)                    | 44                | °C/W |
|                     | – 200lfpm (multi-layer PCB)                      | 36                | °C/W |
|                     | – 500lfpm (multi-layer PCB)                      | 30                | °C/W |
| $\theta_{JC}$       | Package Thermal Resistance (Junction-to-Case)    | 4.3               | °C/W |

**NOTE:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS****Power Supply**

| Symbol                                 | Parameter                                           | T <sub>A</sub> = -40°C |      |      | T <sub>A</sub> = +25°C |      |      | T <sub>A</sub> = +85°C |      |      | Unit |
|----------------------------------------|-----------------------------------------------------|------------------------|------|------|------------------------|------|------|------------------------|------|------|------|
|                                        |                                                     | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. |      |
| V <sub>CCI</sub> ,<br>V <sub>CCO</sub> | Power Supply <sup>(1)</sup>                         | 2.37                   | —    | 3.6  | 2.37                   | —    | 3.8  | 2.37                   | —    | 3.6  | V    |
| I <sub>CC</sub>                        | I <sub>CC</sub> Total Supply Current <sup>(2)</sup> | —                      | 100  | 150  | —                      | 100  | 150  | —                      | 100  | 150  | mA   |

**NOTES:**

- V<sub>CCI</sub> and V<sub>CCO</sub> must be connected together on the PCB such that they remain at the same potential. V<sub>CCI</sub> and V<sub>CCO</sub> are not internally connected on the die.
- No load. Outputs floating.

**LVDS Input (V<sub>CC</sub> = 2.37V to 3.6V, GND = 0V)**

| Symbol          | Parameter                                                  | T <sub>A</sub> = -40°C |      |      | T <sub>A</sub> = +25°C |      |      | T <sub>A</sub> = +85°C |      |      | Unit |
|-----------------|------------------------------------------------------------|------------------------|------|------|------------------------|------|------|------------------------|------|------|------|
|                 |                                                            | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. |      |
| V <sub>IN</sub> | Input Voltage Range                                        | 0                      | —    | 2.4  | 0                      | —    | 2.4  | 0                      | —    | 2.4  | V    |
| V <sub>ID</sub> | Differential Input Swing                                   | 100                    | —    | —    | 100                    | —    | —    | 100                    | —    | —    | mV   |
| I <sub>IL</sub> | Input Low Current <sup>(1)</sup>                           | -1.0                   | —    | —    | -1.0                   | —    | —    | -1.0                   | —    | —    | mA   |
| R <sub>IN</sub> | LVDS Differential Input Resistance (LVDS_CLK to /LVDS_CLK) | 80                     | 100  | 120  | 80                     | 100  | 120  | 80                     | 100  | 120  | Ω    |

**NOTE:**

- For I<sub>IL</sub>, both LVDS inputs are grounded.

**LVPECL Input / Output (V<sub>CC</sub> = 2.37V to 3.6V, GND = 0V)**

| Symbol           | Parameter                                        | T <sub>A</sub> = -40°C   |                          | T <sub>A</sub> = +25°C   |                          | T <sub>A</sub> = +85°C   |                          | Unit |
|------------------|--------------------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|
|                  |                                                  | Min.                     | Max.                     | Min.                     | Max.                     | Min.                     | Max.                     |      |
| V <sub>IH</sub>  | Input HIGH Voltage                               | V <sub>CC</sub> - 1.165  | V <sub>CC</sub> - 0.88   | V <sub>CC</sub> - 1.165  | V <sub>CC</sub> - 0.88   | V <sub>CC</sub> - 1.165  | V <sub>CC</sub> - 0.88   | V    |
| V <sub>IL</sub>  | Input LOW Voltage                                | V <sub>CC</sub> - 1.945  | V <sub>CC</sub> - 1.625  | V <sub>CC</sub> - 1.945  | V <sub>CC</sub> - 1.625  | V <sub>CC</sub> - 1.945  | V <sub>CC</sub> - 1.625  | V    |
| V <sub>PP</sub>  | Minimum Input Swing <sup>(1)</sup><br>LVPECL_CLK | 600                      | —                        | 600                      | —                        | 600                      | —                        | mV   |
| V <sub>CMR</sub> | Common Mode Range <sup>(2)</sup><br>LVPECL_CLK   | -1.5                     | -0.4                     | -1.5                     | -0.4                     | -1.5                     | -0.4                     | V    |
| V <sub>OH</sub>  | Output HIGH Voltage                              | V <sub>CCO</sub> - 1.085 | V <sub>CCO</sub> - 0.880 | V <sub>CCO</sub> - 1.025 | V <sub>CCO</sub> - 0.880 | V <sub>CCO</sub> - 1.025 | V <sub>CCO</sub> - 0.880 | V    |
| V <sub>OL</sub>  | Output LOW Voltage                               | V <sub>CCO</sub> - 1.830 | V <sub>CCO</sub> - 1.555 | V <sub>CCO</sub> - 1.810 | V <sub>CCO</sub> - 1.620 | V <sub>CCO</sub> - 1.810 | V <sub>CCO</sub> - 1.620 | V    |
| I <sub>IH</sub>  | Input HIGH Current                               | —                        | 150                      | —                        | 150                      | —                        | 150                      | μA   |
| I <sub>IL</sub>  | Input LOW Current                                | 0.5                      | —                        | 0.5                      | —                        | 0.5                      | —                        | μA   |

**NOTES:**

- The V<sub>PP</sub> (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
- V<sub>CMR</sub> is defined as the range within which the V<sub>IH</sub> level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V<sub>CCI</sub>. The V<sub>IL</sub> level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V<sub>PP</sub> (min.). The lower end of the CMR range varies 1:1 with V<sub>CCI</sub>. The V<sub>CMR</sub> (min) will be fixed at 3.3V - |V<sub>CMR</sub> (min)|.

**LVCMOS/LVTTL Control Input (OE1, OE2, CLK\_SEL1, CLK\_SEL2)**

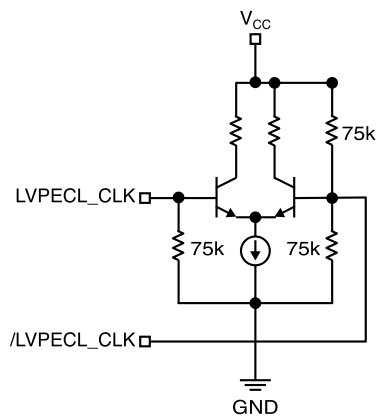
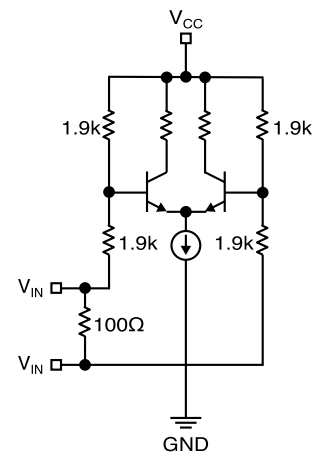
| Symbol          | Parameter          | T <sub>A</sub> = -40°C |      |      | T <sub>A</sub> = +25°C |      |      | T <sub>A</sub> = +85°C |      |      | Unit |
|-----------------|--------------------|------------------------|------|------|------------------------|------|------|------------------------|------|------|------|
|                 |                    | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. | Min.                   | Typ. | Max. |      |
| V <sub>IH</sub> | Input HIGH Voltage | 2.0                    | —    | —    | 2.0                    | —    | —    | 2.0                    | —    | —    | V    |
| V <sub>IL</sub> | Input LOW Voltage  | —                      | —    | 0.8  | —                      | —    | 0.8  | —                      | —    | 0.8  | V    |
| I <sub>IH</sub> | Input HIGH Current | +20                    | —    | -250 | +20                    | —    | -250 | +20                    | —    | -250 | μA   |
| I <sub>IL</sub> | Input LOW Current  | —                      | —    | -600 | —                      | —    | -600 | —                      | —    | -600 | μA   |

**AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 2.37V$  to  $3.6V$ ,  $GND = 0V$ 

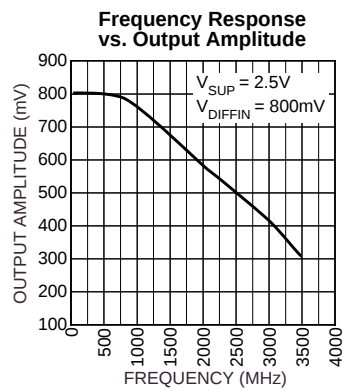
| Symbol             | Parameter                                       | $T_A = -40^{\circ}C$ |      |      | $T_A = +25^{\circ}C$ |      |      | $T_A = +85^{\circ}C$ |      |      | Unit |
|--------------------|-------------------------------------------------|----------------------|------|------|----------------------|------|------|----------------------|------|------|------|
|                    |                                                 | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. | Min.                 | Typ. | Max. |      |
| $f_{MAX}$          | Max Toggle Frequency <sup>(2)</sup>             | 2                    | —    | —    | 2                    | —    | —    | 2                    | —    | —    | GHz  |
| $t_{PD}$           | Propagation Delay (Differential) <sup>(3)</sup> | 0.900                | —    | 1.5  | 0.900                | 1.2  | 1.5  | 0.900                | —    | 1.5  | ns   |
|                    | LVPECL IN<br>LVDS IN                            | 1.1                  | —    | 1.7  | 1.1                  | —    | 1.7  | 1.1                  | —    | 1.7  |      |
| $t_{SKEW}$         | Within-Device Skew <sup>(4)</sup>               | —                    | —    | 35   | —                    | 20   | 35   | —                    | —    | 35   | ps   |
|                    | Part-to-Part Skew <sup>(5)</sup>                | —                    | 100  | 200  | —                    | 100  | 200  | —                    | 100  | 200  | ps   |
| $t_{S(OE)}$        | OE Set-Up Time <sup>(6)</sup>                   | 1.0                  | —    | —    | 1.0                  | —    | —    | 1.0                  | —    | —    | ns   |
| $t_{H(OE)}$        | OE Hold Time <sup>(6)</sup>                     | 0.5                  | —    | —    | 0.5                  | —    | —    | 0.5                  | —    | —    | ns   |
| $t_r$<br>$t_f$     | Output Rise/Fall Time<br>(20% – 80%)            | 300                  | —    | 600  | 300                  | 450  | 600  | 300                  | —    | 600  | ps   |
| $t_{(switchover)}$ | Input Switchover<br>CLK_SEL-to-valid output     | —                    | —    | 1.2  | —                    | —    | 1.2  | —                    | —    | 1.2  | ns   |

**NOTES:**

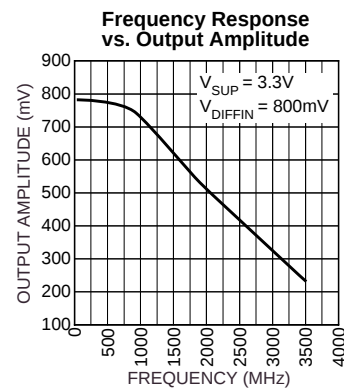
1. Outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$ . Airflow  $\geq 300$ lfpm.
2.  $f_{MAX}$  is defined as the maximum toggle frequency measured. Measured with a 750mV input signal, all loading with  $50\Omega$  to  $V_{CC} - 2V$ .
3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
5. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature. Part-to-part skew is the total skew difference; pin-to-pin skew + part-to-part skew.
6. Set-up and hold time applies to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

**LVDS/LVPECL INPUTS****LVPECL Input Stage****LVDS Input Stage****Figure 1. Simplified LVPECL & LVDS Input Stage**

TYPICAL CHARACTERISTICS



**Frequency Response  
vs. Output Amplitude @2.5V**



**Frequency Response  
vs. Output Amplitude @3.3V**

## LVPECL TERMINATION RECOMMENDATIONS

### Output Considerations

Be sure to properly terminate all outputs as shown below, or equivalent. For AC coupled applications, be sure to include a pull

down resistor at the output of each driver. The emitter follower outputs requires a DC current path to GND. Unused outputs can be left floating with minimal impact on skew and jitter.

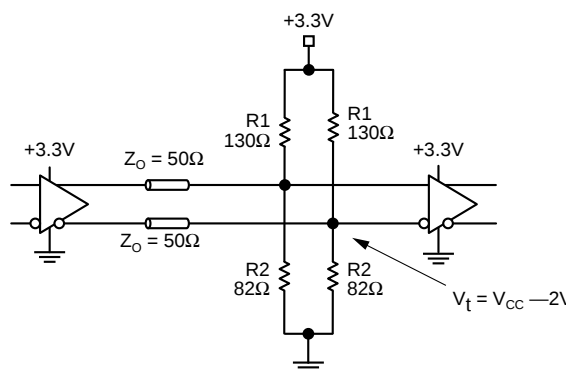


Figure 1. Parallel Termination-Thevenin Equivalent

#### Notes:

- For +2.5V systems:  
R1 = 250Ω  
R2 = 62.5Ω

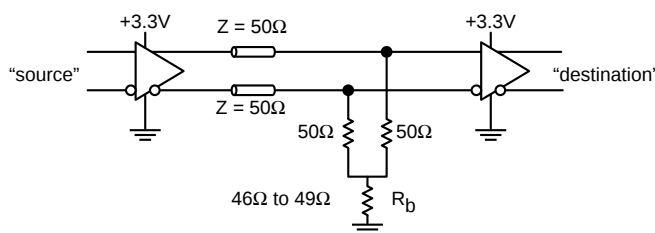
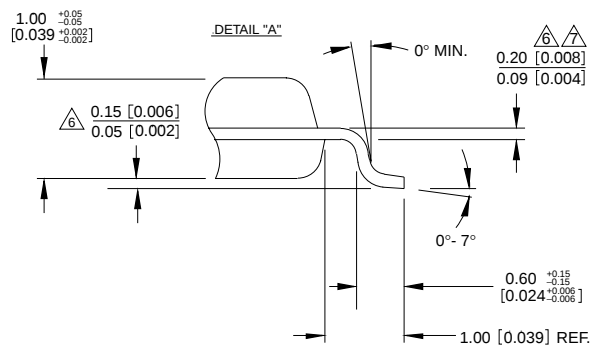
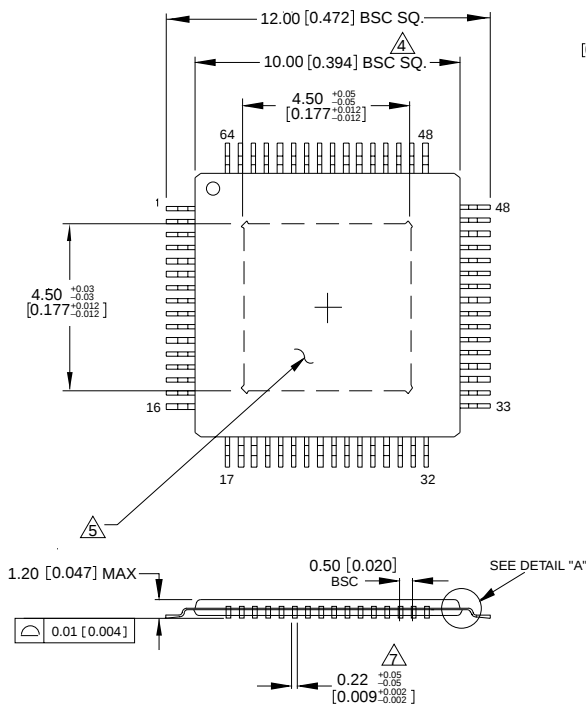


Figure 2. Three-Resistor "Y-Termination"

#### Notes:

- Power-saving alternative to Thevenin termination.
- Place termination resistors as close to destination inputs as possible.
- $R_b$  resistor sets the DC bias voltage equal to  $V_t$ . For +3.3V systems  $R_b = 46\Omega$  to  $50\Omega$ .
- Precision, low-cost 3-Resistor networks are available from resistor manufacturers such as Thin Film Technology ([www.thinfilm.com](http://www.thinfilm.com)).

**64-PIN EPAD-TQFP (DIE UP) (H64-1)****NOTES:**

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX  
MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 03

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.