Power MOSFET

60 V, 39 m Ω , 17 A, Dual N–Channel, Logic Level. Dual SO8FL

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5877NLWF Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Parameter			Syllibol	value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage	9		V _{GS}	±20	V
Continuous Drain Cur-	Steady State	T _{mb} = 25°C	I _D	17	Α
rent $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)		$T_{mb} = 100^{\circ}C$		12	
Power Dissipation		$T_{mb} = 25^{\circ}C$	P_{D}	23	W
R _{ΨJ-mb} (Notes 1, 2, 3)		T _{mb} = 100°C		12	
Continuous Drain Cur-		T _A = 25°C	I _D	6	Α
rent $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	T _A = 100°C		5	
Power Dissipation		T _A = 25°C	P_{D}	3.2	W
$R_{\theta JA}$ (Notes 1, 3)		T _A = 100°C		1.6	
Pulsed Drain Current	$T_A = 25^{\circ}C$, $t_p = 10 \mu s$		I _{DM}	74	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			IS	19	Α
Single Pulse Drain- to-Source Avalanche	(I _{L(pk)} = 14.5 A, L = 0.1 mH)		E _{AS}	10.5	mJ
Energy ($T_J = 25^{\circ}C$, $V_{DD} = 24 \text{ V}$, $V_{GS} =$ 10 V, $R_G = 25 \Omega$)	(I _{L(pk)} = 6.3 A, L = 2 mH)			40	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Note 2, 3)	$R_{\Psi J-mb}$	6.5	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	47	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi (Ψ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface–mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

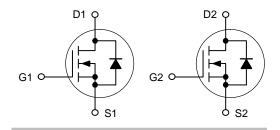


ON Semiconductor®

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V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
60 V	39 mΩ @ 10 V	17 A
	60 mΩ @ 4.5 V	17.8

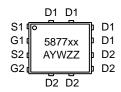
Dual N-Channel





CASE 506BT

MARKING DIAGRAM



5877NL = Specific Device Code for NVMFD5877NL

5877LW = Specific Device Code for NVMFD5877NLWF

A = Assembly Location

Y = Year W = Work Week ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]		
NVMFD5877NLT1G	DFN8 (Pb-Free)	1500 / Tape & Reel		
NVMFD5877NLWFT1G	DFN8 (Pb-Free)	1500 / Tape & Reel		
NVMFD5877NLT3G	DFN8 (Pb-Free)	5000 / Tape & Reel		
NVMFD5877NLWFT3G	DFN8 (Pb-Free)	5000 / Tape & Reel		

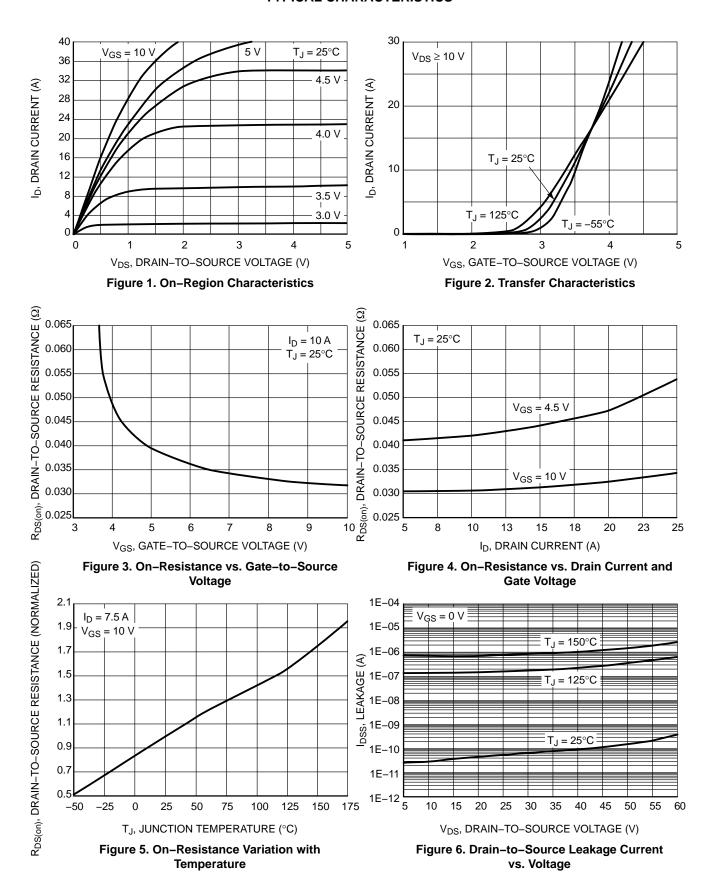
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D =$	= 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	35			53		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1.0	μΑ
		$V_{DS} = 60 \text{ V}$	T _J = 125°C			10	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 250 μΑ	1.0		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				3.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.5 A		31	39	mΩ
	, ,	V _{GS} = 4.5 V	I _D = 7.5 A		42	60	1
Forward Transconductance	9FS	V _{DS} = 15 V, I _D = 5.0 A			7.0		S
CHARGES AND CAPACITANCES	-				•	-	
Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V			540		pF
Output Capacitance	C _{oss}				55		1
Reverse Transfer Capacitance	C _{rss}				36		1
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 5.0 A			5.9		nC
Threshold Gate Charge	Q _{G(TH)}				0.62		1
Gate-to-Source Charge	Q _{GS}				1.64		1
Gate-to-Drain Charge	Q_{GD}				2.80		1
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 4	18V, I _D = 5.0A		11	20	nC
SWITCHING CHARACTERISTICS (No	ote 6)						
Turn-On Delay Time	t _{d(on)}				8.1		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{D}$	s = 48 V.		15.8		1
Turn-Off Delay Time	t _{d(off)}	$I_D = 5.0 \text{ A}, R_G$	$I_D = 5.0 \text{ A}, R_G = 2.5 \Omega$		11.8		1
Fall Time	t _f				3.9		1
Turn-On Delay Time	t _{d(on)}				4.9		ns
Rise Time	t _r	$V_{GS} = 10 \text{ V}, V_{DS}$	s = 48 V,		6.4		1
Turn-Off Delay Time	t _{d(off)}	$I_D = 5.0 \text{ A}, R_G = 2.5 \Omega$			14.5		1
Fall Time	t _f				2.4		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.8	1.2	V
		$I_{S} = 5.0 \text{A}$	T _J = 125°C		0.7		1
Reverse Recovery Time	t _{RR}				14.5		ns
Charge Time	t _a	$V_{GS} = 0 \text{ V, } d_{ S}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 5.0 \text{ A}$			11.5		1
Discharge Time	t _b				3.1		1
Reverse Recovery Charge	Q _{RR}				11		nC
PACKAGE PARASITIC VALUES	-				-	-	
Source Inductance	L _S	T _A = 25°C			0.93		nH
Drain Inductance	L _D				0.005	1	1
Gate Inductance	L _G				1.84	1	1
Gate Resistance	R _G				1.5	1	Ω

^{5.} Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



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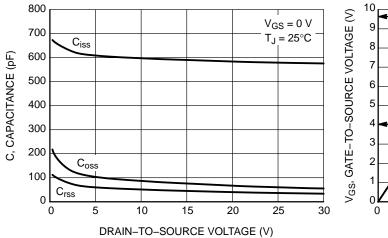


Figure 7. Capacitance Variation

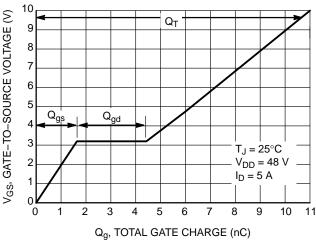


Figure 8. Gate-to-Source vs. Gate Charge

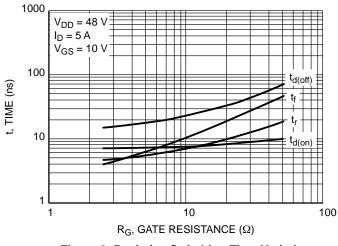


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

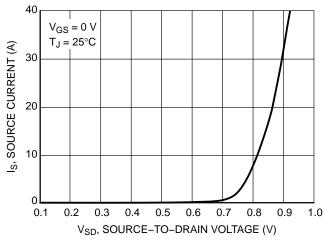


Figure 10. Diode Forward Voltage

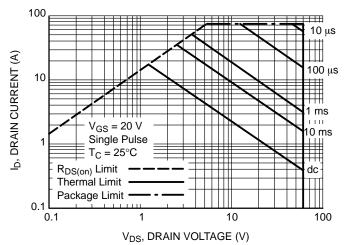


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

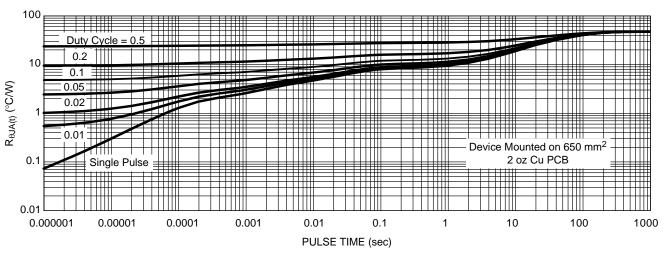
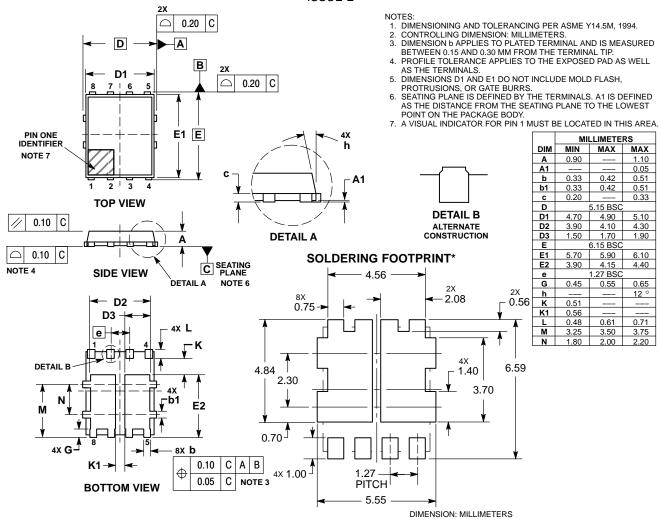


Figure 12. Thermal Response

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT ISSUE E



^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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