# OPAx180 0.1-μV/°C Drift, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers

## 1 Features

- Low Offset Voltage: 75 μV (max)
- Zero-Drift: 0.1 μV/°C
- Low Noise: 10 nV/$\sqrt{\text{Hz}}$
- Very Low 1 / f Noise
- Excellent DC Precision:
  - PSRR: 126 dB
  - CMRR: 114 dB
  - Open-Loop Gain ($A_{OL}$): 120 dB
- Quiescent Current: 525 μA (max)
- Wide Supply Range: ±2 V to ±18 V
- Rail-to-Rail Output:
  Input Includes Negative Rail
- Low Bias Current: 250 pA (typ)
- RFI Filtered Inputs
- *Micro*SIZE Packages

## 2 Applications

- Bridge Amplifiers
- Strain Gauges
- Test Equipment
- Transducer Applications
- Temperature Measurement
- Electronic Scales
- Medical Instrumentation
- Resister Thermal Detectors
- Precision Active Filters

## 3 Description

The OPA180, OPA2180, and OPA4180 operational amplifiers use zero-drift techniques to simultaneously provide low offset voltage (75 μV), and near zero-drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 18 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of 4.0 V to 36 V (±2 V to ±18 V).

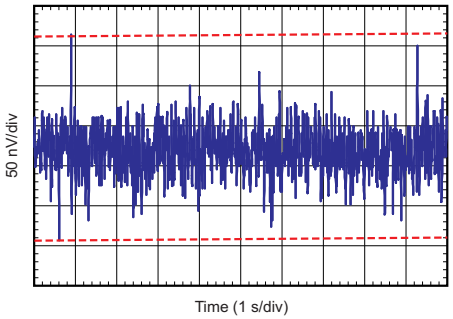
The dual version is offered in VSSOP-8 and SOIC-8 packages. The quad is offered in SOIC-14 and TSSOP-14 packages. All versions are specified for operation from –40°C to 105°C.

**Device Information(1)**

| DEVICE NAME | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA180 | SOT23 (5) | 1.60 mm × 2.90 mm |
| | VSSOP, MSOP (8) | 3.00 mm × 3.00 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| OPA2180 | VSSOP, MSOP (8) | 3.00 mm × 3.00 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| OPA4180 | TSSOP (14) | 5.00 mm × 4.40 mm |
| | SOIC (14) | 8.65 mm × 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Low Noise**
**(Peak-to-Peak Noise = 250 nV)**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (December 2012) to Revision D** — **Page**

- Changed format to meet latest data sheet standards; added *Device Functional Modes*, *Application and Implementation*, and *Power Supply Recommendations* sections, and moved existing sections ... 1
- Added OPA180 to document ... 1
- Added Device Information table ... 1
- Deleted Package Information table ... 3
- OPA180 pin out drawings ... 3
- Added Pin Functions table ... 4
- Added Recommended Operating Conditions table ... 5
- Added Thermal Information: OPA180 table ... 5
- Changed Offset Voltage, *Long-term stability* parameter typical specification in Electrical Characteristics table ... 6
- Changed last sentence of *EMI Rejection* section ... 14

**Changes from Revision B (December 2011) to Revision C** — **Page**

- Changed product status from Mixed Status to Production Data ... 1
- Changed OPA4180 status to Production Data ... 1
- Added package marking to OPS2180 VSSOP-8 row in Package Information table ... 3
- Deleted ordering number and transport media columns from Package Information table ... 3
- Changed Input Bias Current section in Electrical Characteristics ($V_S$ = +4 V to +36 V) table ... 6

**Changes from Revision A (November 2011) to Revision B** — **Page**

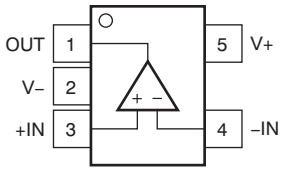
- Changed footnote 1 of Electrical Characteristics table ... 6
- Updated Figure 7 ... 9

## 5 Zero-Drift Amplifier Portfolio

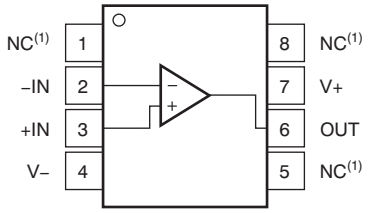
| VERSION | PRODUCT | OFFSET VOLTAGE (μV) | OFFSET VOLTAGE DRIFT (μV/°C) | BANDWIDTH (MHz) |
|---|---|---|---|---|
| Single | OPA188 (4 V to 36 V) | 25 | 0.085 | 2 |
| | OPA180 (4 V to 36 V) | 75 | 0.35 | 2 |
| | OPA333 (5 V) | 10 | 0.05 | 0.35 |
| | OPA378 (5 V) | 50 | 0.25 | 0.9 |
| | OPA735 (12 V) | 5 | 0.05 | 1.6 |
| Dual | OPA2188 (4 V to 36 V) | 25 | 0.085 | 2 |
| | OPA2180 (4 V to 36 V) | 75 | 0.35 | 2 |
| | OPA2333 (5 V) | 10 | 0.05 | 0.35 |
| | OPA2378 (5 V) | 50 | 0.25 | 0.9 |
| | OPA2735 (12 V) | 5 | 0.05 | 1.6 |
| Quad | OPA4188 (4 V to 36 V) | 25 | 0.085 | 2 |
| | OPA4180 (4 V to 36 V) | 75 | 0.35 | 2 |
| | OPA4330 (5 V) | 50 | 0.25 | 0.35 |

## 6 Pin Configuration and Functions

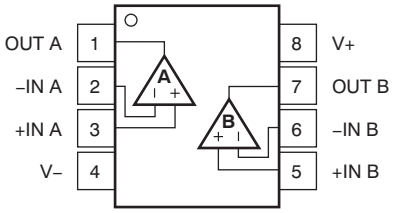
**OPA180**
**DBV Package (SOT23-5)**
**(Top View)**



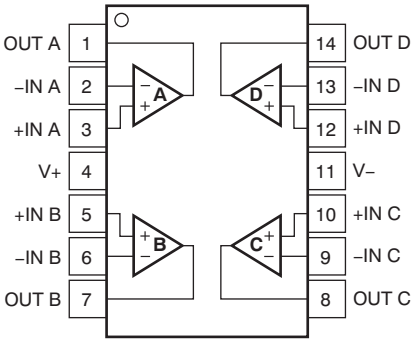

**OPA180**
**D and DGK Packages (SO-8 and MSOP-8)**
**(Top View)**




**OPA2180**
**D, DGK Packages (SOIC-8, VSSOP-8)**
**(Top View)**




**OPA4180**
**D, PW Packages (SOIC-14, TSSOP-14)**
**(Top View)**



**Pin Functions**

| PIN | | | | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | OPA180 | | OPA2180 | OPA4180 | |
| | DBV | D (8), DGK | D (8), DGK | D (14), PW | |
| –IN A | 4 | 2 | 2 | 2 | Inverting input |
| +IN A | 3 | 3 | 3 | 3 | Noninverting input |
| –IN B | — | — | 6 | 6 | Inverting input |
| +IN B | — | — | 5 | 5 | Noninverting input |
| –IN C | — | — | — | 9 | Inverting input |
| +IN C | — | — | — | 10 | Noninverting input |
| –IN D | — | — | — | 13 | Inverting input |
| +IN D | — | — | — | 12 | Noninverting input |
| OUT A | 1 | 6 | 1 | 1 | Output |
| OUT B | — | — | 7 | 7 | Output |
| OUT C | — | — | — | 8 | Output |
| OUT D | — | — | — | 14 | Output |
| V– | 2 | 4 | 4 | 11 | Negative supply or ground (for single-supply operation) |
| V+ | 5 | 7 | 8 | 4 | Positive supply or ground (for single-supply operation) |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | | | ±20, 40 (single supply) | V |
| Signal input terminals | Voltage | (V–) – 0.5 | (V+) + 0.5 | V |
| | Current | | ±10 | mA |
| Output short-circuit(2) | | Continuous | | |
| Operating temperature | | –55 | 105 | °C |
| Storage temperature | | –65 | 150 | °C |
| Junction temperature | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –1.5 | 1.5 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –1 | 1 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage [(V+) – (V–)] | Single supply | 4.5 | | 36 | V |
| | Bipolar supply | ±2.25 | | ±18 | V |
| Operating temperature | | –40 | | 105 | °C |

## 7.4 Thermal Information: OPA180

| THERMAL METRIC(1) | | OPA180 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SO) | DBV (SOT23) | DGK (MSOP) | |
| | | 8 PINS | 5 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 115.8 | 158.8 | 180.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 60.1 | 60.7 | 67.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.4 | 44.8 | 102.1 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.8 | 1.6 | 10.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 55.9 | 4.2 | 100.3 | |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Thermal Information: OPA2180

| THERMAL METRIC(1) | | OPA2180 | | UNIT |
|---|---|---|---|---|
| | | D (SO) | DGK (MSOP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 111.0 | 159.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.9 | 37.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51.7 | 48.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.3 | 1.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 51.1 | 77.1 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.6 Thermal Information: OPA4180

| THERMAL METRIC(1) | | OPA4180 | | UNIT |
|---|---|---|---|---|
| | | D (SO) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 93.2 | 106.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 51.8 | 24.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.4 | 59.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 13.5 | 0.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.2 | 54.3 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.7 Electrical Characteristics: $V_S$ = ±2 V to ±18 V ($V_S$ = 4 V to 36 V)

At $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{COM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{IO}$ | Input offset voltage | | | | 15 | 75 | µV |
| $dV_{IO}/dT$ | Input offset voltage drift | | $T_A$ = –40°C to 105°C | | 0.1 | 0.35 | µV/°C |
| PSRR | Power-supply rejection ratio | | $V_S$ = 4 V to 36 V, $V_{CM}$ = $V_S$ / 2 | | 0.1 | 0.5 | µV/V |
| | | | $T_A$ = –40°C to 105°C, $V_S$ = 4 V to 36 V, $V_{CM}$ = $V_S$ / 2 | | | 0.5 | µV/V |
| | Long-term stability | | | | 4 (1) | | µV |
| | Channel separation, dc | | | | 1 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_{IB}$ | Input bias current | | OPA2180 | | ±0.25 | ±1 | nA |
| | | | OPA2180, $T_A$ = –40°C to 105°C | | | ±5 | nA |
| | | | OPA4180, OPA180 | | ±0.25 | ±1.7 | nA |
| | | | OPA4180, OPA180, $T_A$ = –40°C to 105°C | | | ±6 | nA |
| $I_{IO}$ | Input offset current | | OPA2180 | | ±0.5 | ±2 | nA |
| | | | OPA2180, $T_A$ = –40°C to 105°C | | | ±2.5 | nA |
| | | | OPA4180, OPA180 | | | ±3.4 | nA |
| | | | OPA4180, OPA180, $T_A$ = –40°C to 105°C | | | ±3 | nA |
| **NOISE** | | | | | | | |
| | Input voltage noise | | f = 0.1 Hz to 10 Hz | | 0.25 | | $µV_{PP}$ |
| $e_n$ | Input voltage noise density | | f = 1 kHz | | 10 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input current noise density | | f = 1 kHz | | 10 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | V– | | (V+) – 1.5 | V |
| CMRR | Common-mode rejection ratio | | (V–) < $V_{CM}$ < (V+) – 1.5 V | 104 | 114 | | dB |
| | | | $T_A$ = –40°C to 105°C, (V–) + 0.5 V < $V_{CM}$ < (V+) – 1.5 V | 100 | 104 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| $z_{id}$ | Differential | | | | 100 \|\| 6 | | MΩ \|\| pF |
| $z_{ic}$ | Common-mode | | | | 6 \|\| 9.5 | | $10^{12}$ Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | | (V–) + 500 mV < $V_O$ < (V+) – 500 mV, $R_L$ = 10 kΩ | 110 | 120 | | dB |
| | | | $T_A$ = –40°C to 105°C, (V–) + 500 mV < $V_O$ < (V+) – 500 mV, $R_L$ = 10 kΩ | 104 | 114 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain bandwidth product | | | | 2 | | MHz |
| SR | Slew rate | | G = 1 | | 0.8 | | V/µs |
| $t_s$ | Settling time | 0.1% | $V_S$ = ±18 V, G = 1, 10-V step | | 22 | | µs |
| | | 0.01% | $V_S$ = ±18 V, G = 1, 10-V step | | 30 | | µs |
| $t_{or}$ | Overload recovery time | | $V_{IN}$ × G = $V_S$ | | 1 | | µs |
| THD+N | Total harmonic distortion + noise | | f = 1 kHz, G = 1, $V_{OUT}$ = 1 $V_{RMS}$ | | 0.0001% | | |

(1) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits, or approximately 4 µV.

## Electrical Characteristics: $V_S$ = ±2 V to ±18 V ($V_S$ = 4 V to 36 V) (continued)

At $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, and $V_{COM}$ = $V_{OUT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| | Voltage output swing from rail | No load | | 8 | 18 | mV |
| | | $R_L$ = 10 kΩ | | 250 | 300 | mV |
| | | $T_A$ = –40°C to 105°C, $R_L$ = 10 kΩ | | 325 | 360 | mV |
| $I_{OS}$ | Short-circuit current | | | ±18 | | mA |
| $r_o$ | Output resistance (open loop) | f = 2 MHz, $I_O$ = 0 mA | | 120 | | Ω |
| $C_{LOAD}$ | Capacitive load drive | | | 1 | | nF |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Operating voltage range | | ±2 (or 4) | | ±18 (or 36) | V |
| $I_Q$ | Quiescent current (per amplifier) | | | 450 | 525 | µA |
| | | $T_A$ = –40°C to 105°C, $I_O$ = 0 mA | | | 600 | µA |
| **TEMPERATURE** | | | | | | |
| | Specified range | | –40 | | 105 | °C |
| | Operating range | | –40 | | 105 | °C |

## 7.8 Typical Characteristics

**Table 1. Characteristic Performance Measurements**

| DESCRIPTION | FIGURE |
|---|---|
| $I_B$ and $I_{OS}$ vs Common-Mode Voltage | Figure 1 |
| Input Bias Current vs Temperature | Figure 2 |
| Output Voltage Swing vs Output Current (Maximum Supply) | Figure 3 |
| CMRR vs Temperature | Figure 4 |
| 0.1-Hz to 10-Hz Noise | Figure 5 |
| Input Voltage Noise Spectral Density vs Frequency | Figure 6 |
| Open-Loop Gain and Phase vs Frequency | Figure 7 |
| Open-Loop Gain vs Temperature | Figure 8 |
| Open-Loop Output Impedance vs Frequency | Figure 9 |
| Small-Signal Overshoot vs Capacitive Load (100-mV Output Step) | Figure 10, Figure 11 |
| No Phase Reversal | Figure 12 |
| Positive Overload Recovery | Figure 13 |
| Negative Overload Recovery | Figure 14 |
| Small-Signal Step Response (100 mV) | Figure 15, Figure 16 |
| Large-Signal Step Response | Figure 17, Figure 18 |
| Large-Signal Settling Time (10-V Positive Step) | Figure 19 |
| Large-Signal Settling Time (10-V Negative Step) | Figure 20 |
| Short-Circuit Current vs Temperature | Figure 21 |
| Maximum Output Voltage vs Frequency | Figure 22 |
| Channel Separation vs Frequency | Figure 23 |
| EMIRR IN+ vs Frequency | Figure 24 |

## 7.9 Typical Characteristics

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

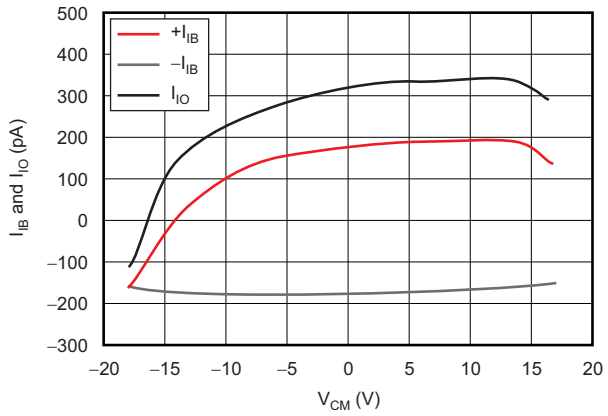



**Figure 1. $I_{IB}$ and $I_{IO}$ vs Common-Mode Voltage**

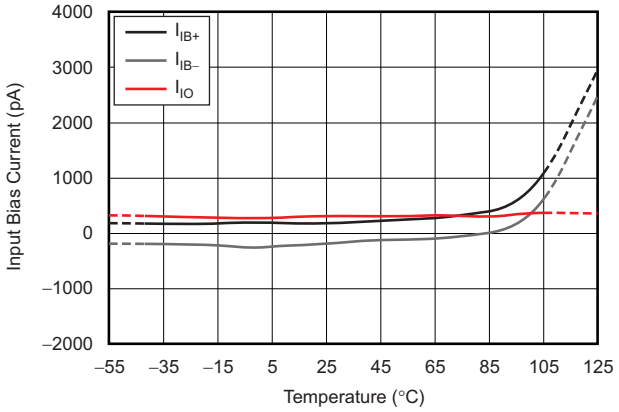



**Figure 2. Input Bias Current vs Temperature**

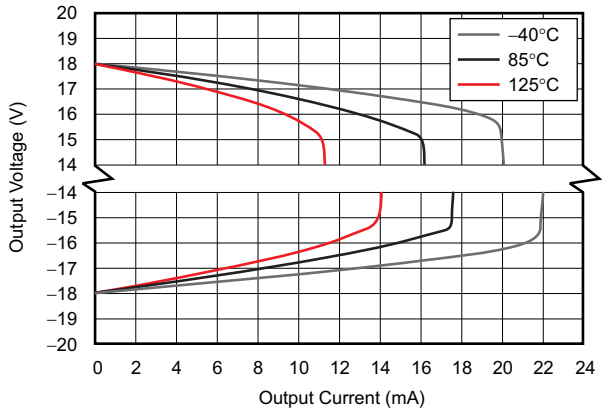
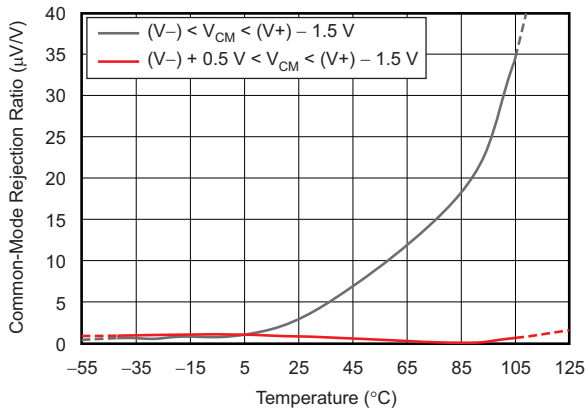
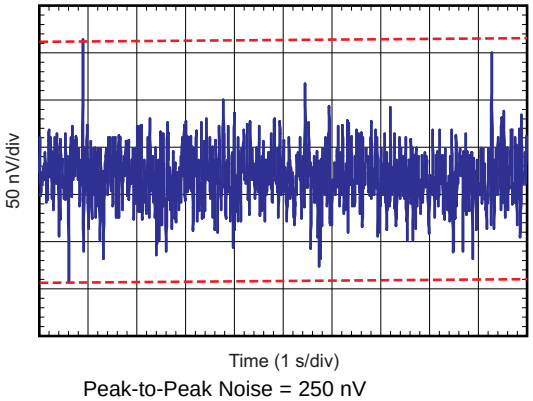



**Figure 3. Output Voltage Swing vs Output Current (Maximum Supply)**




$V_{SUPPLY}$ = ±2 V

**Figure 4. CMRR vs Temperature**




Peak-to-Peak Noise = 250 nV

**Figure 5. 0.1-Hz to 10-Hz Noise**

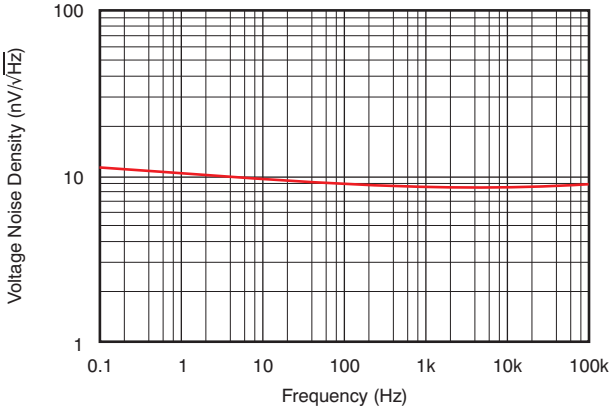



**Figure 6. Input Voltage Noise Spectral Density vs Frequency**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

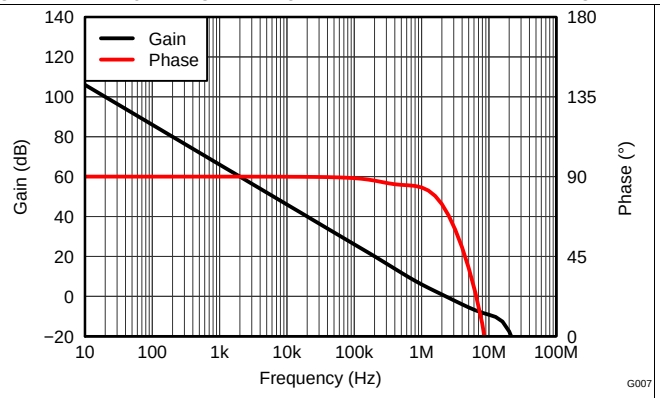



**Figure 7. Open-Loop Gain and Phase vs Frequency**

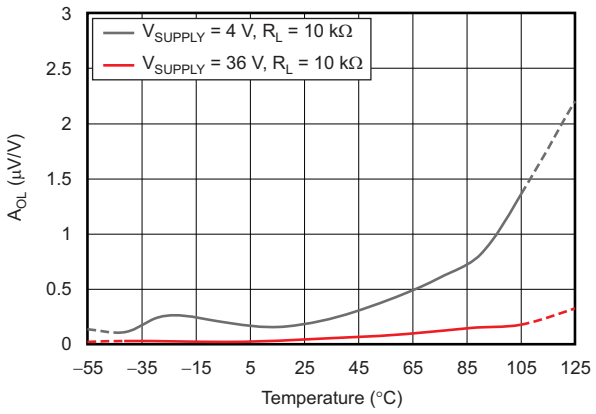



**Figure 8. Open-Loop Gain vs Temperature**

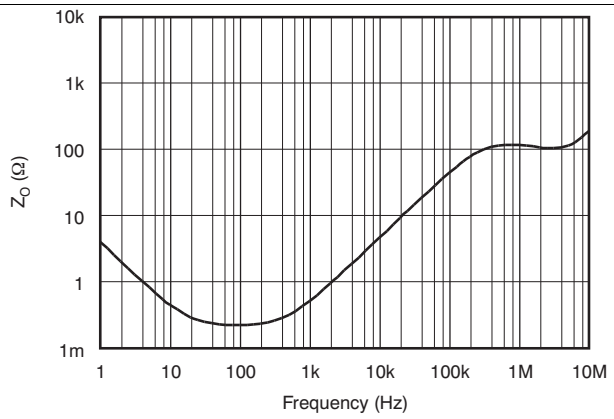
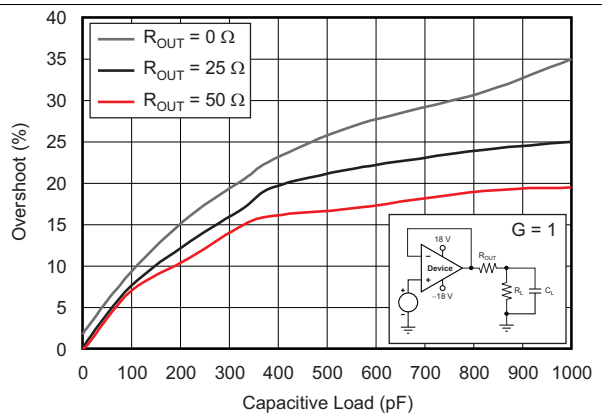
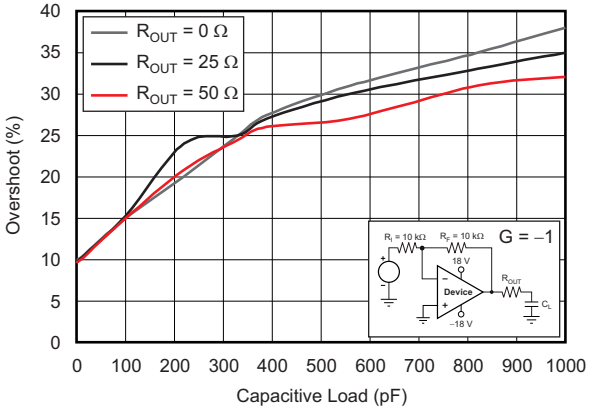



**Figure 9. Open-Loop Output Impedance vs Frequency**




$R_L$ = 10 kΩ

**Figure 10. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**




$R_L$ = 10 kΩ

**Figure 11. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

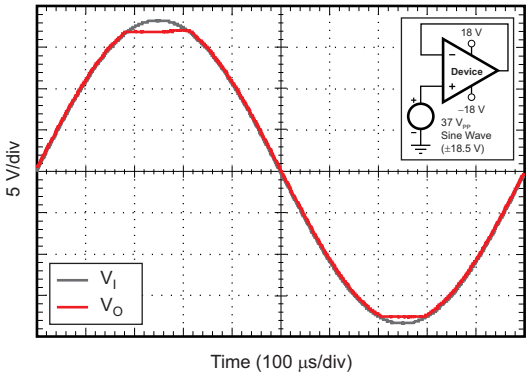



**Figure 12. No Phase Reversal**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

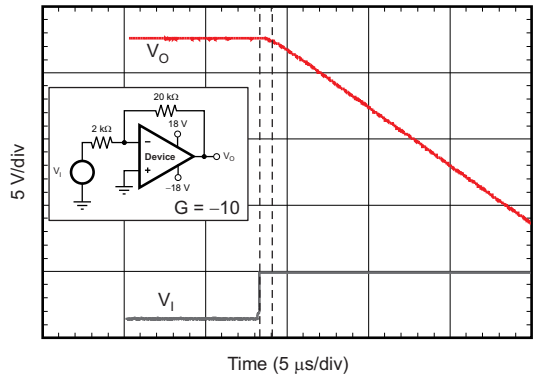



**Figure 13. Positive Overload Recovery**

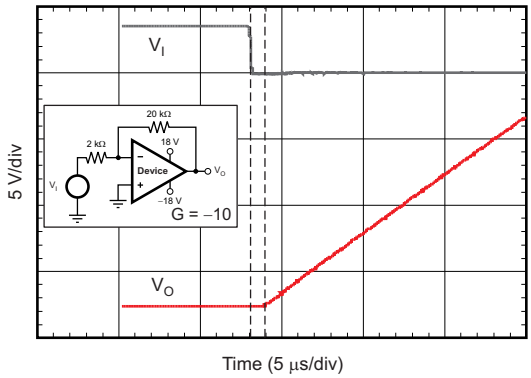
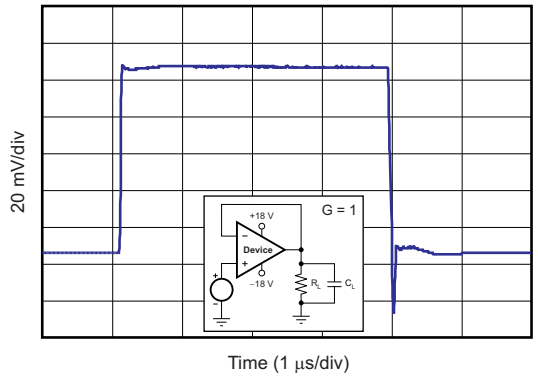
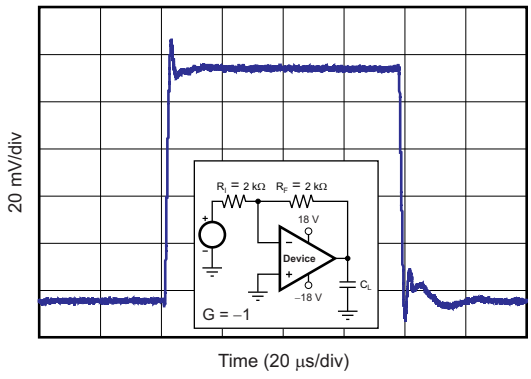



**Figure 14. Negative Overload Recovery**



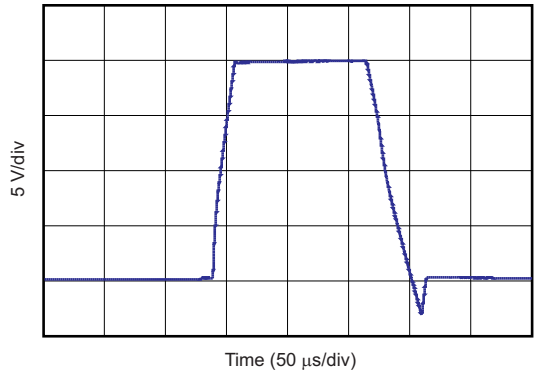

$R_L$ = 10 kΩ $C_L$ = 10 pF

**Figure 15. Small-Signal Step Response (100 mV)**



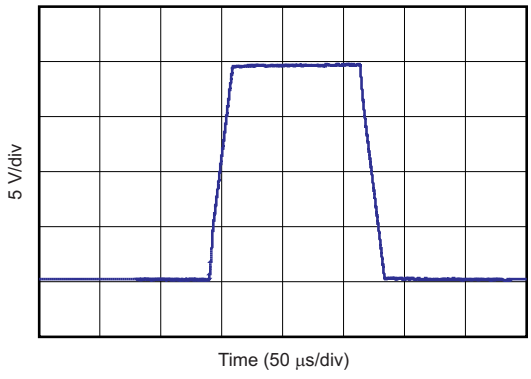

$R_L$ = 10 kΩ $C_L$ = 10 pF

**Figure 16. Small-Signal Step Response (100 mV)**




G = 1 $R_L$ = 10 kΩ $C_L$ = 10 pF

**Figure 17. Large-Signal Step Response**




G = –1 $R_L$ = 10 kΩ $C_L$ = 10 pF

**Figure 18. Large-Signal Step Response**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

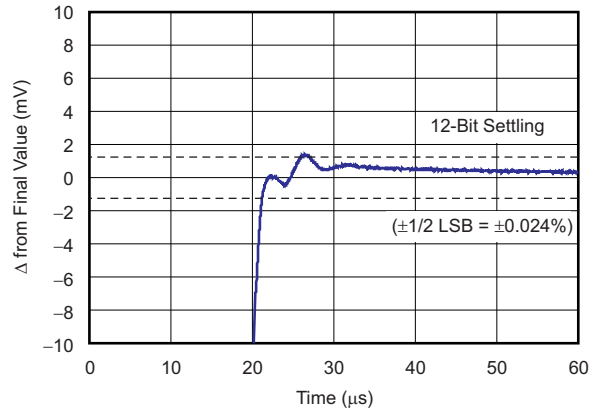



**Figure 19. Large-Signal Settling Time (10-V Positive Step)**

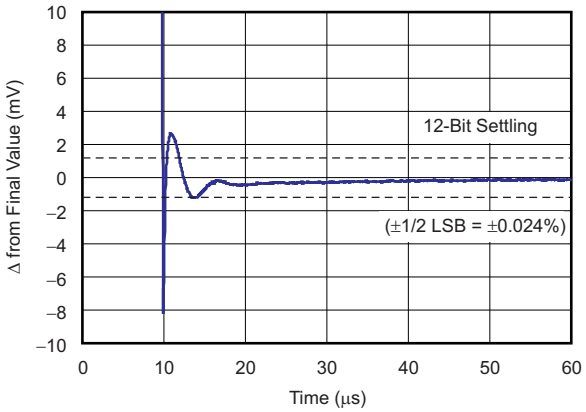



**Figure 20. Large-Signal Settling Time (10-V Negative Step)**

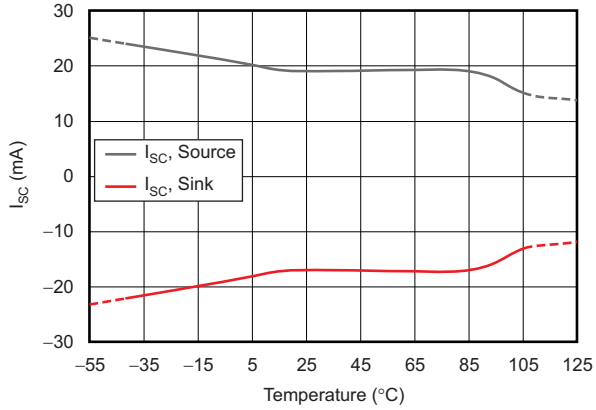



**Figure 21. Short-Circuit Current vs Temperature**

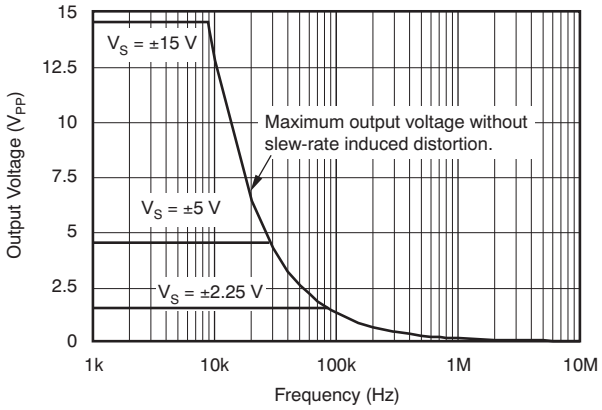



**Figure 22. Maximum Output Voltage vs Frequency**

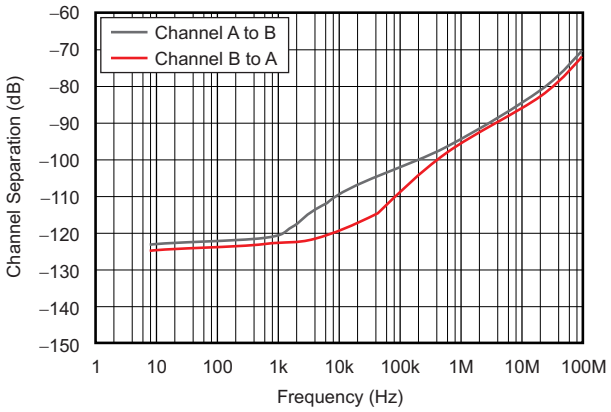



**Figure 23. Channel Separation vs Frequency**

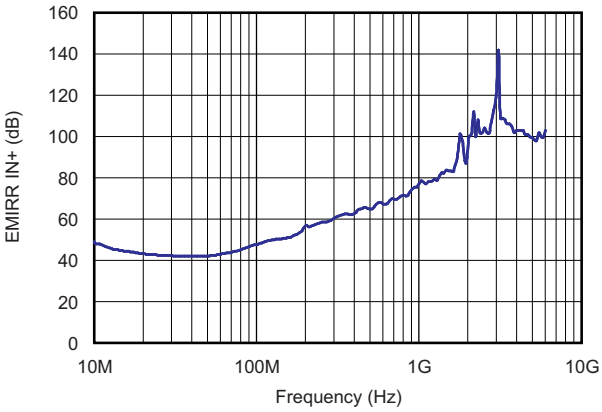


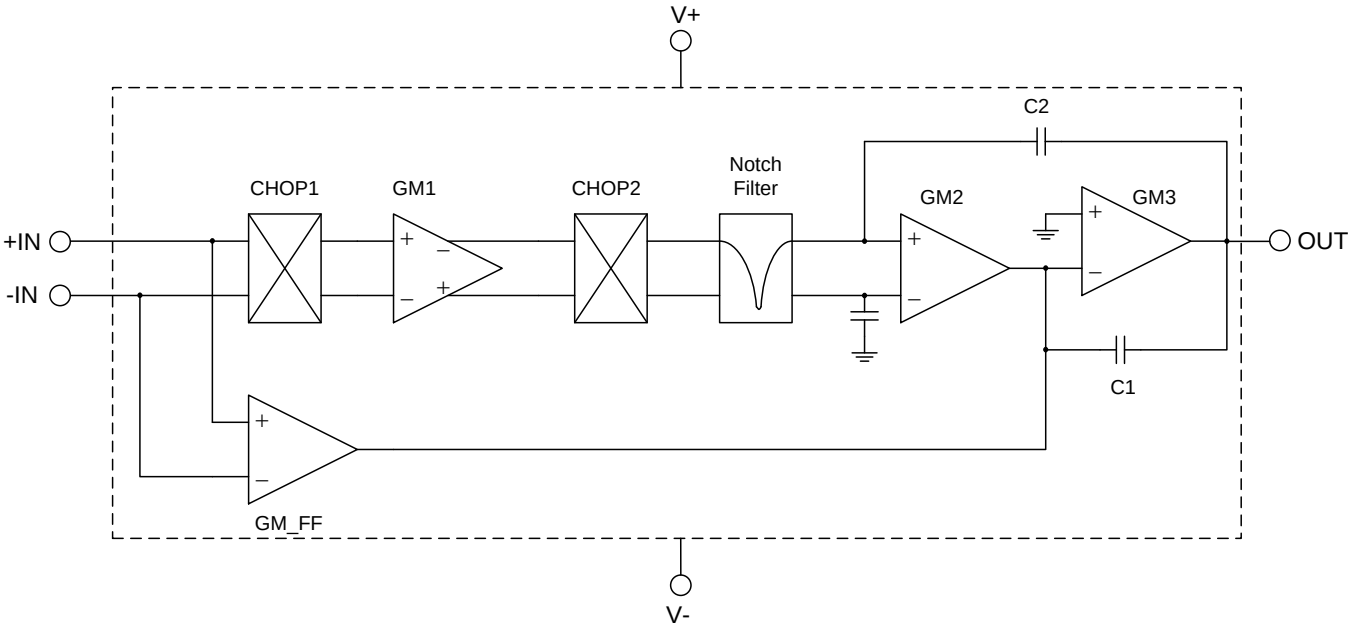

**Figure 24. EMIRR IN+ vs Frequency**

# 8 Detailed Description

## 8.1 Overview

The OPAx180 family of operational amplifiers combine precision offset and drift with excellent overall performance, making them ideal for many precision applications. The precision offset drift of only 0.1 µV/°C provides stability over the entire temperature range. In addition, the devices offer excellent overall performance with high CMRR, PSRR, and $A_{OL}$. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Operating Characteristics

The OPAx180 family of amplifiers is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to 105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

## Feature Description (continued)

### 8.3.2 EMI Rejection

The OPAx180 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx180 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 25 shows the results of this testing on the OPAx180. Detailed information can also be found in the application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

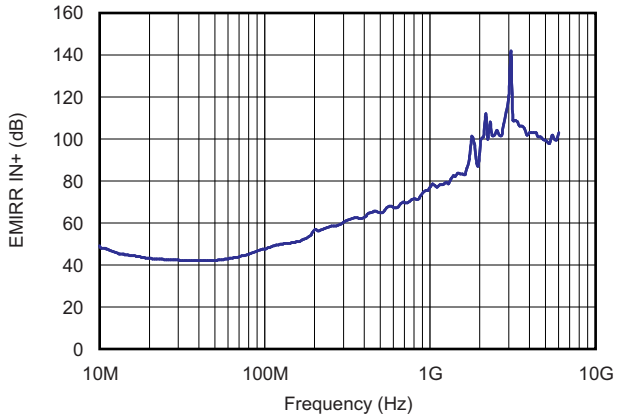



**Figure 25. OPAx180 EMIRR Testing**

### 8.3.3 Phase-Reversal Protection

The OPAx180 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx180 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 26.

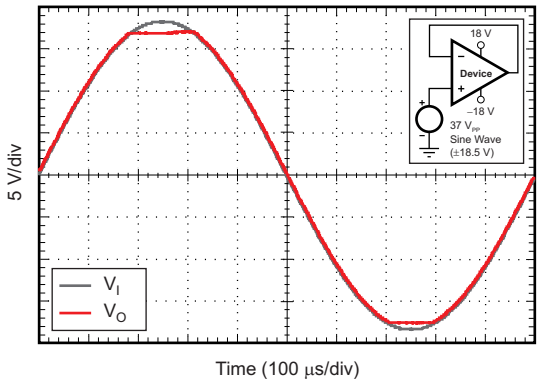



**Figure 26. No Phase Reversal**

## Feature Description (continued)

### 8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx180 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50 Ω) in series with the output. Figure 27 and Figure 28 illustrate graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$. Also, refer to the Applications Report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

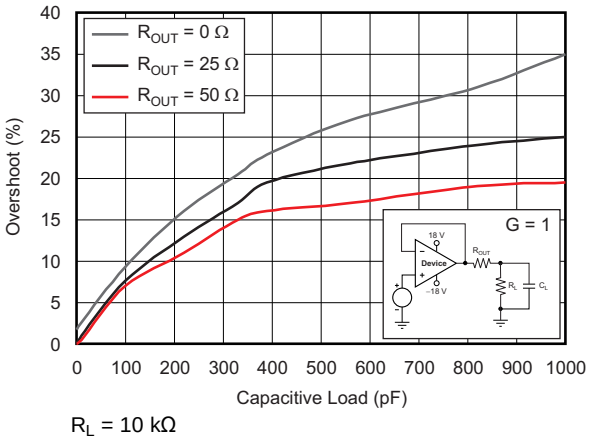



**Figure 27. Small-Signal Overshoot Versus Capacitive Load (100-mV Output Step)**

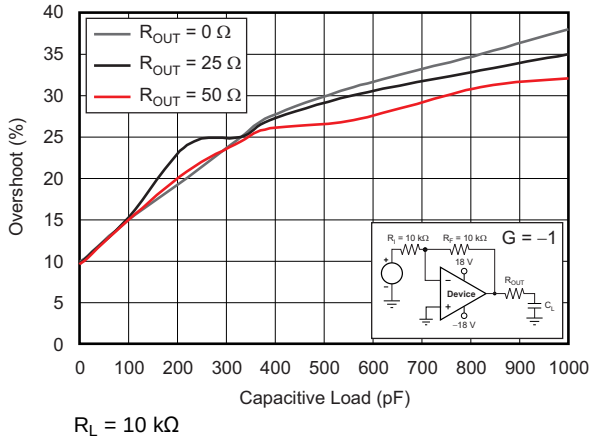



**Figure 28. Small-Signal Overshoot Versus Capacitive Load (100-mV Output Step)**

### 8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 29 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

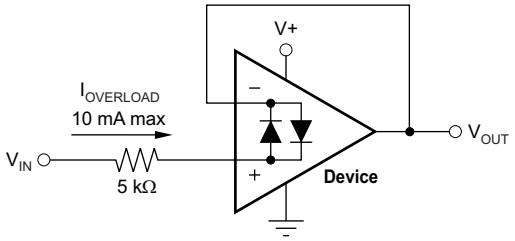



**Figure 29. Input Current Protection**

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

## Feature Description (continued)

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

## 8.4 Device Functional Modes

The OPA180, OPA2180, and OPA4180 are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application. In single-supply operation with V– at ground (0 V), V+ can be any value between 4 V and 36 V. In dual-supply operation the supply voltage difference between V– and V+ is from 4 V to 36 V. Typical examples of dual-supply configuration are ±5 V, ±10 V, ±15 V, and ±18 V. However the supplies must not be symmetrical. Less common examples are V– at –3V and V+ at 9 V or V– at –16 V and V+ at 5 V. Any combination where the difference between V– and V+ is at least 4 V and no greater than 36 V is within the normal operating capabilities of these devices.

# 9 Application and Implementation

## 9.1 Application Information

The OPAx180 family offers excellent dc precision and ac performance. These devices operate up to 36-V supply rails and offer rail-to-rail output, ultra-low offset voltage, and offset voltage drift as well as 2-MHz bandwidth. These features make the OPAx180 a robust, high-performance amplifier for high-voltage industrial applications.

## 9.2 Typical Applications

These application examples highlight only a few of the circuits where the OPAx180 can be used.

### 9.2.1 Bipolar ±10-V Analog Output from a Unipolar Voltage Output DAC

This design is used for conditioning a unipolar digital-to-analog converter (DAC) into an accurate bipolar signal source using the OPA180 and three resistors. The circuit is designed with reactive load stability in mind and is compensated to drive nearly any conventional capacitive load associated with long cable lengths.

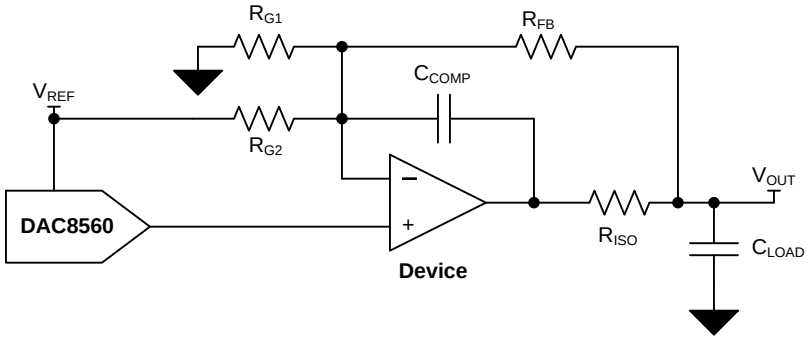



**Figure 30. Circuit Schematic**

#### *9.2.1.1 Design Requirements*

The design requirements are as follows:

- DAC supply voltage: +5-V dc
- Amplifier supply voltage: ±15-V dc
- Input: 3-wire, 24-bit SPI
- Output: ±10-V dc

#### *9.2.1.2 Detailed Design Procedure*

##### 9.2.1.2.1 Component Selection

**DAC:** For convenience, devices with an external reference option or devices with accessible internal references are desirable in this application because the reference is used to create an offset. The DAC selection in this design should primarily be based on dc error contributions typically described by offset error, gain error, and integral nonlinearity error. Occasionally, additional specifications are provided that summarize end-point errors of the DAC typically called zero-code and full-scale errors. For ac applications, additional consideration may be placed on slew rate and settling time.

**Amplifier:** Amplifier input offset voltage ($V_{IO}$) is a key consideration for this design. $V_{IO}$ of an operational amplifier is a typical data sheet specification but in-circuit performance is also affected by drift over temperature, the common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR); thus consideration should be given to these parameters as well. For ac operation, additional considerations should be made concerning slew rate and settling time. Input bias current ($I_{IB}$) can also be a factor, but typically the resistor network is implemented with sufficiently small resistor values that the effects of input bias current are negligible.

## Typical Applications (continued)

**Passive:** Resistor matching for the op-amp resistor network is critical for the success of this design and components should be chosen with tight tolerances. For this design 0.1% resistor values are implemented but this constraint may be adjusted based on application-specific design goals. Resistor matching contributes to both offset error and gain error in this design; see the TI Precision Design TIPD125, *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC* for further details. The tolerance of stability components RISO and CCOMP is not critical and 1% components are acceptable.

### *9.2.1.3 Application Curves*

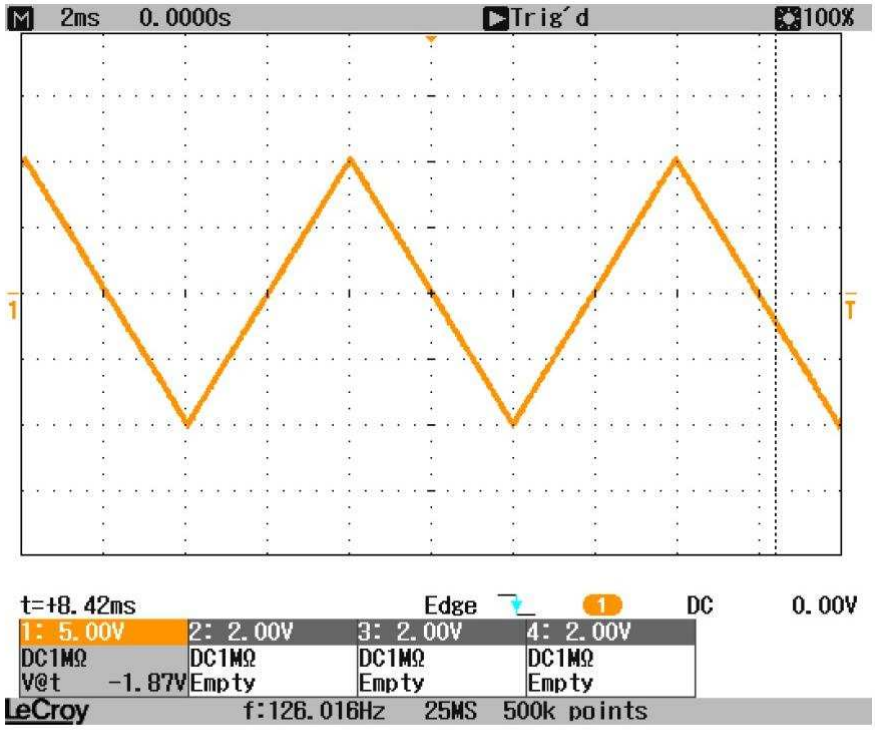



**Figure 31. Full-Scale Output Waveform**

## Typical Applications (continued)

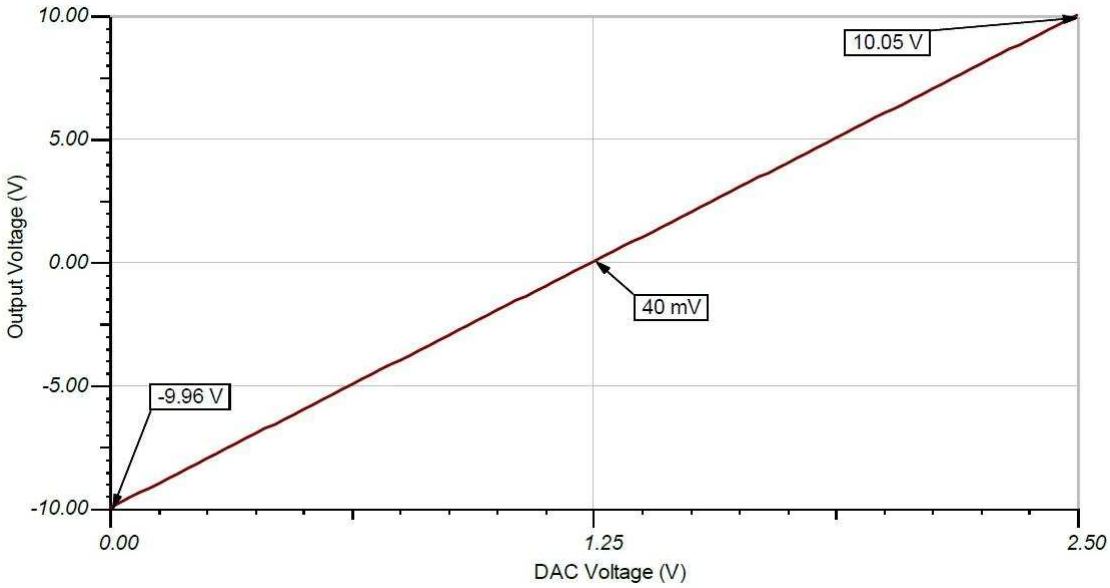



**Figure 32. DC Transfer Characteristic**

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD125, *Bipolar ±10V Analog Output from a Unipolar Voltage Output DAC*

### 9.2.2 Discrete INA + Attenuation

The OPA180 can be used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs).

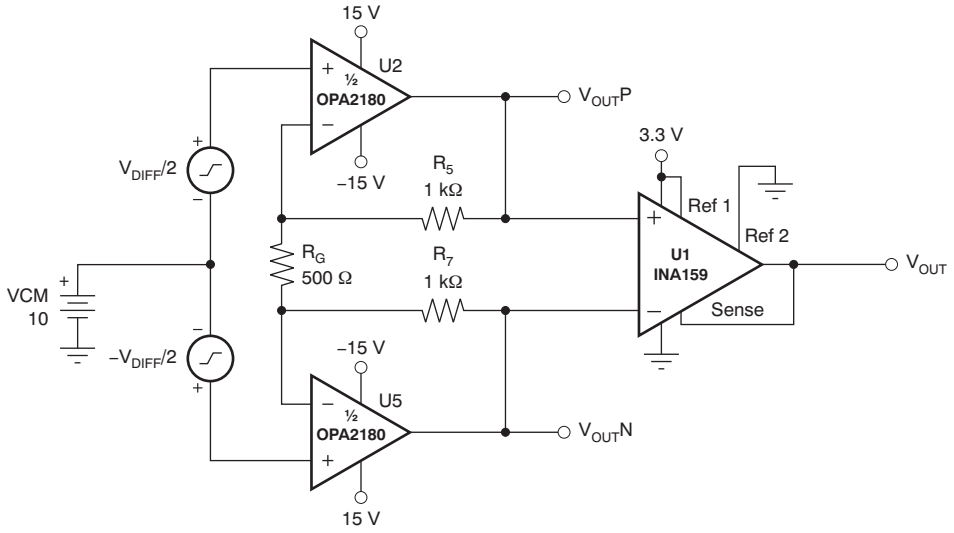
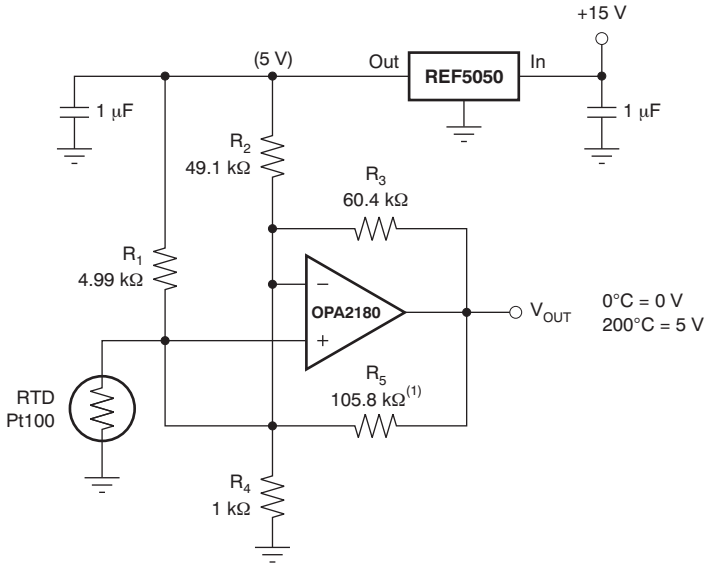



**Figure 33. Discrete INA + Attenuation for ADC with 3.3-V Supply**

### 9.2.3 RTD Amplifier

The OPA180 is excellent for use in analog linearization of resistance temperature detectors (RTDs). The below circuit combines the precision of the OPA180 amplifier and the precision reference REF5050 to linearize a Pt100 RTD.




(1) $R_5$ provides positive-varying excitation to linearize output.

**Figure 34. RTD Amplifier with Linearization**

## 10 Power Supply Recommendations

The OPA180 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Layout* section.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

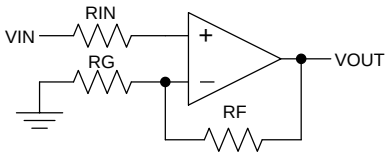
# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the *Circuit Board Layout Techniques* (SLOA089).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 35, keeping RF and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Example




(Schematic Representation)

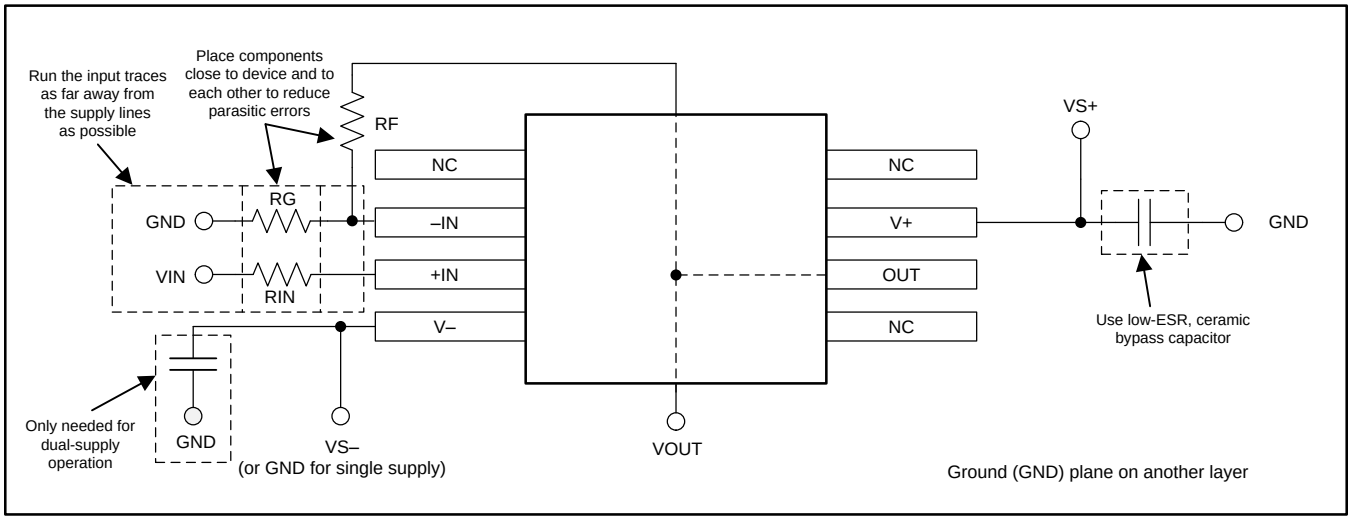



**Figure 35. Operational Amplifier Board Layout for Noninverting Configuration**

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA180 | Click here | Click here | Click here | Click here | Click here |
| OPA2180 | Click here | Click here | Click here | Click here | Click here |
| OPA4180 | Click here | Click here | Click here | Click here | Click here |

## 12.2 Trademarks

All trademarks are the property of their respective owners.

## 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA180ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA180 | Samples |
| OPA180IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | SHJ | Samples |
| OPA180IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | SHJ | Samples |
| OPA180IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | SHK | Samples |
| OPA180IDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | SHK | Samples |
| OPA180IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA180 | Samples |
| OPA2180ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 2180 | Samples |
| OPA2180IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | 2180 | Samples |
| OPA2180IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 105 | 2180 | Samples |
| OPA2180IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 2180 | Samples |
| OPA4180ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA4180 | Samples |
| OPA4180IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA4180 | Samples |
| OPA4180IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA4180 | Samples |
| OPA4180IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | OPA4180 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

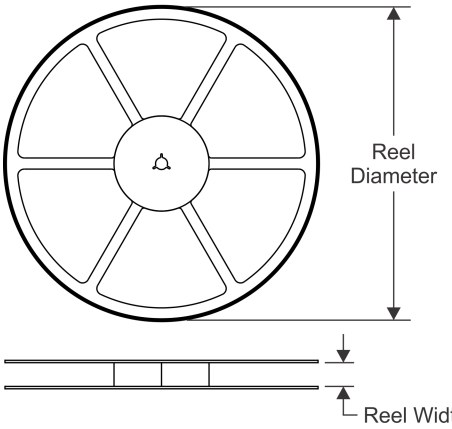
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

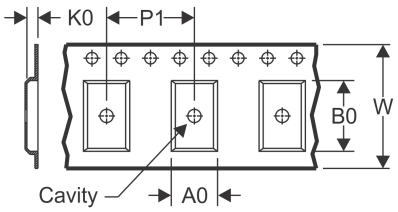
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

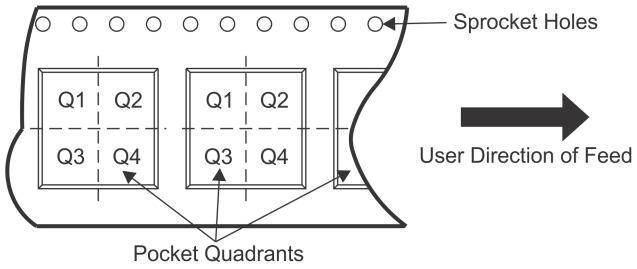



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

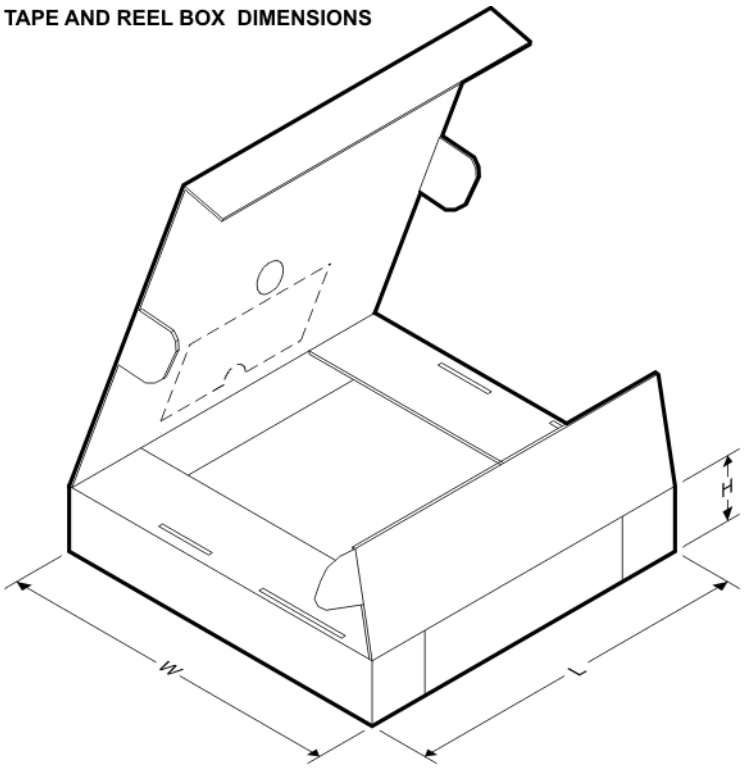
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA180IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA180IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA180IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA180IDGKT | VSSOP | DGK | 8 | 250 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA180IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2180IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2180IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4180IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4180IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

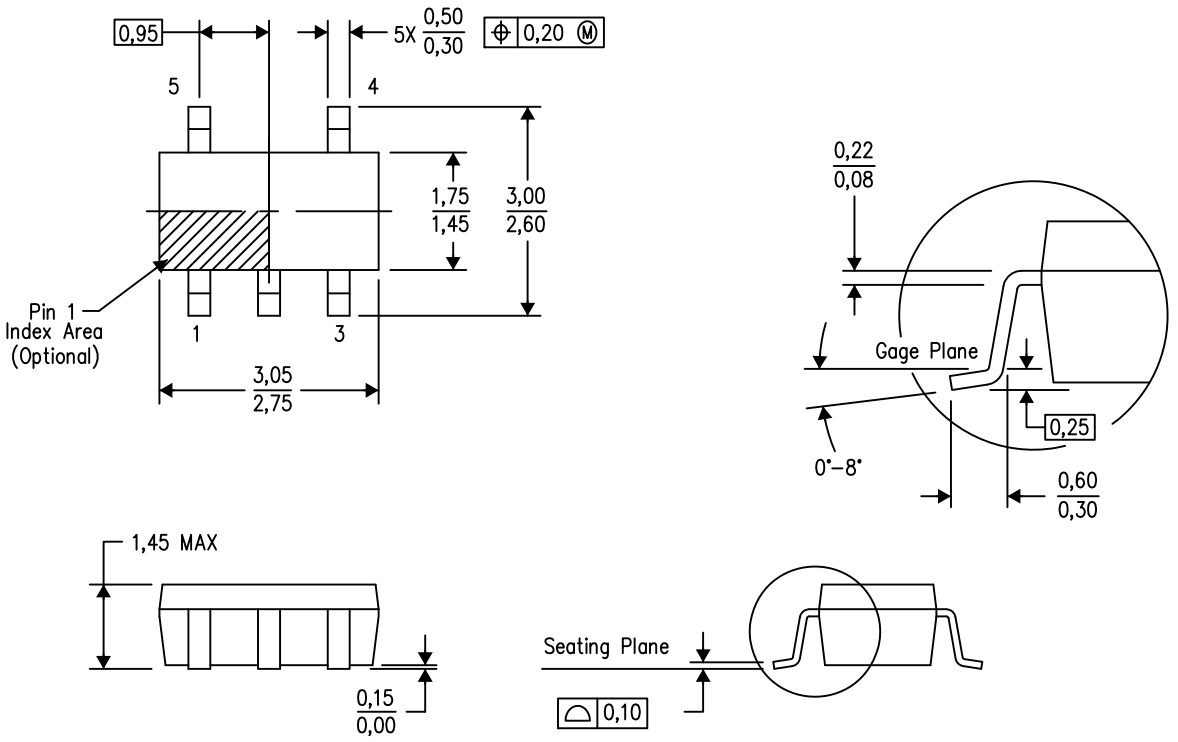
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA180IDBVR | SOT-23 | DBV | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| OPA180IDBVT | SOT-23 | DBV | 5 | 250 | 223.0 | 270.0 | 35.0 |
| OPA180IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| OPA180IDGKT | VSSOP | DGK | 8 | 250 | 223.0 | 270.0 | 35.0 |
| OPA180IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA2180IDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2180IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA4180IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| OPA4180IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

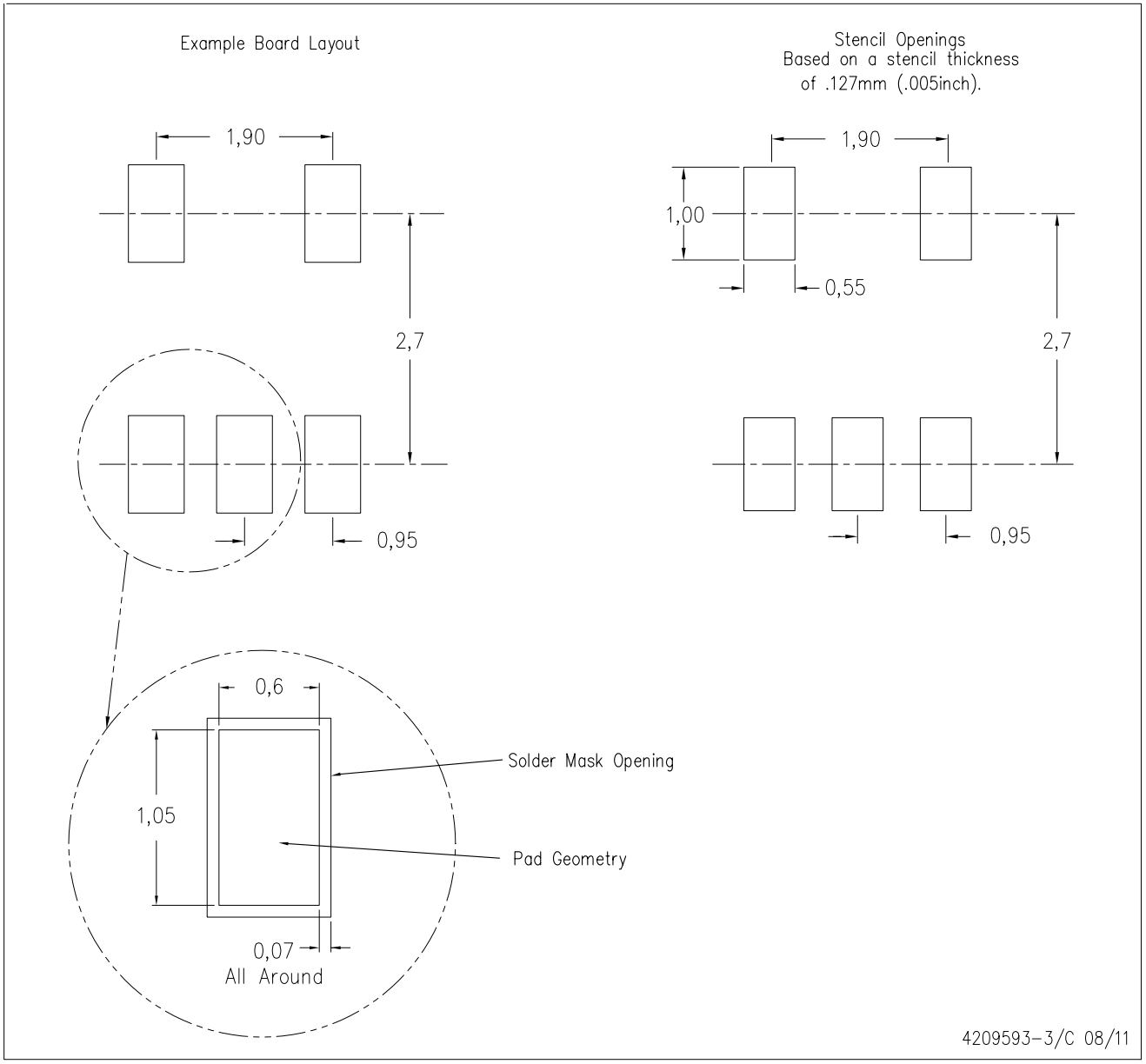
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

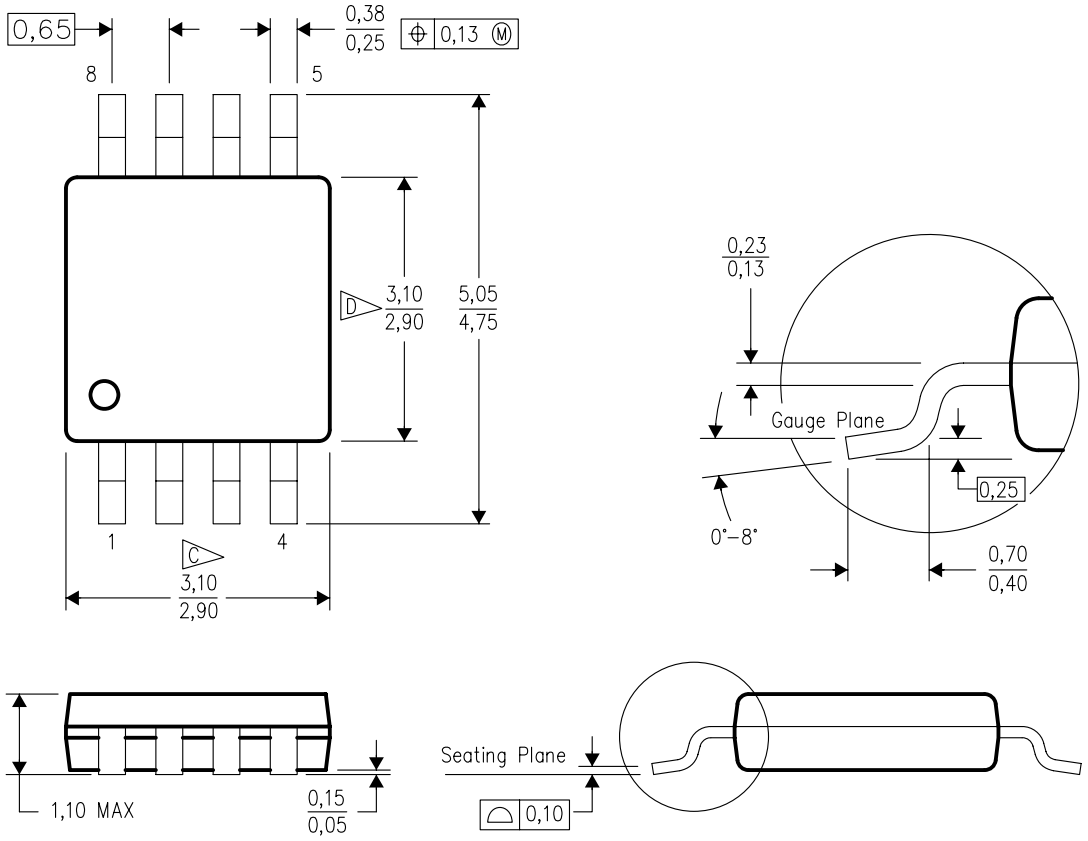
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

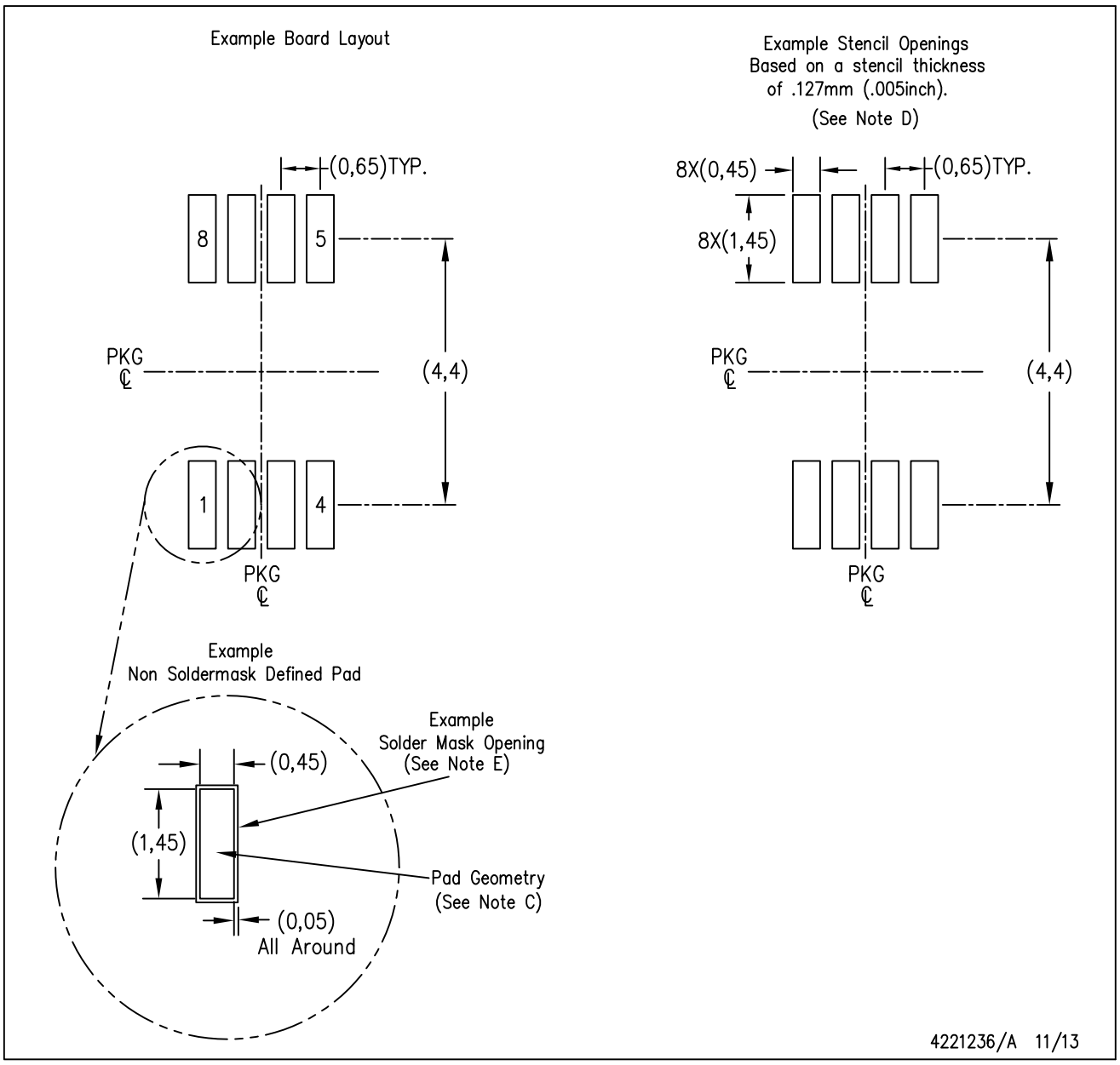
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

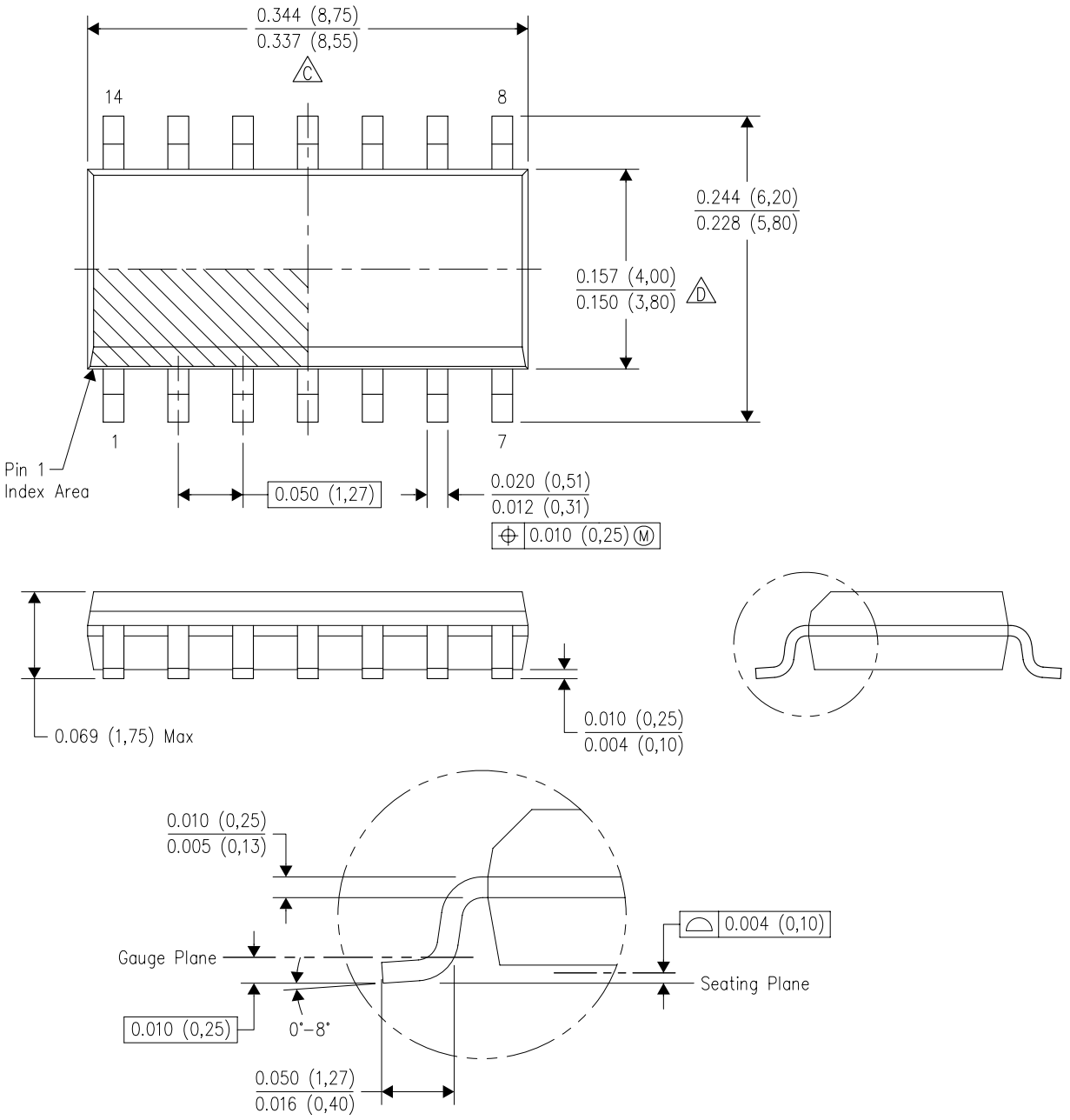
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

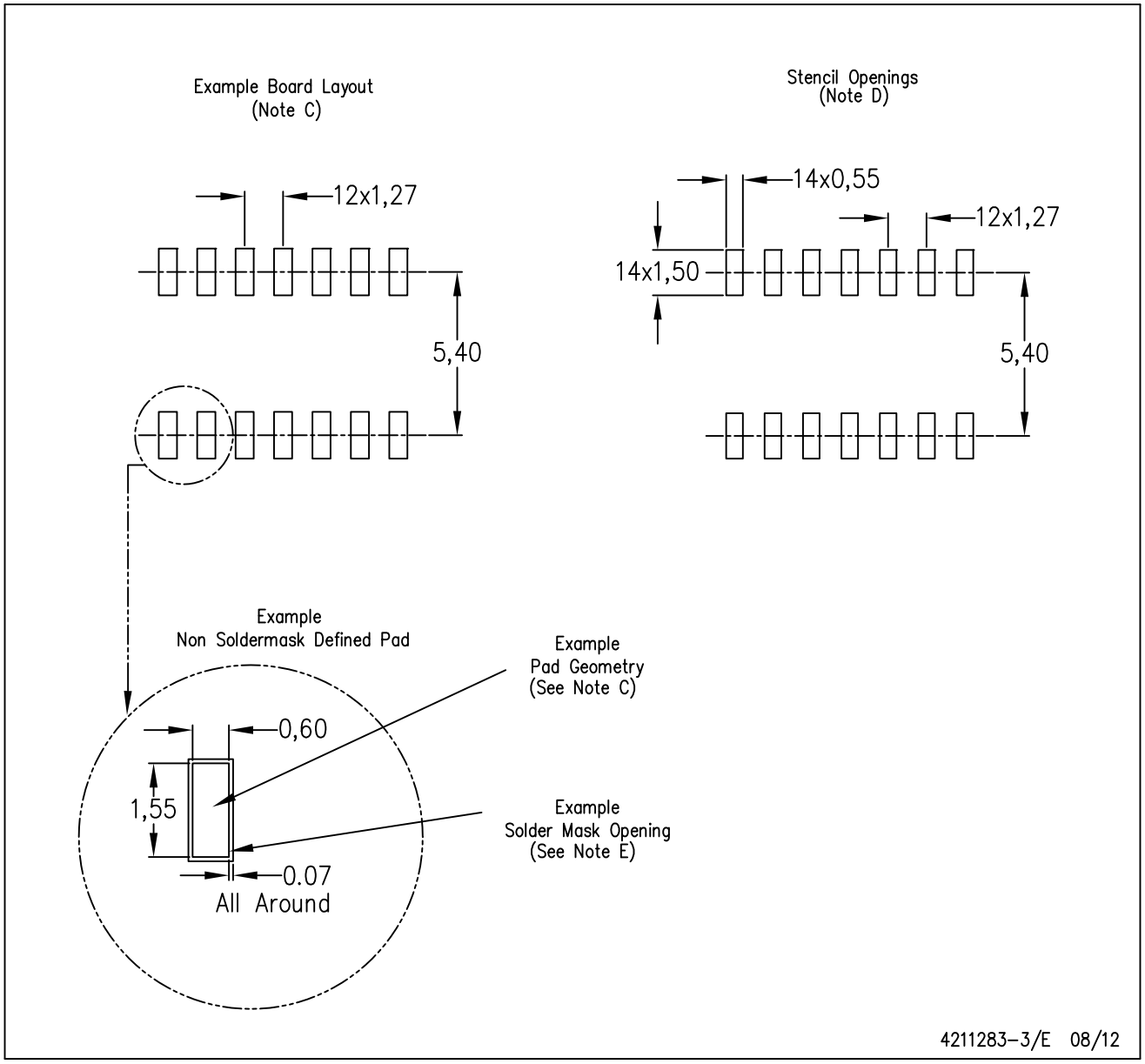
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

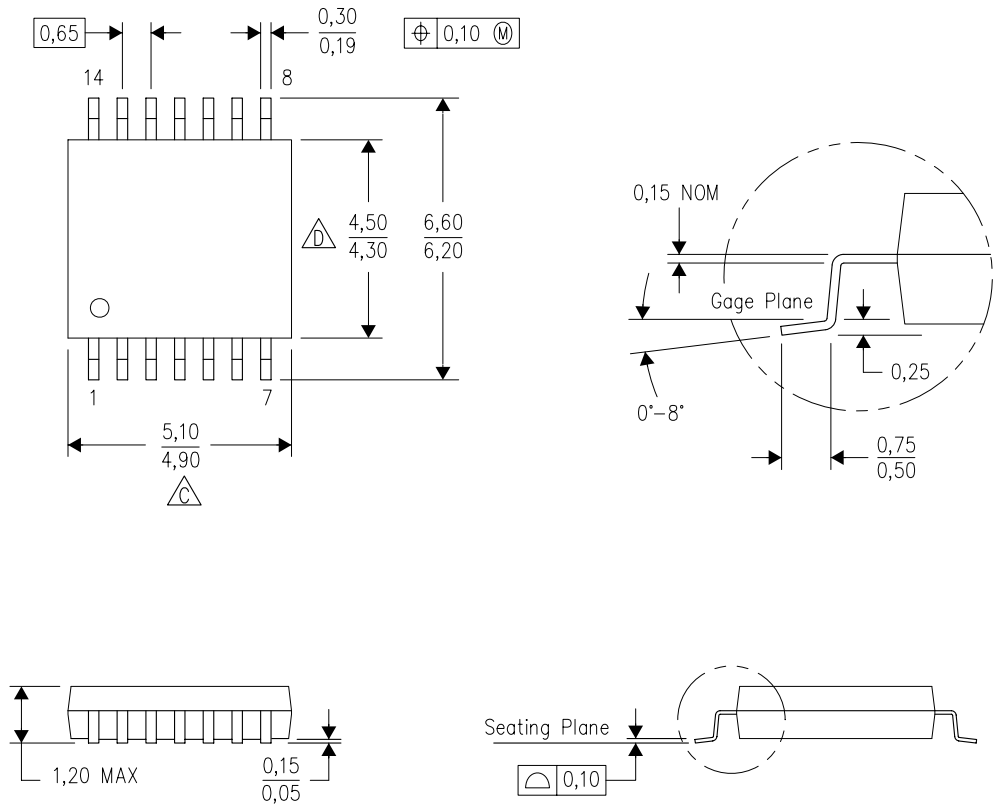
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

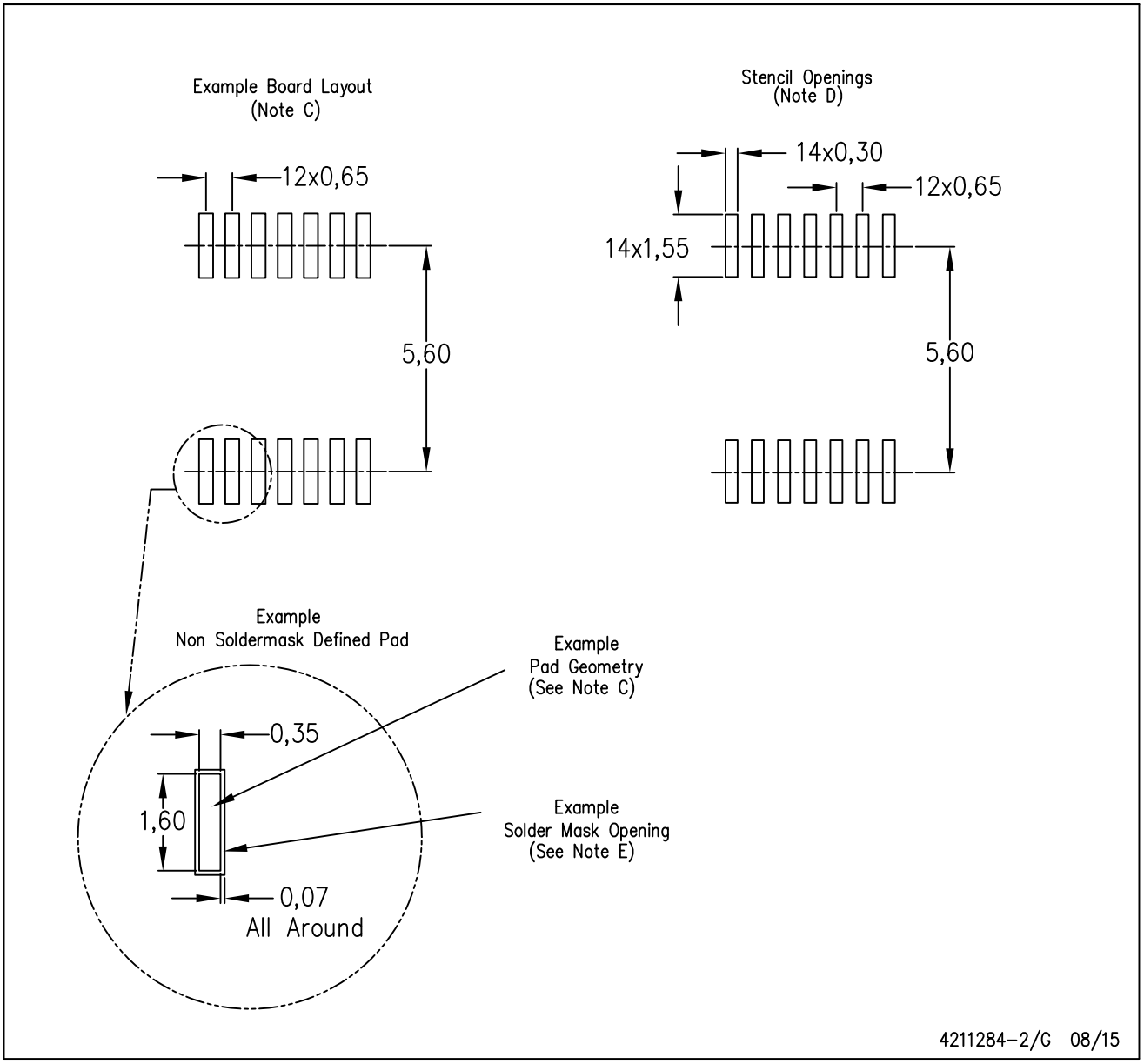
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

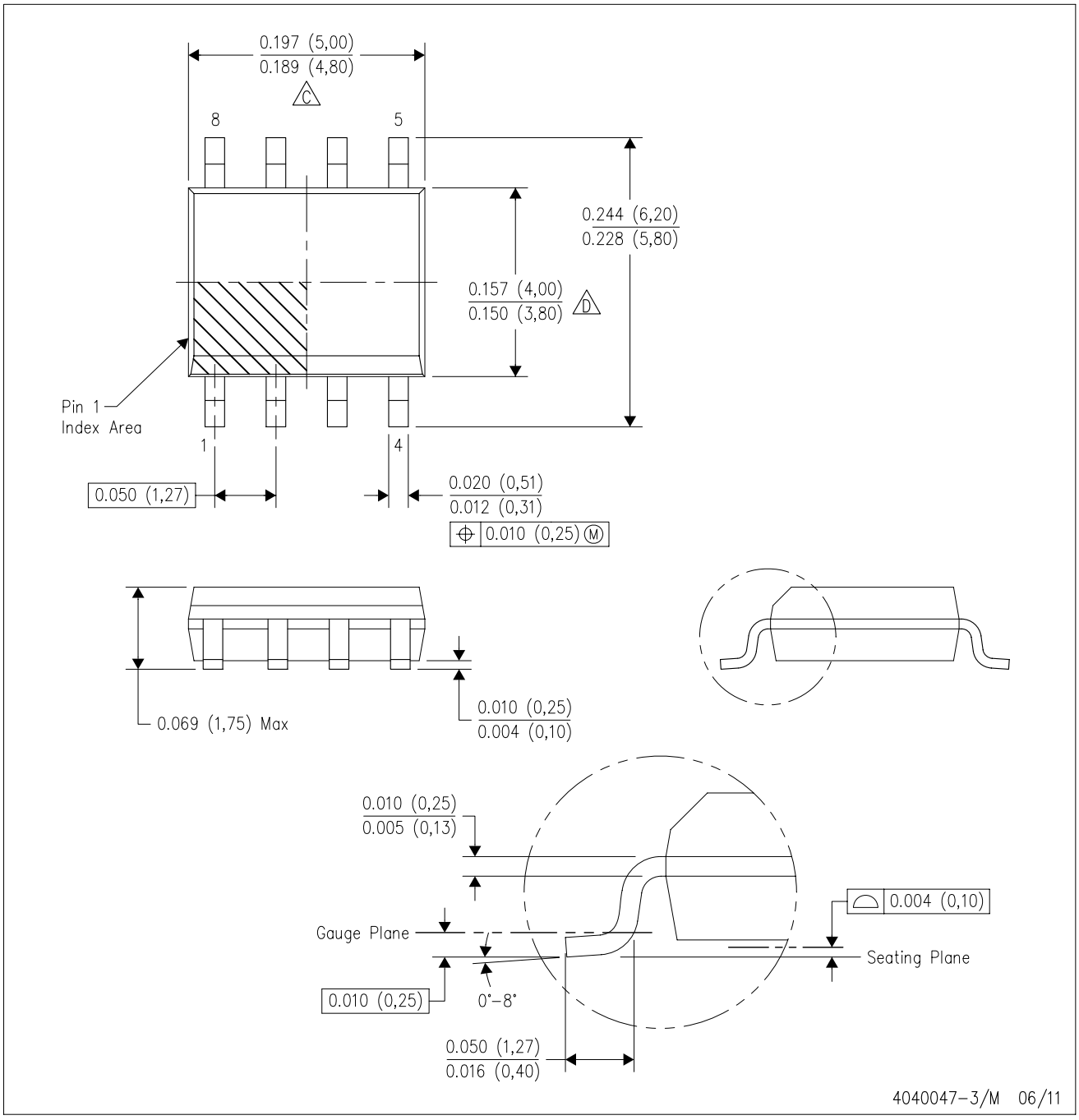
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



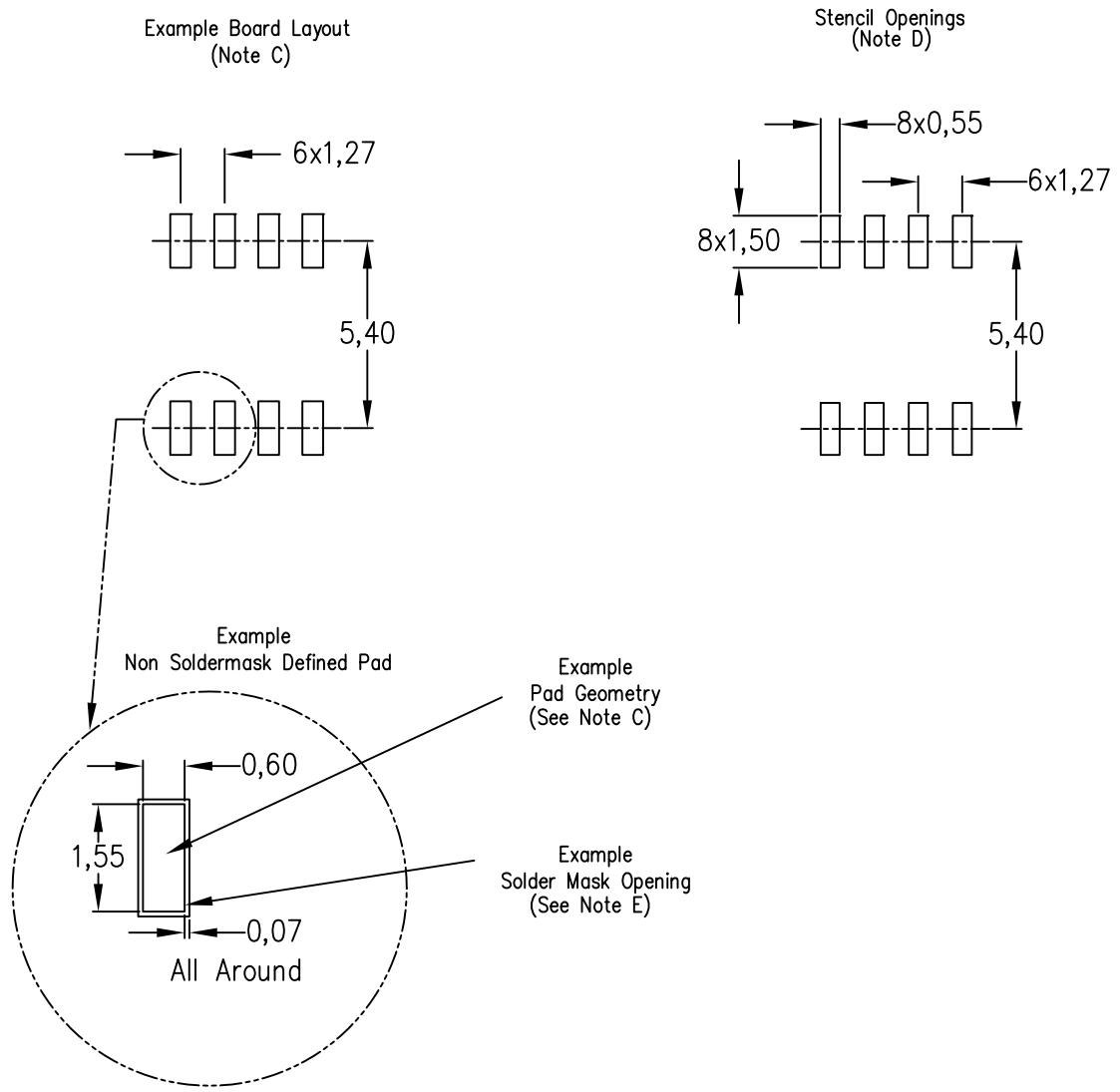

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265