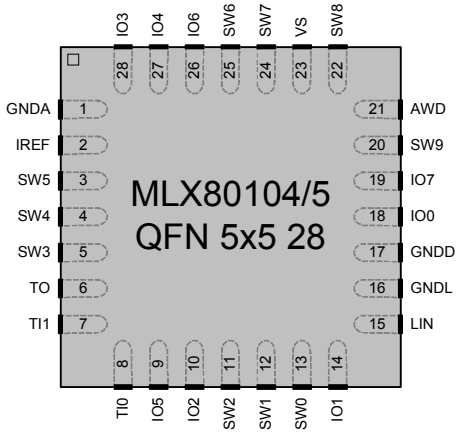
MLX80104/5

LIN Slave for Switches/LIN IO Extension

Features



Application Controller

- Internal 12 MHz RC-Oscillator
- 16-bit MULAN MCU with 16kB ROM or OTP, 512 Byte RAM, 192 Byte EEPROM with ECC

LIN Protocol Controller according to LIN 2.x and SAE J2602

- Baud rate up to 19.2 kBaud
- Frame processing
- Low interrupt load to the application

LIN Transceiver according to LIN 2.x and SAE J2602

- Slew rate control for best EME behaviour
- High EMI immunity

IO Configuration

- 18 fully configurable high current/high voltage inputs/outputs (7mA/26.5V)
- Ground shift tolerant I/Os
- All IOs configurable pull up or pull down characteristics
- Eight PWM outputs (8-bit, 80Hz to 30kHz)
- Ten 10-bit ADC channels
- Eight Interrupt capable Inputs
- Configurable Wake up sources (LIN, IOs, ADC)
- Constant current output (2mA) for external low voltage loads via bipolar transistor
- IOs fully diagnosable
- Integrated window watchdog and additional independent analogue watchdog

Voltage Regulator

- Low standby current consumption of typ 25µA in sleep mode
- Over-temperature shutdown, 45V load dump protected

Other Features

- Automotive Temperature Range of –40°C to 125°C
- Small MLF 5x5 28pin package
- Ready-to-use firmware available (UniROM)

Order Code	*Temp. Range*	*Package*	*Delivery*	*Remark*
MLX80104 KLQ-DAF-000-RE	-40 - 125 °C	QFN 5x5	Reel	ROM
MLX80105 KLQ-DAA-000-RE	-40 - 125 °C	QFN 5x5	Reel	OTP

Short Description

This IC is a fully integrated LIN Slave for matrix switch or single switch Applications in automotive environment. It is suitable for bus systems according to LIN 2.x as well as SAE J2602.
The combination of physical layer LIN transceiver and LIN protocol controller along with easy to configure switch inputs and PWM outputs make it possible to develop in a short timeframe simple, but powerful and cheap switch slave nodes for LIN Bus systems.

Contents

1. General Overview

1.1 MLX80104 Block Diagram

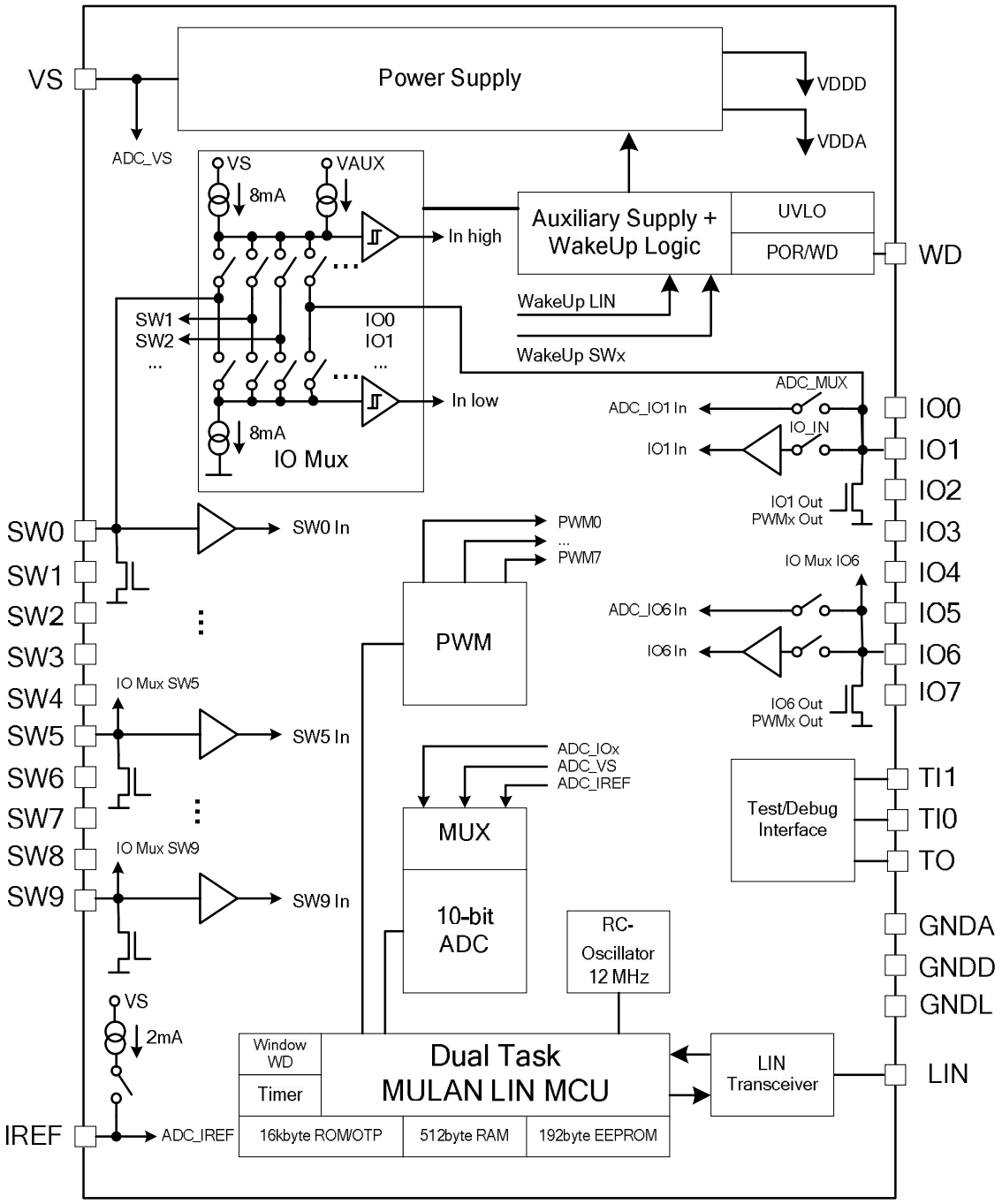


Figure 1 - MLX80104 Block Diagram

2. Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC.

2.1 Absolute Maximum Ratings

In accordance with the Maximum Rating System (IEC 60134). The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S		-0.3	40	V
Short term supply voltage	V_{S_ld}	ISO 7637/2 pulse 5; t < 400 ms	-0.3	40	V
Transients at supply voltage	V_{S_tr1}	ISO 7637/2 pulse 1[1]	-100		V
Transients at supply voltage	V_{S_tr2}	ISO 7637/2 pulses 2 [1]		+50	V
Transients at high voltage signal pins	V_{LINx_tr1}	ISO 7637/3 pulse 1 [2]	-100		V
Transients at high voltage signal pins	V_{LINx_tr2}	ISO 7637/3 pulses 2 [2]		+50	V
Transient at high voltage signal and power supply pins	V_{HV_tr3}	ISO 7637/2 pulses 3A, 3B [3]	-150	+100	V
DC voltage on LIN, SWx, IOx pins	V_{LIN_DC}	T<500ms, V_S = 18V V_S = 0V	-22 -40	40	V
DC voltage on IREF, AWD pin	V_{logic_DC}		-0.3	7	V
ESD capability	V_{ESDIEC}	IEC 61000-4-2 Pin LIN, VS to GND	-6	6	kV
	V_{ESDHBM}	HBM (AEC-Q100-002) [4] Pin LIN, VS to GND Other pins	 -8 -2	 8 2	 kV kV
	V_{ESDCDM}	CDM (AEC-Q100-011)	-750	750	V
Maximum latch – up free current at any pin	I_{LATCH}		-500	500	mA
Maximum power dissipation	P_{tot}	T_{amb} = +125 °C		0.78	W
		T_{amb} = + 85 °C		2	
Thermal impedance	Θ_{JA}	JEDEC 1s2p board, none air flow		32	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

Table 1 - Absolute Maximum Ratings

[1] ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[2] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 100nF.
[3] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 1nF.
ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[4] Equivalent to discharging a 100pF capacitor through a 1.5Kohm resistor conforms to AEC-Q100-002

2.2 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	5	27	V
Operating ambient temperature	T_{amb}	-40	+125	°C

Table 2 - Operating Conditions

[1] V_s is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4…1V, V_{BAT_ECU} = 6…27V.

3. IO Ports

The MLX80104/5 contains two types of ports. All of them are proof to battery voltage.
In case of ECU loss of battery (LOB) and a short of the wiring harness to an external supply line the MLX80104/5 will be reverse powered.

3.1 Common Features of Pin SWx and IOx

The ports *SW0..9* as well as the ports *IO0..7* allow a very flexible control of up to 18 single switches or a switch matrix or any combination of both, supplied by an internal current source of typically >7mA. The switch control is sequential and periodical, so that only one port will be supplied at the same time.
If switches are placed outside and connected via a wiring harness to the ECU the MLX80104/5 allows full diagnosis of short circuits or broken line.
All ports provide a programmable wake up function and a 10mA open drain low side switch (matrix row connection to GND).
If ports are not used for switch detection, they can be configured passive (tristate behaviour) or as general purpose 10mA open drain output with port monitor. The input thresholds are compatible to 3.3V/5V supply systems. The accuracy of the input threshold allows a monitoring of external voltages without ADC. It allows connection of external supplied encoders, halls or similar.
Furthermore this architecture supports driving of logic output signals for other ECU components via an external pull up resistor as well as the driving of high side or low side loads by providing base current for an external pnp transistor.

3.1.1. Pin structure

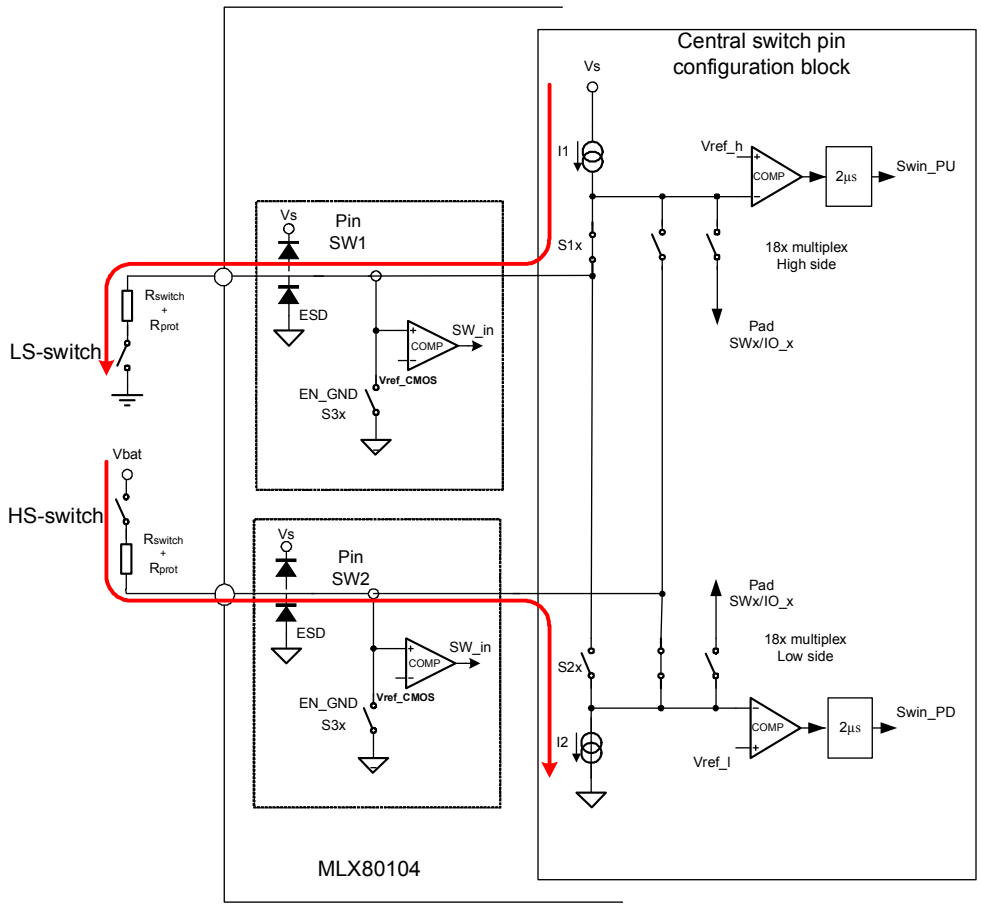


Figure 2 - Common pin Structure SWx and IOx

Figure 2 illustrates the basic structure and control of the ports for switch detection.

The default configuration of all ports after power on or wake up is tristate. After the initialisation procedure the ports will be configured by the MCU. The pull up or pull down current is provided by two central current sources I1 and I2. The currents for switch control have to be applied sequentially by the multiplex switches S1x or S2x. If a low impedance path to Ground is required (open drain buffer or matrix mode row connection), the local switch S3x has to be used.
Because of the multiplex principle only two comparators are required to detect the port input voltage levels. For RF interference as well as suppression of automotive disturbances the comparator path contains a debounce filter of typically 2µs.

The multiplex switches S1, S2 as well as the local open drain buffer S3 are controlled by the registers S3H and S3L.

3.2 Additional Operation Modes SWx Ports

Open drain output mode
The SWx pins can also be used as normal open drain outputs. This mode can be switched on via the configuration register bits. In this mode the central current source (S1x and S3x) should not be applied to the open drain configured pin.
Because of the high voltage capability of the pin the current capability can be easy extended via an external pnp-transistor.

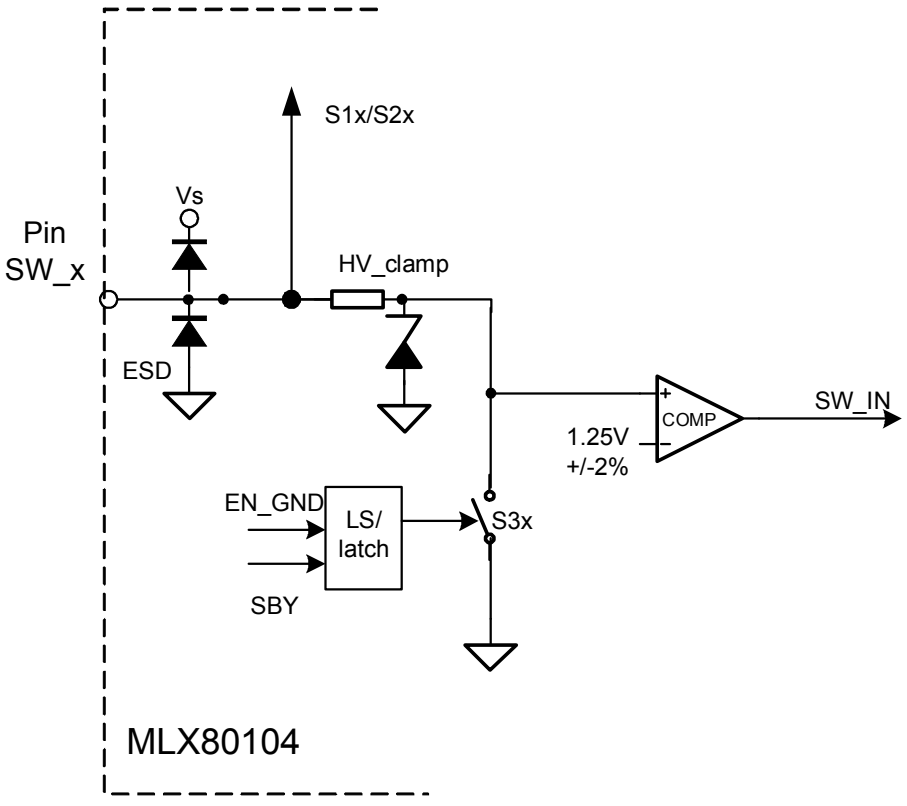


Figure 3 - Structure of SWx pins

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ADC input mode
Every IOx pin can also be used as analogue input signal for the integrated 10-bit ADC. Via the ADC_CTL register the IOx pins can be selected to be used as ADC channel.

Interrupt capable input
In case external events should generate an interrupt the IOx pins can also be configured as an interrupt source. The interrupt sensitivity can be configured either for the falling or for the rising or for both edges.

PWM Output
The eight available PWM channels can be applied to the corresponding IOx pin via the register PWM_AD. For output of the PWM channels the pin must be configured in open drain configuration.

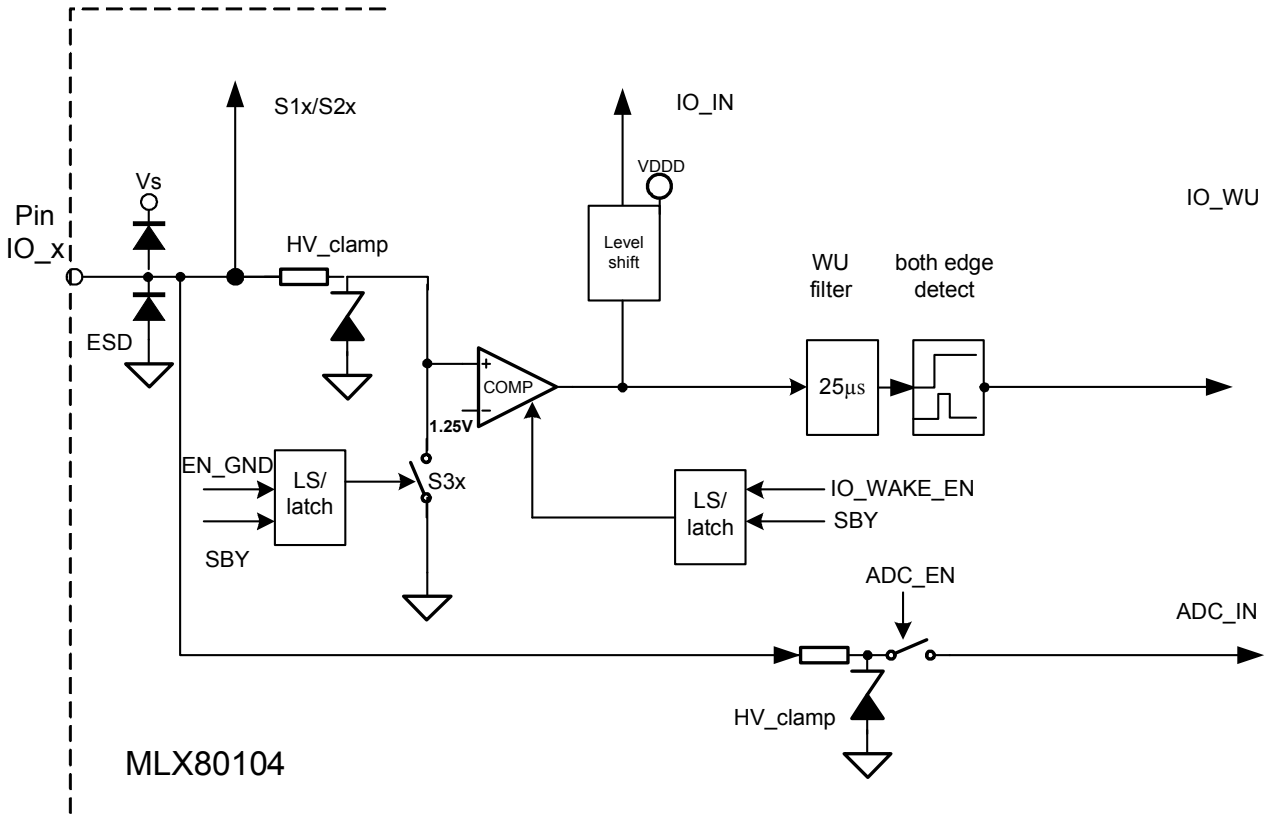

Figure 4 - Structure of IOx pins

3.4 The IREF pin

This pin provides a calibrated pull up current from the VS supply. This output current can be used for generation of an external reference or supply voltage by using an external bipolar transistor.

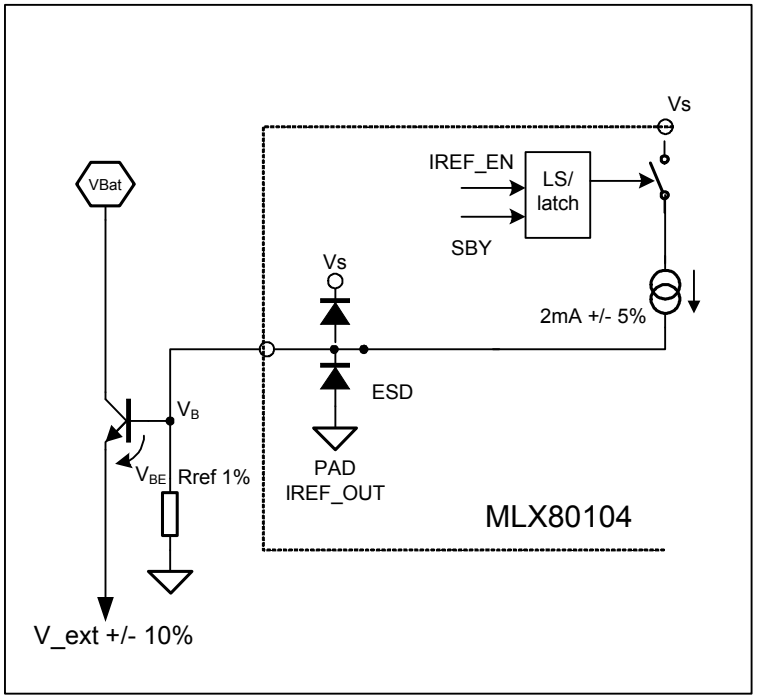

Figure 5 - Sample circuitry for IREF pin

For increasing the accuracy of the V_ext voltage at higher loads a zener diode can be placed at the base of the transistor. $V\_ext = V_B - V_{BE}$

Via the central current source diagnose register the IREF current can be switched on/off.

The voltage at this pin can be monitored via the internal ADC channel IREF

4. Application Hints

Further information regarding the use of the IO and SW pins can be found in the Application note “Standard input/output pin configurations”.

4.1 Application Examples

The SWx are used for connection to a switch matrix as well as for single switches to GND or VS
The IOx pins can be used for different purposes:

1. Single switch input connected to GND or VS
2. Rotating encoder input
3. General purpose digital input
4. Open drain high voltage capable output
5. ADC Input

The pin IREF, via an external bipolar transistor, is used to generate a 5V voltage to supply external pull up resistors.

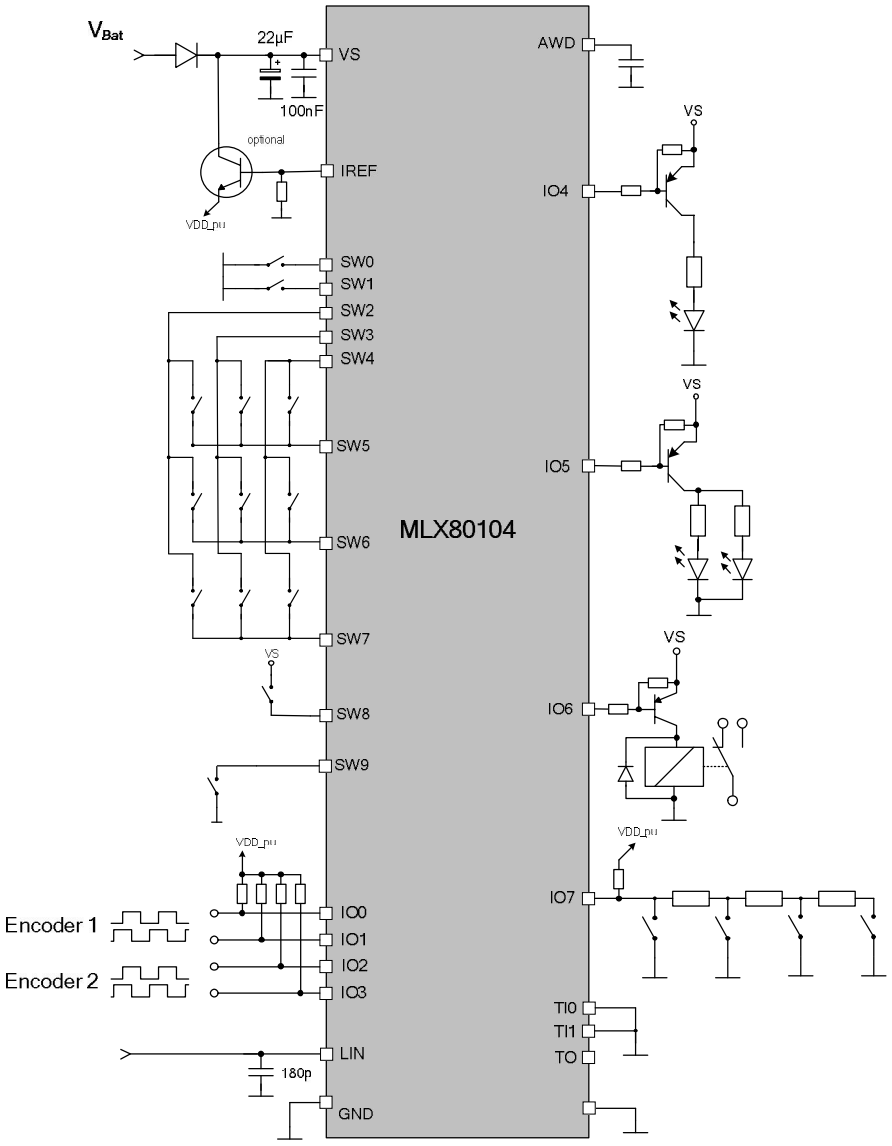

Figure 6 - Application schematic sample

5. Pin Description

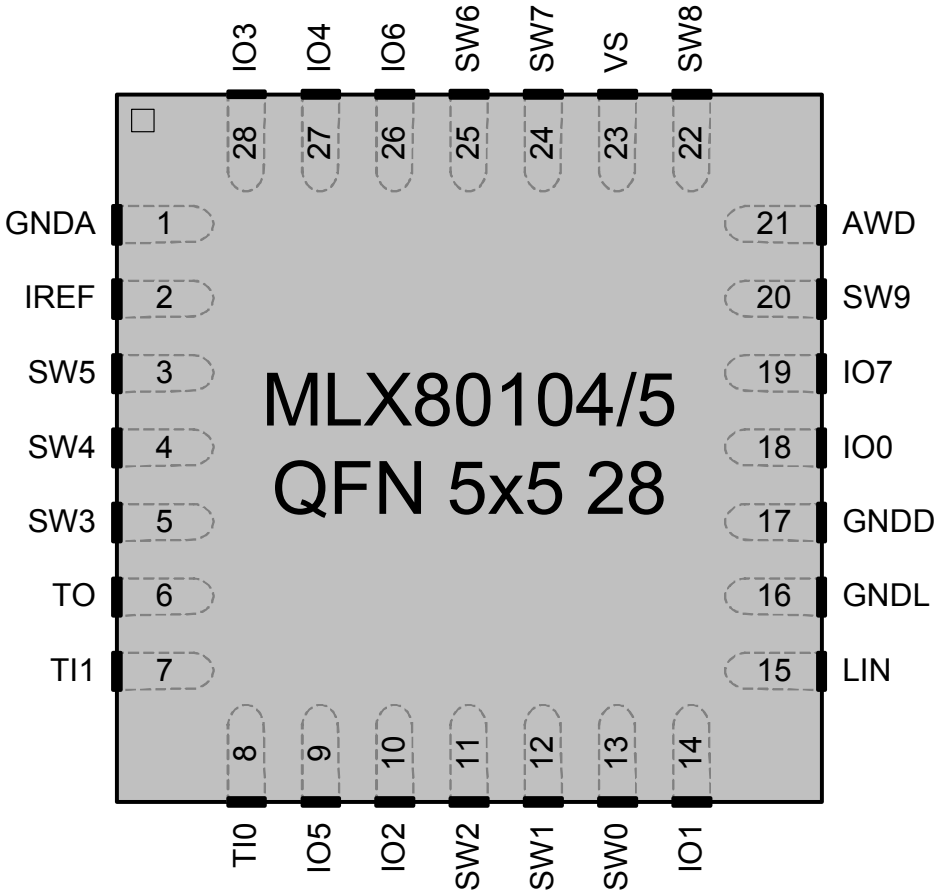

Figure 7 - Pin out MLX80104/5 – Top view

Table 1 – Pin Description MLX80104 QFN 5x5 28

Pin No	Name	Function	I/O Type
1	GNDA	Analogue ground and ADC ground	GND
2	IREF	IREF output	O
3	SW5	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
4	SW4	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
5	SW3	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
6	TO	Test output, unconnected in application mode	O
7	TI1	Test input - connect to GND in application mode	I
8	TI0	Test input - connect to GND in application mode	I
9	IO5	SWx functionality and ADC input, wake up capable, PWM output	I/O
10	IO2	SWx functionality and ADC input, wake up capable, PWM output	I/O
11	SW2	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
12	SW1	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
13	SW0	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
14	IO1	SWx functionality and ADC input, wake up capable, PWM output	I/O
15	LIN	Connection to LIN bus	IO
16	GNDL	LIN driver ground	GND
17	GNDD	Digital ground	GND
18	IO0	SWx functionality and ADC input, wake up capable, PWM output	I/O
19	IO7	SWx functionality and ADC input, wake up capable, PWM output	I/O
20	SW9	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
21	AWD	Watch dog load capacitor	I/O
22	SW8	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
23	VS	High voltage supply, battery voltage	P
24	SW7	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
25	SW6	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
26	IO6	SWx functionality and ADC input, wake up capable, PWM output	I/O
27	IO4	SWx functionality and ADC input, wake up capable, PWM output	I/O
28	IO3	SWx functionality and ADC input, wake up capable, PWM output	I/O

6. Mechanical Specification

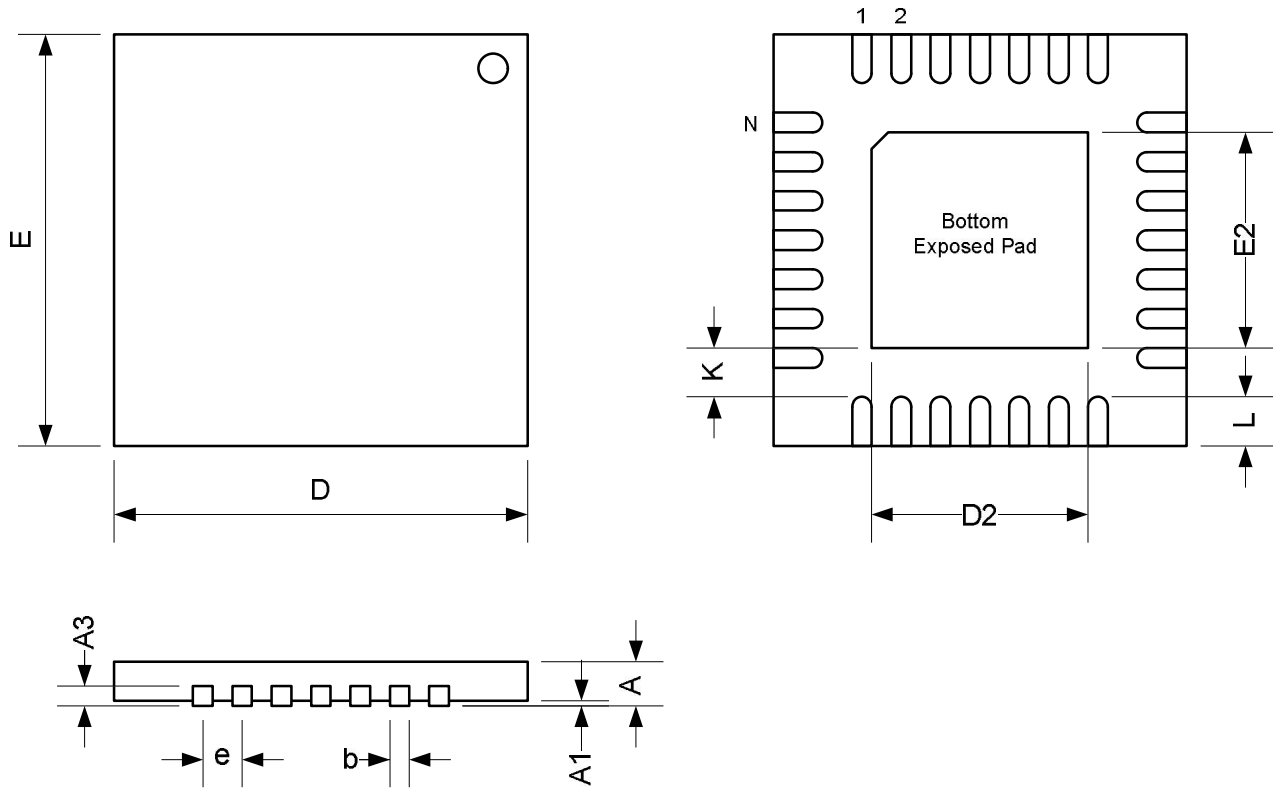

Figure 8 – QFN Drawing

Table 2 – QFN28 Package Dimensions

Symbol		A	A1	A3	b	D	D2	E	E2	e	K	L	N [6][3]	ND [5]	NE [5]	
QFN28	min	0.80	0	0.20	0.18	5.00	3.00	5.00	3.00	0.5	0.20	0.55	28	7	7	[1] [2]
	nom	0.90	0.02		0.25		3.10		3.10			0.60				
	max	1.00	0.05		0.30		3.25		3.25			0.65				

[1] Dimensions and tolerances conform to ASME Y14.5M-1994
[2] All dimensions are in Millimeters. All angels are in degrees
[3] N is the total number of terminals
[4] Dimension b applies to metalized terminal and is measured between 0.25 and 0.30mm from terminal tip
[5] ND and NE refer to the number of terminals on each D and E side respectively
[6] Depopulation is possible in a symmetrical fashion

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Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

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