# EFR32MG14 Mighty Gecko Multi-Protocol Wireless SoC Family Data Sheet

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The Mighty Gecko multi-protocol family of SoCs is part of the Wireless Gecko portfolio. Mighty Gecko SoCs are ideal for enabling energy-friendly multi-protocol, multi-band networking for IoT devices.

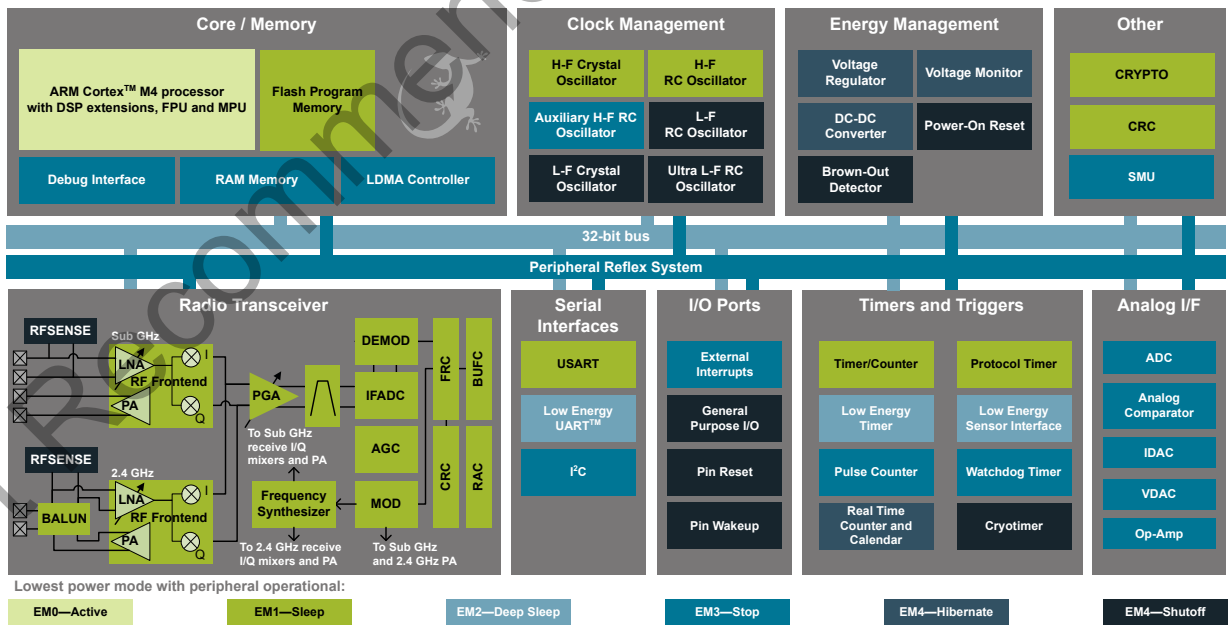
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, and no-compromise MCU features.

Mighty Gecko applications include:

- IoT Multi-Protocol Devices
- Connected Home
- Lighting
- Health and Wellness
- Metering
- Home and Building Automation and Security

**KEY FEATURES**

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- 256 kB of flash and 32 kB of RAM
- Pin-compatible across EFR32MG families (exceptions apply for 5V-tolerant pins)
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator
- Integrated PA with up to 19 dBm (2.4 GHz) or 20 dBm (Sub-GHz) tx power
- Integrated balun for 2.4 GHz
- Robust peripheral set and up to 32 GPIO



# 1. Feature List

The EFR32MG14 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - 256 kB flash program memory
  - 32 kB RAM data memory
  - 2.4 GHz and Sub-GHz radio operation
  - Transmit power:
    - 2.4 GHz radio: Up to 19 dBm
    - Sub-GHz radio: Up to 20 dBm
- **Low Energy Consumption**
  - 10.2 mA RX current at 250 kbps, DSSS-OQPSK, 2.4 GHz
  - 8.8 mA RX current at 1 Mbps, GFSK, 2.4 GHz
  - 8.4 mA RX current at 38.4 kbps, GFSK, 169 MHz
  - 8.5 mA TX current at 0 dBm output power at 2.4 GHz
  - 35.3 mA TX current at 14 dBm output power at 868 MHz
  - 67 µA/MHz in Active Mode (EM0)
  - 1.3 µA EM2 DeepSleep current (16 kB RAM retention and RTCC running from LFRCO)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -93.8 dBm sensitivity at 1 Mbit/s GFSK, 2.4 GHz
  - -103.3 dBm sensitivity at 250 kbps DSSS-OQPSK, 2.4 GHz
  - -126.2 dBm sensitivity at 600 bps, GFSK, 915 MHz
  - -120.6 dBm sensitivity at 2.4 kbps, GFSK, 868 MHz
  - -109.9 dBm sensitivity at 4.8 kbps, OOK, 433 MHz
  - -112.2 dBm sensitivity at 38.4 kbps, GFSK, 169 MHz
- **Supported Modulation Formats**
  - 2/4 (G)FSK with fully configurable shaping
  - BPSK / DBPSK TX
  - OOK / ASK
  - Shaped OQPSK / (G)MSK
  - Configurable DSSS and FEC
- **Supported Protocols**
  - Zigbee
  - Thread
  - Bluetooth® Low Energy (Bluetooth 5)
  - Proprietary Protocols
  - Wireless M-Bus
  - Selected IEEE 802.15.4g SUN-FSK PHYs
  - Low Power Wide Area Networks
- **Suitable for Systems Targeting Compliance With:**
  - FCC Part 90.210 Mask D, FCC part 15.247, 15.231, 15.249
  - ETSI Category I Operation, EN 300 220, EN 300 328
  - ARIB T-108, T-96
  - China regulatory
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - 2 × Operational Amplifier (Opamp)
  - Digital to Analog Current Converter (IDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Up to 32 pins connected to analog channels (APORT) shared between analog peripherals
  - Up to 32 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 × 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - 2 × Watchdog Timer with dedicated RC oscillator
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/$I^2S$)
  - Low Energy UART (LEUART™)
  - $I^2C$ interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C) and Extended (-40 °C to 125 °C) temperature grades available
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **QFN32 5x5 mm Package**
- **QFN48 7x7 mm Package**

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## 2. Ordering Information

**Table 2.1. Ordering Information**

| Ordering Code | Protocol Stack | Frequency Band @ Max TX Power | Flash (kB) | RAM (kB) | GPIO | Package | Temp Range |
|---|---|---|---|---|---|---|---|
| EFR32MG14P733F256GM48-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | • 2.4 GHz @ 19 dBm<br>• Sub-GHz @ 20 dBm | 256 | 32 | 28 | QFN48 | -40 to +85°C |
| EFR32MG14P733F256IM48-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | • 2.4 GHz @ 19 dBm<br>• Sub-GHz @ 20 dBm | 256 | 32 | 28 | QFN48 | -40 to +125°C |
| EFR32MG14P732F256GM48-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 19 dBm | 256 | 32 | 31 | QFN48 | -40 to +85°C |
| EFR32MG14P732F256IM48-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 19 dBm | 256 | 32 | 31 | QFN48 | -40 to +125°C |
| EFR32MG14P732F256GM32-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 19 dBm | 256 | 32 | 16 | QFN32 | -40 to +85°C |
| EFR32MG14P732F256IM32-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 19 dBm | 256 | 32 | 16 | QFN32 | -40 to +125°C |

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| Ordering Code | Protocol Stack | Frequency Band @ Max TX Power | Flash (kB) | RAM (kB) | GPIO | Package | Temp Range |
|---|---|---|---|---|---|---|---|
| EFR32MG14P731F256GM48-B | • Zigbee<br>• Proprietary<br>• Multiproto-col | Sub-GHz @ 20 dBm | 256 | 32 | 32 | QFN48 | -40 to +85°C |
| EFR32MG14P632F256GM48-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 10 dBm | 256 | 32 | 31 | QFN48 | -40 to +85°C |
| EFR32MG14P632F256GM32-B | • Bluetooth Low Energy<br>• Zigbee<br>• Thread<br>• Proprietary<br>• Multiproto-col | 2.4 GHz @ 10 dBm | 256 | 32 | 16 | QFN32 | -40 to +85°C |

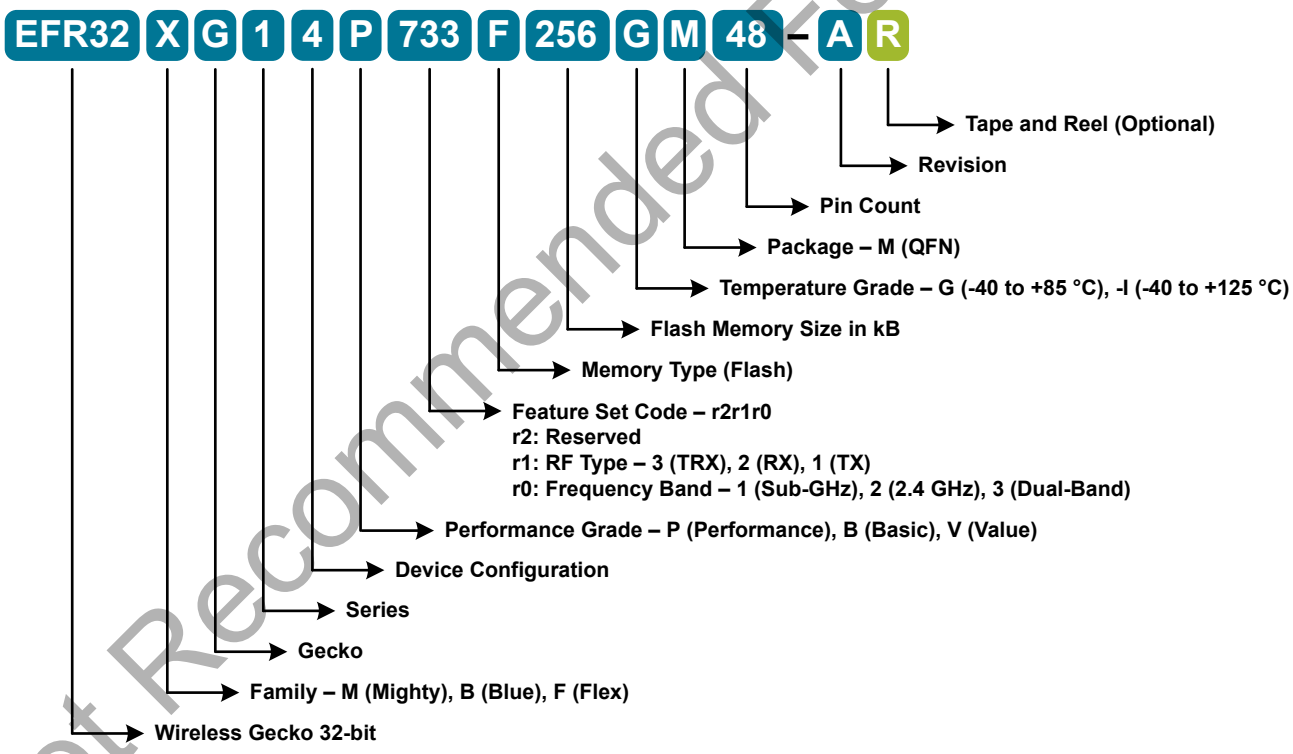


**Figure 2.1. Ordering Code Key**

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# 3. System Overview

## 3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG14 Wireless Gecko Reference Manual.

A block diagram of the EFR32MG14 family is shown in Figure 3.1 Detailed EFR32MG14 Block Diagram on page 8. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

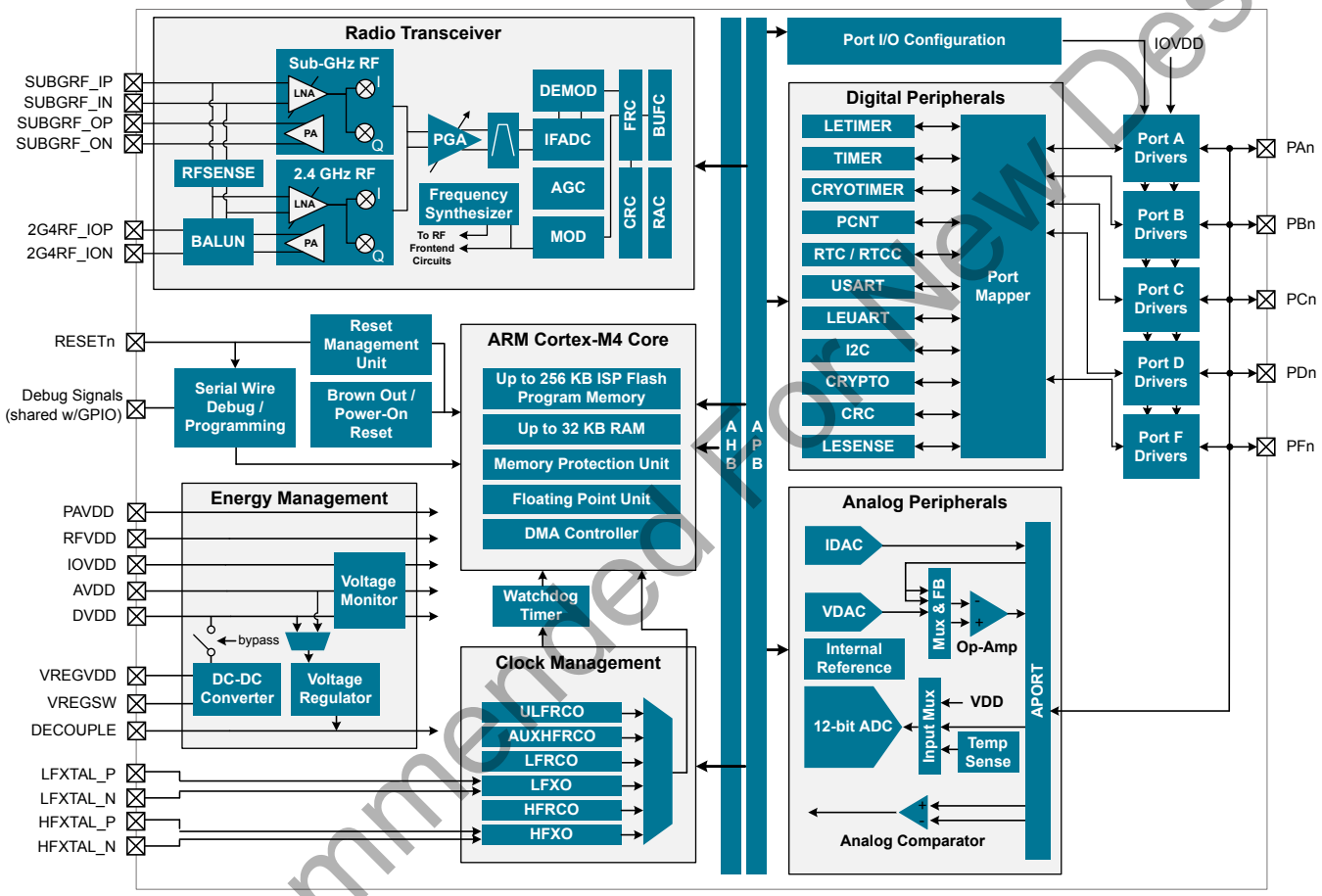


**Figure 3.1. Detailed EFR32MG14 Block Diagram**

## 3.2 Radio

The Mighty Gecko family features a highly configurable radio transceiver supporting a wide range of wireless protocols.

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### 3.2.1 Antenna Interface

The EFR32MG14 family includes devices which support both single-band and dual-band RF communication over separate physical RF interfaces.

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The sub-GHz antenna interface consists of a differential transmit interface (pins SUBGRF_OP and SUBGRF_ON) and a differential receive interface (pinsSUBGRF_IP and SUBGRF_IN).

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

### 3.2.2 Fractional-N Frequency Synthesizer

The EFR32MG14 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

### 3.2.3 Receiver Architecture

The EFR32MG14 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS) for 2.4 GHz and sub-GHz bands.

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32MG14 features integrated support for antenna diversity to mitigate the problem of frequency-selective fading due to multipath propagation and improve link budget. Support for antenna diversity is available for specific PHY configurations in 2.4 GHz and sub-GHz bands. Internal configurable hardware controls an external switch for automatic switching between antennae during RF receive detection operations.

**Note:** Due to the shorter preamble of 802.15.4 and BLE packets, RX diversity is not supported.

### 3.2.4 Transmitter Architecture

The EFR32MG14 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MG14. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

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### 3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32MG14 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

### 3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

### 3.2.7 Flexible Frame Handling

EFR32MG14 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

### 3.2.8 Packet and State Trace

The EFR32MG14 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

### 3.2.9 Data Buffering

The EFR32MG14 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

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### 3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32MG14. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

### 3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

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### 3.3 Power

The EFR32MG14 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32MG14 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

#### 3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

#### 3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

#### 3.3.3 Power Domains

The EFR32MG14 has two peripheral power domains for operation in EM2 and EM3. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

**Table 3.1. Peripheral Power Subdomains**

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---|---|
| ACMP0 | ACMP1 |
| PCNT0 | CSEN |
| ADC0 | VDAC0 |
| LETIMER0 | LEUART0 |
| LESENSE | I2C0 |
| APORT | IDAC |

### 3.4 General Purpose Input/Output (GPIO)

EFR32MG14 has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

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## 3.5 Clocking

### 3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32MG14. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

### 3.5.2 Internal and External Oscillators

The EFR32MG14 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

## 3.6 Counters/Timers and PWM

### 3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

### 3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

### 3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

Not Recommended For New Designs

### 3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

### 3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.7 Communications and Other Digital Peripherals

### 3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- $I^2S$

### 3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.7.3 Inter-Integrated Circuit Interface ($I^2C$)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$ bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the $I^2C$ module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

Not Recommended For New Designs

### 3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

## 3.8 Security Features

### 3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF($2^m$), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

### 3.8.3 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

## 3.9 Analog

### 3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

Not Recommended For New Designs

### 3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

### 3.9.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

### 3.9.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

## 3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MG14. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

## 3.11 Core and Memory

### 3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

### 3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

Not Recommended For New Designs

### 3.12 Memory Map

The EFR32MG14 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

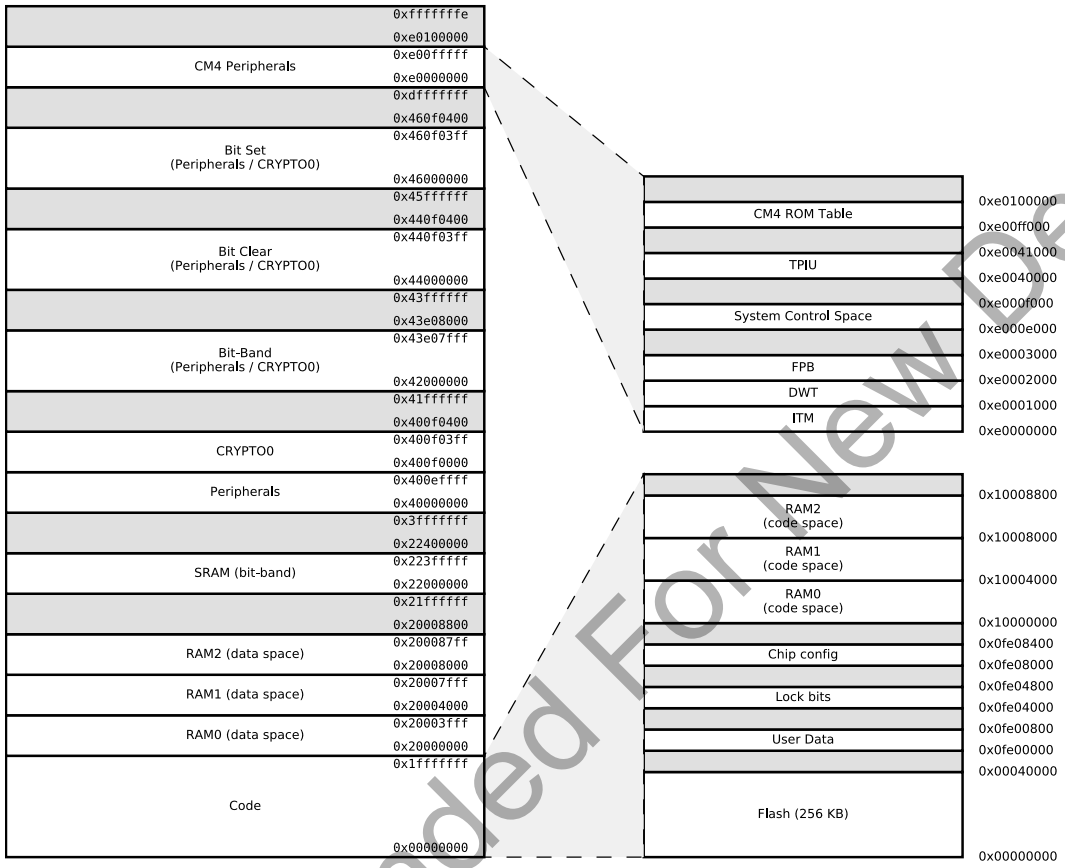


**Figure 3.2. EFR32MG14 Memory Map — Core Peripherals and Code Space**

Not Recommended For New Designs

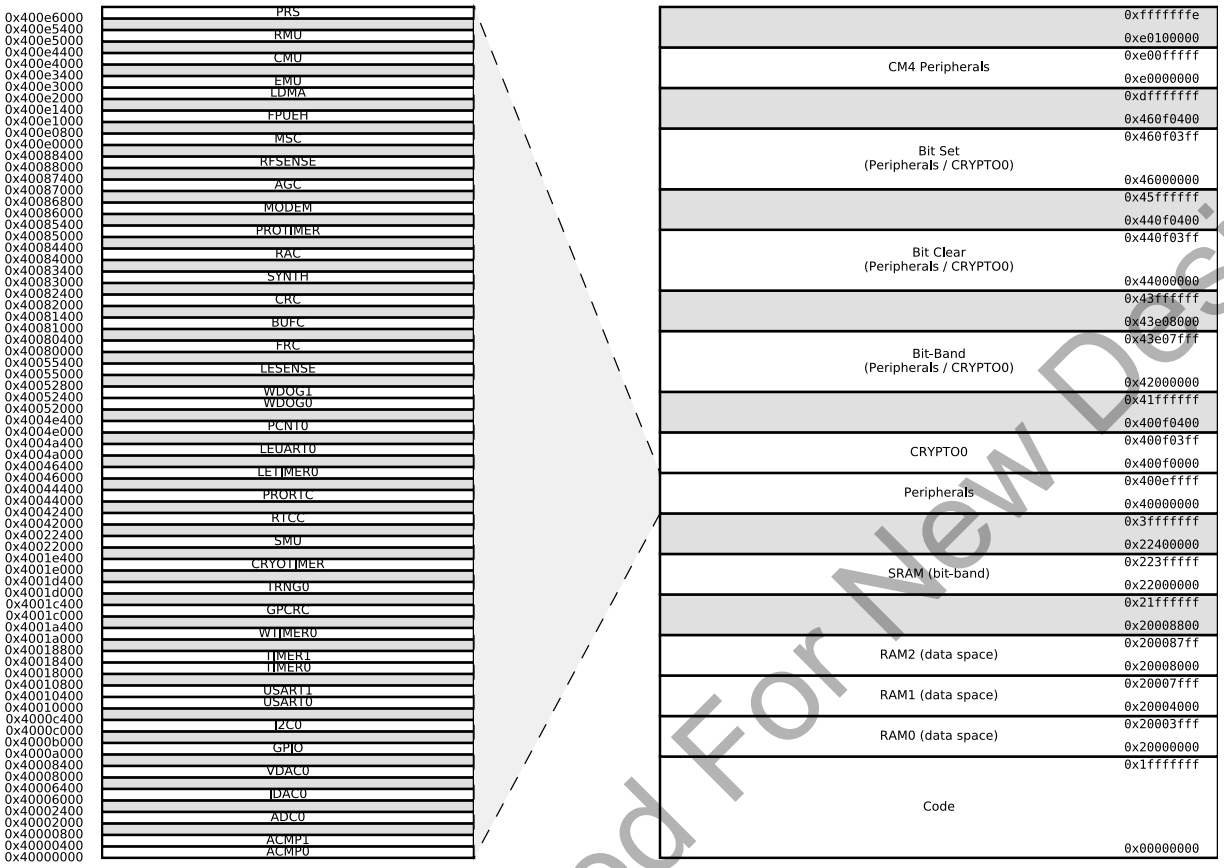


**Figure 3.3. EFR32MG14 Memory Map — Peripherals**

### 3.13 Configuration Summary

The features of the EFR32MG14 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

**Table 3.2. Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| USART0 | IrDA<br>SmartCard | US0_TX, US0_RX, US0_CLK, US0_CS |
| USART1 | I²S<br>SmartCard | US1_TX, US1_RX, US1_CLK, US1_CS |
| TIMER0 | with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | - | TIM1_CC[3:0] |
| WTIMER0 | with DTI | WTIM0_CC[2:0], WTIM0_CDTI[2:0] |

Not Recommended For New Designs

# 4. Electrical Specifications

## 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}$=25 °C and $V_{DD}$= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω source or load.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

Not Recommended For New Designs

### 4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 4.1. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -50 | — | 150 | °C |
| Voltage on any supply pin | $V_{DDMAX}$ | | -0.3 | — | 3.8 | V |
| Voltage ramp rate on any supply pin | $V_{DDRAMPMAX}$ | | — | — | 1 | V / µs |
| DC voltage on any GPIO pin | $V_{DIGPIN}$ | 5V tolerant GPIO pins[1] [2] [3] | -0.3 | — | Min of 5.25 and IOVDD +2 | V |
| | | Standard GPIO pins | -0.3 | — | IOVDD+0.3 | V |
| Voltage on HFXO pins | $V_{HFXOPIN}$ | | -0.3 | — | 1.4 | V |
| Input RF level on pins 2G4RF_IOP and 2G4RF_ION | $P_{RFMAX2G4}$ | | — | — | 10 | dBm |
| Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION) | $V_{MAXDIFF2G4}$ | | -50 | — | 50 | mV |
| Absolute voltage on RF pins 2G4RF_IOP and 2G4RF_ION | $V_{MAX2G4}$ | | -0.3 | — | 3.3 | V |
| Absolute voltage on Sub-GHz RF pins | $V_{MAXSUBG}$ | Pins SUBGRF_OP and SUBGRF_ON | -0.3 | — | 3.3 | V |
| | | Pins SUBGRF_IP and SUBGRF_IN, | -0.3 | — | 0.3 | V |
| Total current into VDD power lines | $I_{VDDMAX}$ | Source | — | — | 200 | mA |
| Total current into VSS ground lines | $I_{VSSMAX}$ | Sink | — | — | 200 | mA |
| Current per I/O pin | $I_{IOMAX}$ | Sink | — | — | 50 | mA |
| | | Source | — | — | 50 | mA |
| Current for all I/O pins | $I_{IOALLMAX}$ | Sink | — | — | 200 | mA |
| | | Source | — | — | 200 | mA |
| Junction temperature | $T_J$ | -G grade devices | -40 | — | 105 | °C |
| | | -I grade devices | -40 | — | 125 | °C |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

Not Recommended For New Designs

### 4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD, RFVDD, PAVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

Not Recommended For New Designs

#### 4.1.2.1 General Operating Conditions

**Table 4.2. General Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating ambient temperature range[5] | $T_A$ | -G temperature grade | -40 | 25 | 85 | °C |
| | | -I temperature grade | -40 | 25 | 125 | °C |
| AVDD supply voltage[2] | $V_{AVDD}$ | | 1.8 | 3.3 | 3.8 | V |
| VREGVDD operating supply voltage[2] [1] | $V_{VREGVDD}$ | DCDC in regulation | 2.4 | 3.3 | 3.8 | V |
| | | DCDC in bypass, 50mA load | 1.8 | 3.3 | 3.8 | V |
| | | DCDC not in use. DVDD externally shorted to VREGVDD | 1.8 | 3.3 | 3.8 | V |
| VREGVDD current | $I_{VREGVDD}$ | DCDC in bypass, T ≤ 85 °C | — | — | 200 | mA |
| | | DCDC in bypass, T > 85 °C | — | — | 100 | mA |
| RFVDD operating supply voltage | $V_{RFVDD}$ | | 1.62 | — | $V_{VREGVDD}$ | V |
| DVDD operating supply voltage | $V_{DVDD}$ | | 1.62 | — | $V_{VREGVDD}$ | V |
| PAVDD operating supply voltage | $V_{PAVDD}$ | | 1.62 | — | $V_{VREGVDD}$ | V |
| IOVDD operating supply voltage | $V_{IOVDD}$ | All IOVDD pins | 1.62 | — | $V_{VREGVDD}$ | V |
| DECOUPLE output capacitor[3] [4] | $C_{DECOUPLE}$ | | 0.75 | 1.0 | 2.75 | µF |
| Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)[2] | $dV_{DD}$ | | — | — | 0.1 | V |
| HFCORECLK frequency | $f_{CORE}$ | VSCALE2, MODE = WS1 | — | — | 40 | MHz |
| | | VSCALE0, MODE = WS0 | — | — | 20 | MHz |
| HFCLK frequency | $f_{HFCLK}$ | VSCALE2 | — | — | 40 | MHz |
| | | VSCALE0 | — | — | 20 | MHz |

**Note:**

1. The minimum voltage required in bypass mode is calculated using $R_{BYP}$ from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD_min}+I_{LOAD} * R_{BYP_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. The maximum limit on $T_A$ may be lower due to device self-heating, which depends on the power dissipation of the specific application. $T_A$ (max) = $T_J$ (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for $T_J$ and $THETA_{JA}$.

Not Recommended For New Designs

### 4.1.3 Thermal Characteristics

**Table 4.3. Thermal Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal resistance, QFN48 Package | $THETA_{JA_QFN48}$ | 2-Layer PCB, Air velocity = 0 m/s | — | 64.5 | — | °C/W |
| | | 2-Layer PCB, Air velocity = 1 m/s | — | 51.6 | — | °C/W |
| | | 2-Layer PCB, Air velocity = 2 m/s | — | 47.7 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 0 m/s | — | 26.2 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 23.1 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 22.1 | — | °C/W |
| Thermal resistance, QFN32 Package | $THETA_{JA_QFN32}$ | 2-Layer PCB, Air velocity = 0 m/s | — | 82.1 | — | °C/W |
| | | 2-Layer PCB, Air velocity = 1 m/s | — | 64.7 | — | °C/W |
| | | 2-Layer PCB, Air velocity = 2 m/s | — | 56.3 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 0 m/s | — | 36.8 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 32 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 30.6 | — | °C/W |

Not Recommended For New Designs

### 4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

**Table 4.4. DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{DCDC_I}$ | Bypass mode, $I_{DCDC_LOAD}$ = 50 mA | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 100 mA, or Low power (LP) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 10 mA | 2.4 | — | $V_{VREGVDD_MAX}$ | V |
| | | Low noise (LN) mode, 1.8 V output, $I_{DCDC_LOAD}$ = 200 mA | 2.6 | — | $V_{VREGVDD_MAX}$ | V |
| Output voltage programmable range[1] | $V_{DCDC_O}$ | | 1.8 | — | $V_{VREGVDD}$ | V |
| Regulation DC accuracy | $ACC_{DC}$ | Low Noise (LN) mode, 1.8 V target output | 1.7 | — | 1.9 | V |
| Regulation window[4] | $WIN_{REG}$ | Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, $I_{DCDC_LOAD}$ ≤ 75 µA | 1.63 | — | 2.2 | V |
| | | Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, $I_{DCDC_LOAD}$ ≤ 10 mA | 1.63 | — | 2.1 | V |
| Steady-state output ripple | $V_R$ | Radio disabled | — | 3 | — | mVpp |
| Output voltage under/overshoot | $V_{OV}$ | CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA | — | 25 | 60 | mV |
| | | DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA | — | 45 | 90 | mV |
| | | Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode | — | 200 | — | mV |
| | | Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode | — | 40 | — | mV |
| | | Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode | — | 100 | — | mV |
| DC line regulation | $V_{REG}$ | Input changes between $V_{VREGVDD_MAX}$ and 2.4 V | — | 0.1 | — | % |
| DC load regulation | $I_{REG}$ | Load changes between 0 mA and 100 mA in CCM mode | — | 0.1 | — | % |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max load current | $I_{LOAD_MAX}$ | Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C | — | — | 200 | mA |
| | | Low noise (LN) mode, Heavy Drive[2], T > 85 °C | — | — | 100 | mA |
| | | Low noise (LN) mode, Medium Drive[2] | — | — | 100 | mA |
| | | Low noise (LN) mode, Light Drive[2] | — | — | 50 | mA |
| | | Low power (LP) mode, LPCMPBIASEMxx[3] = 0 | — | — | 75 | µA |
| | | Low power (LP) mode, LPCMPBIASEMxx[3] = 3 | — | — | 10 | mA |
| DCDC nominal output capacitor[5] | $C_{DCDC}$ | 25% tolerance | 1 | 4.7 | 4.7 | µF |
| DCDC nominal output inductor | $L_{DCDC}$ | 20% tolerance | 4.7 | 4.7 | 4.7 | µH |
| Resistance in Bypass mode | $R_{BYP}$ | | — | 1.2 | 2.5 | Ω |

**Note:**

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with $C_{DCDC}$ 4.7 µF. Different settings for DCDCLNCOMPCTRL must be used if $C_{DCDC}$ is lower than 4.7 µF. See Application Note AN0948 for details.

Not Recommended For New Designs

### 4.1.5 Current Consumption

#### 4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

**Table 4.5. Current Consumption 3.3 V without DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 38.4 MHz crystal, CPU running while loop from flash[1] | — | 123 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 96 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 93 | 103 | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 116 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 95 | 106 | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 227 | 384 | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | $I_{ACTIVE_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 82 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 198 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 38.4 MHz crystal[1] | — | 73 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 44 | 47 | µA/MHz |
| | | 26 MHz HFRCO | — | 46 | 51 | µA/MHz |
| | | 1 MHz HFRCO | — | 178 | 335 | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | $I_{EM1_VS}$ | 19 MHz HFRCO | — | 41 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 158 | — | µA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled | $I_{EM2_VS}$ | Full 32 kB RAM retention and RTCC running from LFXO | — | 1.9 | — | µA |
| | | Full 32 kB RAM retention and RTCC running from LFRCO | — | 2.2 | — | µA |
| | | 1 bank (16 kB) RAM retention and RTCC running from LFRCO[2] | — | 1.9 | 3.3 | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | $I_{EM3_VS}$ | Full 32 kB RAM retention and CRYOTIMER running from ULFRCO | — | 1.44 | 3.0 | µA |
| Current consumption in EM4H mode, with voltage scaling enabled | $I_{EM4H_VS}$ | 128 byte RAM retention, RTCC running from LFXO | — | 0.89 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.55 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.54 | 0.8 | µA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM4S mode | $I_{EM4S}$ | No RAM retention, no RTCC | — | 0.04 | 0.085 | µA |

**Note:**

1. CMU_HFXOCTRL_LOWPOWER=0.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Not Recommended For New Designs

#### 4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

**Table 4.6. Current Consumption 3.3 V using DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2] | $I_{ACTIVE_DCM}$ | 38.4 MHz crystal, CPU running while loop from flash[4] | — | 84 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 68 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 67 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 80 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 73 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 606 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1] | $I_{ACTIVE_CCM}$ | 38.4 MHz crystal, CPU running while loop from flash[4] | — | 94 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 79 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 78 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 90 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 90 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1109 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1] | $I_{ACTIVE_CCM_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 97 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1093 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2] | $I_{EM1_DCM}$ | 38.4 MHz crystal[4] | — | 55 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 38 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 45 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 580 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2] | $I_{EM1_DCM_VS}$ | 19 MHz HFRCO | — | 48 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 569 | — | µA/MHz |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3] | $I_{EM2_VS}$ | Full 32 kB RAM retention and RTCC running from LFXO | — | 1.4 | — | µA |
| | | Full 32 kB RAM retention and RTCC running from LFRCO | — | 1.5 | — | µA |
| | | 1 bank (16 kB) RAM retention and RTCC running from LFRCO[5] | — | 1.3 | — | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | $I_{EM3_VS}$ | Full 32 kB RAM retention and CRYOTIMER running from ULFRCO | — | 1.02 | — | µA |
| Current consumption in EM4H mode, with voltage scaling enabled | $I_{EM4H_VS}$ | 128 byte RAM retention, RTCC running from LFXO | — | 0.74 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.48 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.48 | — | µA |
| Current consumption in EM4S mode | $I_{EM4S}$ | No RAM retention, no RTCC | — | 0.07 | — | µA |

**Note:**

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. CMU_HFXOCTRL_LOWPOWER=0.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Not Recommended For New Designs

#### 4.1.5.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

**Table 4.7. Current Consumption 1.8 V without DC-DC Converter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled | $I_{ACTIVE}$ | 38.4 MHz crystal, CPU running while loop from flash[1] | — | 123 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running Prime from flash | — | 96 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running while loop from flash | — | 93 | — | µA/MHz |
| | | 38 MHz HFRCO, CPU running CoreMark from flash | — | 115 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 95 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 224 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled | $I_{ACTIVE_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 81 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 195 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled | $I_{EM1}$ | 38.4 MHz crystal[1] | — | 74 | — | µA/MHz |
| | | 38 MHz HFRCO | — | 44 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 46 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 175 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled | $I_{EM1_VS}$ | 19 MHz HFRCO | — | 41 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 155 | — | µA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled | $I_{EM2_VS}$ | Full 32 kB RAM retention and RTCC running from LFXO | — | 1.7 | — | µA |
| | | Full 32 kB RAM retention and RTCC running from LFRCO | — | 1.9 | — | µA |
| | | 1 bank (16 kB) RAM retention and RTCC running from LFRCO[2] | — | 1.7 | — | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | $I_{EM3_VS}$ | Full 32 kB RAM retention and CRYOTIMER running from ULFRCO | — | 1.33 | — | µA |
| Current consumption in EM4H mode, with voltage scaling enabled | $I_{EM4H_VS}$ | 128 byte RAM retention, RTCC running from LFXO | — | 0.80 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.44 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.43 | — | µA |
| Current consumption in EM4S mode | $I_{EM4S}$ | no RAM retention, no RTCC | — | 0.04 | — | µA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. CMU_HFXOCTRL_LOWPOWER=0.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Not Recommended For New Designs

#### 4.1.5.4 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

**Table 4.8. Current Consumption Using Radio 3.3 V with DC-DC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C | $I_{RX_ACTIVE}$ | 500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4 | — | 9.3 | 10.2 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4 | — | 8.6 | 10.2 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4 | — | 8.6 | 10.2 | mA |
| | | 50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4 | — | 8.6 | 10.2 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4 | — | 8.6 | 10.2 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4 | — | 8.4 | 10.2 | mA |
| | | 1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4 | — | 8.8 | — | mA |
| | | 802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3 | — | 10.2 | — | mA |
| Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C | $I_{RX_ACTIVE_HT}$ | 500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |
| | | 50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4 | — | — | 13 | mA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C | $I_{RX_LISTEN}$ | 500 kbit/s, 2GFSK, F = 915 MHz, No radio clock prescaling | — | 10.2 | 11 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 868 MHz, No radio clock prescaling | — | 9.5 | 11 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 490 MHz, No radio clock prescaling | — | 9.5 | 11 | mA |
| | | 50 kbit/s, 2GFSK, F = 433 MHz, No radio clock prescaling | — | 9.5 | 11 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 315 MHz, No radio clock prescaling | — | 9.4 | 11 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 169 MHz, No radio clock prescaling | — | 9.3 | 11 | mA |
| | | 1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling | — | 9.6 | — | mA |
| | | 802.15.4, F = 2.4 GHz, No radio clock prescaling | — | 11.1 | — | mA |
| Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C | $I_{RX_LISTEN_HT}$ | 500 kbit/s, 2GFSK, F = 915 MHz, No radio clock prescaling | — | — | 14 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 868 MHz, No radio clock prescaling | — | — | 14 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 490 MHz, No radio clock prescaling | — | — | 14 | mA |
| | | 50 kbit/s, 2GFSK, F = 433 MHz, No radio clock prescaling | — | — | 14 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 315 MHz, No radio clock prescaling | — | — | 14 | mA |
| | | 38.4 kbit/s, 2GFSK, F = 169 MHz, No radio clock prescaling | — | — | 14 | mA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C | $I_{TX}$ | F = 915 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | 90.2 | 134.3 | mA |
| | | F = 915 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | 36 | 42.5 | mA |
| | | F = 868 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | 79.7 | 106.7 | mA |
| | | F = 868 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | 35.3 | 41 | mA |
| | | F = 490 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | 93.8 | 125.4 | mA |
| | | F = 433 MHz, CW, 10 dBm match, External PA supply connected to DC-DC output | — | 20.3 | 24 | mA |
| | | F = 433 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | 34 | 41.5 | mA |
| | | F = 315 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | 33.5 | 42 | mA |
| | | F = 169 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | 88.6 | 116.7 | mA |
| | | F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3 | — | 8.5 | — | mA |
| | | F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1 | — | 9.5 | — | mA |
| | | F = 2.4 GHz, CW, 3 dBm output power | — | 16.5 | — | mA |
| | | F = 2.4 GHz, CW, 8 dBm output power | — | 26.0 | — | mA |
| | | F = 2.4 GHz, CW, 10.5 dBm output power | — | 34.0 | — | mA |
| | | F = 2.4 GHz, CW, 16.5 dBm output power, PAVDD connected directly to external 3.3V supply | — | 91.6 | — | mA |
| | | F = 2.4 GHz, CW, 19.5 dBm output power, PAVDD connected directly to external 3.3V supply | — | 131.0 | — | mA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C | $I_{TX_HT}$ | F = 915 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | — | 134.3 | mA |
| | | F = 915 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | — | 42.5 | mA |
| | | F = 868 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | — | 109.8 | mA |
| | | F = 868 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | — | 41.3 | mA |
| | | F = 490 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | — | 130.8 | mA |
| | | F = 433 MHz, CW, 10 dBm match, External PA supply connected to DC-DC output | — | — | 24.4 | mA |
| | | F = 433 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | — | 41.5 | mA |
| | | F = 315 MHz, CW, 14 dBm match, External PA supply connected to DCDC output | — | — | 42 | mA |
| | | F = 169 MHz, CW, 20 dBm match, External PA supply = 3.3V | — | — | 122.8 | mA |

Not Recommended For New Designs

### 4.1.6 Wake Up Times

**Table 4.9. Wake Up Times**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Wake up time from EM1 | $t_{EM1_WU}$ | | — | 3 | — | AHB Clocks |
| Wake up from EM2 | $t_{EM2_WU}$ | Code execution from flash | — | 10 | — | µs |
| | | Code execution from RAM | — | 3 | — | µs |
| Wake up from EM3 | $t_{EM3_WU}$ | Code execution from flash | — | 10 | — | µs |
| | | Code execution from RAM | — | 3 | — | µs |
| Wake up from EM4H[1] | $t_{EM4H_WU}$ | Executing from flash | — | 86 | — | µs |
| Wake up from EM4S[1] | $t_{EM4S_WU}$ | Executing from flash | — | 290 | — | µs |
| Time from release of reset source to first instruction execution | $t_{RESET}$ | Soft Pin Reset released | — | 50 | — | µs |
| | | Any other reset released | — | 340 | — | µs |
| Power mode scaling time | $t_{SCALE}$ | VSCALE0 to VSCALE2, HFCLK = 19 MHz[4] [2] | — | 31.8 | — | µs |
| | | VSCALE2 to VSCALE0, HFCLK = 19 MHz[3] | — | 4.3 | — | µs |

**Note:**

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

Not Recommended For New Designs

### 4.1.7 Brown Out Detector (BOD)

**Table 4.10. Brown Out Detector (BOD)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DVDD BOD threshold | $V_{DVDDBOD}$ | DVDD rising | — | — | 1.62 | V |
| | | DVDD falling (EM0/EM1) | 1.35 | — | — | V |
| | | DVDD falling (EM2/EM3) | 1.3 | — | — | V |
| DVDD BOD hysteresis | $V_{DVDDBOD_HYST}$ | | — | 18 | — | mV |
| DVDD BOD response time | $t_{DVDDBOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 2.4 | — | µs |
| AVDD BOD threshold | $V_{AVDDBOD}$ | AVDD rising | — | — | 1.8 | V |
| | | AVDD falling (EM0/EM1) | 1.62 | — | — | V |
| | | AVDD falling (EM2/EM3) | 1.53 | — | — | V |
| AVDD BOD hysteresis | $V_{AVDDBOD_HYST}$ | | — | 20 | — | mV |
| AVDD BOD response time | $t_{AVDDBOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 2.4 | — | µs |
| EM4 BOD threshold | $V_{EM4DBOD}$ | AVDD rising | — | — | 1.7 | V |
| | | AVDD falling | 1.45 | — | — | V |
| EM4 BOD hysteresis | $V_{EM4BOD_HYST}$ | | — | 25 | — | mV |
| EM4 BOD response time | $t_{EM4BOD_DELAY}$ | Supply drops at 0.1V/µs rate | — | 300 | — | µs |

Not Recommended For New Designs

### 4.1.8 Frequency Synthesizer

**Table 4.11. Frequency Synthesizer**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF synthesizer frequency range | $f_{RANGE}$ | 2400 - 2483.5 MHz | 2400 | — | 2483.5 | MHz |
| | | 779 - 956 MHz | 779 | — | 956 | MHz |
| | | 584 - 717 MHz | 584 | — | 717 | MHz |
| | | 358 - 574 MHz | 358 | — | 574 | MHz |
| | | 191 - 358 MHz | 191 | — | 358 | MHz |
| | | 110 - 191 MHz | 110 | — | 191 | MHz |
| LO tuning frequency resolution with 38.4 MHz crystal | $f_{RES}$ | 2400 - 2483.5 MHz | — | — | 73 | Hz |
| | | 779 - 956 MHz | — | — | 24 | Hz |
| | | 584 - 717 MHz | — | — | 18.3 | Hz |
| | | 358 - 574 MHz | — | — | 12.2 | Hz |
| | | 191 - 358 MHz | — | — | 7.3 | Hz |
| | | 110 - 191 MHz | — | — | 4.6 | Hz |
| Frequency deviation resolution with 38.4 MHz crystal | $df_{RES}$ | 2400 - 2483.5 MHz | — | — | 73 | Hz |
| | | 779 - 956 MHz | — | — | 24 | Hz |
| | | 584 - 717 MHz | — | — | 18.3 | Hz |
| | | 358 - 574 MHz | — | — | 12.2 | Hz |
| | | 191 - 358 MHz | — | — | 7.3 | Hz |
| | | 110 - 191 MHz | — | — | 4.6 | Hz |
| Maximum frequency deviation with 38.4 MHz crystal | $df_{MAX}$ | 2400 - 2483.5 MHz | — | — | 1677 | kHz |
| | | 779 - 956 MHz | — | — | 559 | kHz |
| | | 584 - 717 MHz | — | — | 419 | kHz |
| | | 358 - 574 MHz | — | — | 280 | kHz |
| | | 191 - 358 MHz | — | — | 167 | kHz |
| | | 110 - 191 MHz | — | — | 105 | kHz |

Not Recommended For New Designs

### 4.1.9 2.4 GHz RF Transceiver Characteristics

#### 4.1.9.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.12. RF Transmitter General Characteristics for 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum TX power[1] | $POUT_{MAX}$ | 19 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply | — | 19.5 | — | dBm |
| | | 10 dBm-rated part numbers | — | 10.5 | — | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | CW | | -30 | — | dBm |
| Output power step size | $POUT_{STEP}$ | -5 dBm< Output power < 0 dBm | — | 1 | — | dB |
| | | 0 dBm < output power < $POUT_{MAX}$ | — | 0.5 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power > 10 dBm. | — | 4.5 | — | dB |
| | | 1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power = 10 dBm. | — | 3.8 | — | dB |
| | | 1.8 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter | — | 2.2 | — | dB |
| Output power variation vs temperature at $POUT_{MAX}$ | $POUT_{VAR_T}$ | From -40 to +85 °C, PAVDD connected to DC-DC output | — | 1.5 | — | dB |
| | | From -40 to +125 °C, PAVDD connected to DC-DC output | — | 2.6 | — | dB |
| | | From -40 to +85 °C, PAVDD connected to external supply | — | 1.5 | — | dB |
| | | From -40 to +125 °C, PAVDD connected to external supply | — | 2.0 | — | dB |
| Output power variation vs RF frequency at $POUT_{MAX}$ | $POUT_{VAR_F}$ | Over RF tuning frequency range | — | 0.4 | — | dB |
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.9.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.13. RF Receiver General Characteristics for 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 2400 | — | 2483.5 | MHz |
| Receive mode maximum spurious emission | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -57 | — | dBm |
| | | 1 GHz to 12 GHz | — | -47 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216 MHz to 960 MHz, Conducted Measurement | — | -55.2 | — | dBm |
| | | Above 960 MHz, Conducted Measurement | — | -47.2 | — | dBm |
| Level above which RFSENSE will trigger[1] | $RFSENSE_{TRIG}$ | CW at 2.45 GHz | — | -24 | — | dBm |
| Level below which RFSENSE will not trigger[1] | $RFSENSE_{THRES}$ | CW at 2.45 GHz | — | -50 | — | dBm |
| 1% PER sensitivity | $SENS_{2GFSK}$ | 2 Mbps 2GFSK signal | — | -89.6 | — | dBm |
| | | 250 kbps 2GFSK signal | — | -100.7 | — | dBm |

**Note:**
1. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.9.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 85%.

**Table 4.14. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmit 6dB bandwidth | TXBW | 10 dBm | — | 761 | — | kHz |
| Power spectral density limit | $PSD_{LIMIT}$ | Per FCC part 15.247 at 10 dBm | — | -9.5 | — | dBm/ 3kHz |
| | | Per FCC part 15.247 at 20 dBm | — | -2 | — | dBm/ 3kHz |
| | | Per ETSI 300.328 at 10 dBm/1 MHz | — | 10 | — | dBm |
| Occupied channel bandwidth per ETSI EN300.328 | $OCP_{ETSI328}$ | 99% BW at highest and lowest channels in band, 10 dBm | — | 1.1 | — | MHz |
| In-band spurious emissions, with allowed exceptions[3] | $SPUR_{INB}$ | At ± 2 MHz, 10 dBm | — | -39.5 | — | dBm |
| | | At ± 3 MHz, 10 dBm | — | -44.3 | — | dBm |
| | | At ± 2 MHz, 20 dBm | — | — | -20 | dBm |
| | | At ± 3 MHz, 20 dBm | — | — | -30 | dBm |
| Emissions of harmonics out-of-band, per FCC part 15.247 | $SPUR_{HRM_FCC}$ | 2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier | — | -47 | — | dBm |
| Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply | $SPUR_{OOB_FCC}$ | Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[1 2] | — | -47 | — | dBm |
| | | Per FCC part 15.247, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Non-Restricted Bands | — | -26 | — | dBc |
| Spurious emissions out-of-band; per ETSI 300.328 | $SPUR_{ETSI328}$ | [2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz | — | -16 | — | dBm |
| | | [2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328 | — | -26 | — | dBm |
| Spurious emissions per ETSI EN300.440 | $SPUR_{ETSI440}$ | 47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz | — | -60 | — | dBm |
| | | 25-1000 MHz | — | -42 | — | dBm |
| | | 1-12 GHz | — | -36 | — | dBm |

**Note:**

1. For 2476 MHz, 1.5 dB of power backoff is used to achieve this value.
2. For 2478 MHz, 4.2 dB of power backoff is used to achieve this value.
3. Per Bluetooth Core_5.0, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

Not Recommended For New Designs

#### 4.1.9.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz.

**Table 4.15. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4GHz Band, 1 Mbps Data Rate**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level, 0.1% BER | SAT | Signal is reference signal[2]. Packet length is 20 bytes. | — | 10 | — | dBm |
| Sensitivity, 0.1% BER | SENS | Signal is reference signal[2]. Using DC-DC converter. | — | -93.8 | — | dBm |
| | | With non-ideal signals as specified in RF-PHY.TS.4.2.2, section 4.6.1. | — | -93.6 | — | dBm |
| Signal to co-channel interferer, 0.1% BER | $C/I_{CC}$ | Desired signal 3 dB above reference sensitivity. | — | 11.25 | — | dB |
| N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm | $C/I_{1+}$ | Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz | — | -4.7 | — | dB |
| N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm | $C/I_{1-}$ | Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz | — | -4.8 | — | dB |
| Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm | $C/I_2$ | Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz | — | -45.8 | — | dB |
| Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm | $C/I_3$ | Interferer is reference signal at ± 3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz | — | -49.4 | — | dB |
| Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm | $C/I_{IM}$ | Interferer is reference signal at image frequency with 1 MHz precision | — | -40.5 | — | dB |
| Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -67 dBm | $C/I_{IM+1}$ | Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision | — | -49.4 | — | dB |
| Blocking, less than 0.1% BER. Desired is -67dBm BLE reference signal at 2426MHz. Interferer is CW in OOB range[1] | $BLOCK_{OOB}$ | Interferer frequency 30 MHz ≤ f ≤ 2000 MHz | -5 | — | — | dBm |
| | | Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz[3] | -10 | — | — | dBm |
| | | Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz | -10 | — | — | dBm |
| | | Interferer frequency 3 GHz ≤ f ≤ 6 GHz | -10 | — | — | dBm |
| | | Interferer frequency 6 GHz ≤ f ≤ 12.75 GHz | -17 | — | — | dBm |
| Intermodulation performance | IM | Per Core_4.1, Vol 6, Part A, Section 4.4 with n = 3 | — | -22.2 | — | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Interferer max power limited by equipment capabilities and path loss. Minimum specified at 25 °C.
2. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
3. Except -13 dBm at Desired Frequency - Crystal Frequency.

Not Recommended For New Designs

#### 4.1.9.5 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 66%.

**Table 4.16. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error vector magnitude (offset EVM), per 802.15.4-2011, not including 2415 MHz channel | EVM | Average across frequency. Signal is DSSS-OQPSK reference packet[1] | — | 3.8 | — | % rms |
| Power spectral density limit | $PSD_{LIMIT}$ | Relative, at carrier ± 3.5 MHz, output power at $POUT_{MAX}$ | — | -26 | — | dBc/ 100kHz |
| | | Absolute, at carrier ± 3.5 MHz, output power at $POUT_{MAX}$[3] | — | -36 | — | dBm/ 100kHz |
| | | Per FCC part 15.247, output power at $POUT_{MAX}$ | — | -4.0 | — | dBm/ 3kHz |
| | | ETSI | — | 12.1 | — | dBm |
| Occupied channel bandwidth per ETSI EN300.328 | $OCP_{ETSI328}$ | 99% BW at highest and lowest channels in band | — | 2.25 | — | MHz |
| Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz | $SPUR_{HRM_FCC_R}$ | Continuous transmission of modulated carrier | — | -45.8 | — | dBm |
| Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz | $SPUR_{HRM_FCC_NRR}$ | Continuous transmission of modulated carrier | — | -26 | — | dBc |
| Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz | $SPUR_{OOB_FCC_R}$ | Restricted bands 30-88 MHz; continuous transmission of modulated carrier | — | -61 | — | dBm |
| | | Restricted bands 88-216 MHz; continuous transmission of modulated carrier | — | -58 | — | dBm |
| | | Restricted bands 216-960 MHz; continuous transmission of modulated carrier | — | -55 | — | dBm |
| | | Restricted bands >960 MHz; continuous transmission of modulated carrier[4] [5] | — | -47 | — | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz | $SPUR_{OOB_FCC_NR}$ | Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier | — | -26 | — | dBc |
| Spurious emissions out-of-band; per ETSI 300.328[2] | $SPUR_{ETSI328}$ | [2400-BW to 2400], [2483.5 to 2483.5+BW]; | — | -16 | — | dBm |
| | | [2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328 | — | -26 | — | dBm |
| Spurious emissions per ETSI EN300.440[2] | $SPUR_{ETSI440}$ | 47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz | — | -60 | — | dBm |
| | | 25-1000 MHz, excluding above frequencies | — | -42 | — | dBm |
| | | 1G-14G | — | -36 | — | dBm |

**Note:**

1. Reference packet is defined as 20 octet PSDU, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content.
2. Specified at maximum power output level of 10 dBm.
3. For 2415 MHz, 2 dB of power backoff is used to achieve this value.
4. For 2475 MHz, 2 dB of power backoff is used to achieve this value.
5. For 2480 MHz, 13 dB of power backoff is used to achieve this value.

Not Recommended For New Designs

#### 4.1.9.6 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

**Table 4.17. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Max usable receiver input level, 1% PER | SAT | Signal is reference signal[4]. Packet length is 20 octets. | — | 10 | — | dBm |
| Sensitivity, 1% PER | SENS | Signal is reference signal. Packet length is 20 octets. Using DC-DC converter. | — | -103.3 | — | dBm |
| | | Signal is reference signal. Packet length is 20 octets. Without DC-DC converter. | — | -103.3 | — | dBm |
| Co-channel interferer rejection, 1% PER | CCR | Desired signal 3 dB above sensitivity limit | — | -4.6 | — | dB |
| High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[5] | $ACR_{P1}$ | Interferer is reference signal at +1 channel-spacing. | — | 40.7 | — | dB |
| | | Interferer is filtered reference signal[2] at +1 channel-spacing. | — | 47 | — | dB |
| | | Interferer is CW at +1 channel-spacing[3]. | — | 60.1 | — | dB |
| Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[5] | $ACR_{M1}$ | Interferer is reference signal at -1 channel-spacing. | — | 40.8 | — | dB |
| | | Interferer is filtered reference signal[2] at -1 channel-spacing. | — | 47.5 | — | dB |
| | | Interferer is CW at -1 channel-spacing. | — | 61.6 | — | dB |
| Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[5] | $ACR_2$ | Interferer is reference signal at ± 2 channel-spacing | — | 51.5 | — | dB |
| | | Interferer is filtered reference signal[2] at ± 2 channel-spacing | — | 53.7 | — | dB |
| | | Interferer is CW at ± 2 channel-spacing | — | 66.4 | — | dB |
| Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level[5] | IR | Interferer is CW in image band[3] | — | 50.4 | — | dB |
| Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[5]. Interferer is reference signal | BLOCK | Interferer frequency < Desired frequency - 3 channel-spacing | — | 58.5 | — | dB |
| | | Interferer frequency > Desired frequency + 3 channel-spacing | — | 56.4 | — | dB |
| Blocking rejection of 802.11g signal centered at +12MHz or -13MHz[1] | $BLOCK_{80211G}$ | Desired is reference signal at 6dB above reference sensitivity level[5] | — | 54.8 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | over $RSSI_{MIN}$ to $RSSI_{MAX}$ | — | 0.25 | — | dB |
| RSSI accuracy in the linear region as defined by 802.15.4-2003 | $RSSI_{LIN}$ | | — | +/-6 | — | dB |

**Note:**

1. This is an IEEE 802.11b/g ERP-PBCC 22 MBit/s signal as defined by the IEEE 802.11 specification and IEEE 802.11g addendum.
2. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stopband rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.
4. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
5. Reference sensitivity level is -85 dBm.

Not Recommended For New Designs

### 4.1.10 Sub-GHz RF Transceiver Characteristics

Not Recommended For New Designs

#### 4.1.10.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 915 MHz.

**Table 4.18. Sub-GHz RF Transmitter characteristics for 915 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 902 | — | 930 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA supply = 3.3V, 20 dBm output power setting | 18 | 19.8 | 23.3 | dBm |
| | | External PA supply connected to DC-DC output, 14 dBm output power setting | 12.6 | 14.2 | 16.1 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -45.5 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = 3.3 V, T = 25 °C | — | 4.8 | — | dB |
| | | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply connected to DC-DC output, T = 25 °C | — | 1.9 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | -40 to +85 °C with External PA supply = 3.3 V | — | 0.6 | 1.3 | dB |
| | | -40 to +125 °C with External PA supply = 3.3 V | — | 0.8 | 1.6 | dB |
| | | -40 to +85 °C with External PA supply connected to DC-DC output | — | 0.7 | 1.4 | dB |
| | | -40 to +125 °C with External PA supply connected to DC-DC output | — | 1.0 | 1.9 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | External PA supply = 3.3 V, T = 25 °C | — | 0.2 | 0.6 | dB |
| | | External PA supply connected to DC-DC output, T = 25 °C | — | 0.3 | 0.6 | dB |
| Spurious emissions of harmonics at 20 dBm output power, Conducted measurement, 20dBm match, External PA supply = 3.3V, Test Frequency = 915 MHz | $SPUR_{HARM_FCC_20}$ | In restricted bands, per FCC Part 15.205 / 15.209 | — | -45 | -42 | dBm |
| | | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emissions out-of-band at 20 dBm output power, Conducted measurement, 20dBm match, External PA supply = 3.3V, Test Frequency = 915 MHz | $SPUR_{OOB_FCC_20}$ | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209 | — | -52 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209 | — | -61 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209 | — | -58 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |
| Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 915 MHz | $SPUR_{HARM_FCC_14}$ | In restricted bands, per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |
| | | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 915 MHz | $SPUR_{OOB_FCC_14}$ | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209 | — | -52 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209 | — | -61 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209 | — | -58 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209 | — | -45 | -42 | dBm |
| Error vector magnitude (offset EVM), per 802.15.4-2011 | EVM | Signal is DSSS-OQPSK reference packet. Modulated according to 802.15.4-2011 DSSS-OQPSK in the 915MHz band, with pseudo-random packet data content. External PA supply = 3.3V. | — | 1.0 | 2.8 | %rms |
| Power spectral density limit | PSD | Relative, at carrier ± 1.2 MHz. Average spectral power shall be measured using a 100kHz resolution bandwidth. The reference level shall be the highest average spectral power measured within ± 600kHz of the carrier frequency. External PA supply = 3.3V. | — | -37.1 | -24.8 | dBc/ 100kHz |
| | | Absolute, at carrier ± 1.2 MHz. Average spectral power shall be measured using a 100kHz resolution bandwidth. External PA supply = 3.3V. | — | -24.2 | -20 | dBm/ 100kHz |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.10.2 Sub-GHz RF Receiver Characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 915 MHz.

**Table 4.19. Sub-GHz RF Receiver Characteristics for 915 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 902 | — | 930 | MHz |
| Max usable input level, 0.1% BER | $SAT_{500K}$ | Desired is reference 500 kbps GFSK signal[4] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 4.8 kbps OOK signal[3], 20% PER, T ≤ 85 °C | — | -107.8 | -100.7 | dBm |
| | | Desired is reference 4.8 kbps OOK signal[3], 20% PER, T > 85 °C | — | — | -99.5 | dBm |
| | | Desired is reference 600 bps GFSK signal[6], 0.1% BER | — | -126.2 | — | dBm |
| | | Desired is reference 50 kbps GFSK signal[5], 0.1% BER, T ≤ 85 °C | — | -108.2 | -104.2 | dBm |
| | | Desired is reference 50 kbps GFSK signal[5], 0.1% BER, T > 85 °C | — | — | -103.1 | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C | — | -105.1 | -101.5 | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C | — | — | -101.3 | dBm |
| | | Desired is reference 500 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C | — | -98.2 | -93.2 | dBm |
| | | Desired is reference 500 kbps GFSK signal[4], 0.1% BER, T > 85 °C | — | — | -93.1 | dBm |
| | | Desired is reference 400 kbps GFSK signal[2], 1% PER, T ≤ 85 °C | — | -95.2 | -91 | dBm |
| | | Desired is reference 400 kbps GFSK signal[2], 1% PER, T > 85 °C | — | — | -91 | dBm |
| | | Desired is reference O-QPSK DSSS signal[7], 1% PER, Payload length is 20 octets | — | -100.1 | — | dBm |
| Level above which RFSENSE will trigger[8] | $RFSENSE_{TRIG}$ | CW at 915 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[8] | $RFSENSE_{THRES}$ | CW at 915 MHz | — | -50 | — | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing | $C/I_1$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 48.1 | — | dB |
| | | Desired is 600 bps GFSK signal[6] at 3dB above sensitivity level, 0.1% BER | — | 71.4 | — | dB |
| | | Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER | — | 49.8 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 51.1 | — | dB |
| | | Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 48.1 | — | dB |
| | | Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 41.4 | — | dB |
| | | Desired is reference O-QPSK DSSS signal[7] at 3dB above sensitivity level, 1% PER | — | 49.1 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing | $C/I_2$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 56.3 | — | dB |
| | | Desired is 600 bps GFSK signal[6] at 3dB above sensitivity level, 0.1% BER | — | 74.7 | — | dB |
| | | Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER | — | 55.8 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 56.4 | — | dB |
| | | Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 51.8 | — | dB |
| | | Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 46.8 | — | dB |
| | | Desired is reference O-QPSK DSSS signal[7] at 3dB above sensitivity level, 1% PER | — | 57.7 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 48.4 | — | dB |
| | | Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER | — | 54.9 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 49.1 | — | dB |
| | | Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 47.9 | — | dB |
| | | Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 42.8 | — | dB |
| | | Desired is reference O-QPSK DSSS signal[7] at 3dB above sensitivity level, 1% PER | — | 48.9 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 100 kbps GFSK signal at 3dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 58.7 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 62.5 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 76.4 | — | dB |
| Intermod selectivity, 0.1% BER. CW interferers at 400 kHz and 800 kHz offsets | $C/I_{IM}$ | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level | — | 45 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -55 | -49.2 | dBm |
| | | Above 960 MHz | — | -47 | -41.2 | dBm |
| Max spurious emissions during active receive mode,per ARIB STD-T108 Section 3.3 | $SPUR_{RX_ARIB}$ | Below 710 MHz, RBW=100kHz | — | -60 | -54 | dBm |
| | | 710-900 MHz, RBW=1MHz | — | -61 | -55 | dBm |
| | | 900-915 MHz, RBW=100kHz | — | -61 | -55 | dBm |
| | | 915-930 MHz, RBW=100kHz | — | -61 | -55 | dBm |
| | | 930-1000 MHz, RBW=100kHz | — | -60 | -54 | dBm |
| | | Above 1000 MHz, RBW=1MHz | — | -53 | -47 | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz, channel spacing = 400 kHz.
2. Definition of reference signal is 400 kbps 4GFSK, BT=0.5, inner deviation = 33.3 kHz, RX channel BW = 368.920 kHz, channel spacing = 600 kHz.
3. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 306.036 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 175 kHz, RX channel BW = 835.076 kHz, channel spacing = 1 MHz.
5. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 99.012 kHz, channel spacing = 200 kHz.
6. Definition of reference signal is 600 bps 2GFSK, BT=0.5, Δf = 0.3 kHz, RX channel BW = 1.2 kHz, channel spacing = 300 kHz.
7. Definition of reference signal is O-QPSK DSSS per 802.15.4, Frequency Range = 902-928 MHz, Data rate = 250 kbps, 16-chip PN sequence mapping.
8. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.10.3 Sub-GHz RF Transmitter characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 868 MHz.

**Table 4.20. Sub-GHz RF Transmitter characteristics for 868 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 863 | — | 876 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA connected directly to 3.3V supply, 20 dBm output power setting | 17.1 | 19.3 | 22.9 | dBm |
| | | External PA supply connected to DC-DC output, 14 dBm output power setting | 11.4 | 13.7 | 16.5 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -43.5 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply at $POUT_{MAX}$ | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = 3.3 V, T = 25 °C | — | 5 | — | dB |
| | | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply connected to DC-DC output, T = 25 °C | — | 2 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | -40 to +85 °C with External PA supply = 3.3 V | — | 0.6 | 0.9 | dB |
| | | -40 to +125 °C with External PA supply = 3.3 V | — | 0.8 | 1.3 | dB |
| | | -40 to +85 °C with External PA supply connected to DC-DC output | — | 0.5 | 1.2 | dB |
| | | -40 to +125 °C with External PA supply connected to DC-DC output | — | 0.7 | 1.5 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | External PA supply = 3.3 V, T = 25 °C | — | 0.2 | 0.6 | dB |
| | | External PA supply connected to DC-DC output, T = 25 °C | — | 0.2 | 0.8 | dB |
| Spurious emissions of harmonics, Conducted measurement, External PA supply connected to DC-DC output, Test Frequency = 868 MHz | $SPUR_{HARM_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 | — | -35 | -30 | dBm |
| Spurious emissions out-of-band, Conducted measurement, External PA supply connected to DC-DC output, Test Frequency = 868 MHz | $SPUR_{OOB_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -59 | -54 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) | — | -42 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) | — | -36 | -30 | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Error vector magnitude (offset EVM), per 802.15.4-2015 | EVM | Signal is DSSS-BPSK reference packet. Modulated according to 802.15.4-2015 DSSS-BPSK in the 868MHz band, with pseudo-random packet data content. External PA supply connected to external 3.3V supply | — | 5.7 | — | %rms |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.10.4 Sub-GHz RF Receiver Characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 868 MHz.

**Table 4.21. Sub-GHz RF Receiver Characteristics for 868 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 863 | — | 876 | MHz |
| Max usable input level, 0.1% BER | $SAT_{2k4}$ | Desired is reference 2.4 kbps GFSK signal[1] | — | 10 | — | dBm |
| Max usable input level, 0.1% BER | $SAT_{38k4}$ | Desired is reference 38.4 kbps GFSK signal[2] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER | — | -120.6 | — | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C | — | -109.5 | -105.4 | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C | — | — | -105.2 | dBm |
| | | Desired is reference 500 kbps GFSK signal[3], 0.1% BER | — | -96.4 | — | dBm |
| Level above which RFSENSE will trigger[4] | $RFSENSE_{TRIG}$ | CW at 868 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[4] | $RFSENSE_{THRES}$ | CW at 868 MHz | — | -50 | — | dBm |
| Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing | $C/I_1$ | Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | 44.5 | 56.9 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | 35.4 | 43 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing | $C/I_2$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 56.8 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 48.2 | — | dB |
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 50.2 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 48.7 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 72.1 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 77.5 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 90.4 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -63 | -57 | dBm |
| | | 1 GHz to 12 GHz | — | -53 | -47 | dBm |

**Note:**

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.797 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.10.5 Sub-GHz RF Transmitter characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 490 MHz.

**Table 4.22. Sub-GHz RF Transmitter characteristics for 490 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 470 | — | 510 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA supply = 3.3V | 18.1 | 20.3 | 23.7 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | | -44.9 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply, peak to peak | $POUT_{VAR_V}$ | at 20 dBm;1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply connected directly to external supply, T = 25 °C | — | 4.3 | — | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | -40 to +85 °C at 20 dBm | — | 0.2 | 0.9 | dB |
| | | -40 to +125 °C at 20 dBm | — | 0.3 | 1.3 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | T = 25 °C | — | 0.2 | 0.4 | dB |
| Harmonic emissions, 20 dBm output power setting, 490 MHz | $SPUR_{HARM_CN}$ | Per China SRW Requirement, Section 2.1, frequencies below 1GHz | — | -40 | -36 | dBm |
| | | Per China SRW Requirement, Section 2.1, frequencies above 1GHz | — | -36 | -30 | dBm |
| Spurious emissions, 20 dBm output power setting, 490 MHz | $SPUR_{OOB_CN}$ | Per China SRW Requirement, Section 3 (48.5-72.5MHz, 76-108MHz, 167-223MHz, 470-556MHz, and 606-798MHz) | — | -54 | — | dBm |
| | | Per China SRW Requirement, Section 2.1 (other frequencies below 1GHz) | — | -42 | — | dBm |
| | | Per China SRW Requirement, Section 2.1 (frequencies above 1GHz) | — | -36 | — | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.10.6 Sub-GHz RF Receiver Characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 490 MHz.

**Table 4.23. Sub-GHz RF Receiver Characteristics for 490 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 470 | — | 510 | dBm |
| Max usable input level, 0.1% BER | $SAT_{2k4}$ | Desired is reference 2.4 kbps GFSK signal[3] | — | 10 | — | dBm |
| Max usable input level, 0.1% BER | $SAT_{38k4}$ | Desired is reference 38.4 kbps GFSK signal[4] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps GFSK signal[3], 0.1% BER | — | -122.2 | — | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C | — | -111.4 | -108.9 | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[4], 0.1% BER, T > 85 °C | — | — | -107.9 | dBm |
| | | Desired is reference 10 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C | — | -116.8 | -113.9 | dBm |
| | | Desired is reference 10 kbps GFSK signal[2], 0.1% BER, T > 85 °C | — | — | -113.2 | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C | — | -107.3 | -104.7 | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C | — | — | -104 | dBm |
| Level above which RFSENSE will trigger[5] | $RFSENSE_{TRIG}$ | Desired is reference 100 kbps GFSK signal[1], 0.1% BER | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[5] | $RFSENSE_{THRES}$ | CW at 490 MHz | — | -50 | — | dBm |
| Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing | $C/I_1$ | Desired is 2.4 kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER | 48 | 60.3 | — | dB |
| | | Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | 38.3 | 45.6 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing | $C/I_2$ | Desired is 2.4kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER | — | 60.4 | — | dB |
| | | Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 52.6 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 2.4kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER | — | 56.5 | — | dB |
| | | Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 54.1 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[3] at 3 dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 73.9 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 75.4 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 90.2 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -53 | -47 | dBm |
| | | 1 GHz to 12 GHz | — | -53 | -47 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz.
2. Definition of reference signal is 10 kbps 2GFSK, BT=0.5, Δf = 5 kHz, RX channel BW = 20.038 kHz.
3. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
4. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
5. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.10.7 Sub-GHz RF Transmitter characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 433 MHz.

**Table 4.24. Sub-GHz RF Transmitter characteristics for 433 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 426 | — | 445 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA supply connected to DC-DC output, 14dBm output power | 12.5 | 15.1 | 17.4 | dBm |
| | | External PA supply connected to DC-DC output, 10dBm output power | 8.3 | 10.6 | 13.3 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | — | -42 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply, peak to peak, Pout = 10dBm | $POUT_{VAR_V}$ | At 10 dBm;1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = DC-DC output, T = 25 °C | — | 1.7 | — | dB |
| Output power variation vs temperature, peak to peak, Pout= 10dBm | $POUT_{VAR_T}$ | -40 to +85C at 10dBm | — | 0.5 | 1.2 | dB |
| | | -40 to +125C at 10dBm | — | 0.7 | 1.7 | dB |
| Output power variation vs RF frequency, Pout = 10dBm | $POUT_{VAR_F}$ | T = 25 °C | — | 0.1 | 0.2 | dB |
| Spurious emissions of harmonics FCC, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz | $SPUR_{HARM_FCC}$ | In restricted bands, per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |
| | | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| Spurious emissions out-of-band FCC, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz | $SPUR_{OOB_FCC}$ | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209 | — | -52 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209 | — | -61 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209 | — | -58 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |
| Spurious emissions of harmonics ETSI, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz | $SPUR_{HARM_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies below 1Ghz) | — | -42 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1Ghz) | — | -36 | -30 | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurious emissions out-of-band ETSI, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz | $SPUR_{OOB_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -60 | -54 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) | — | -42 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) | — | -36 | -30 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.10.8 Sub-GHz RF Receiver Characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 433 MHz.

**Table 4.25. Sub-GHz RF Receiver Characteristics for 433 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 426 | — | 445 | MHz |
| Max usable input level, 0.1% BER | $SAT_{2k4}$ | Desired is reference 2.4 kbps GFSK signal[2] | — | 10 | — | dBm |
| Max usable input level, 0.1% BER | $SAT_{50k}$ | Desired is reference 50 kbps GFSK signal[4] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 4.8 kbps OOK signal[3], 20% PER | — | -109.9 | — | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C | — | -107.3 | -105 | dBm |
| | | Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C | — | — | -104 | dBm |
| | | Desired is reference 50 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C | — | -110.3 | -107.2 | dBm |
| | | Desired is reference 50 kbps GFSK signal[4], 0.1% BER, T > 85 °C | — | — | -106.6 | dBm |
| | | Desired is reference 2.4 kbps GFSK signal[2], 0.1% BER | — | -123.1 | — | dBm |
| | | Desired is reference 9.6 kbps GFSK signal[5], 1% PER, T ≤ 85 °C | — | -112.6 | -109 | dBm |
| | | Desired is reference 9.6 kbps GFSK signal[5], 1% PER, T > 85 °C | — | — | -108 | dBm |
| Level above which RFSENSE will trigger[6] | $RFSENSE_{TRIG}$ | CW at 433 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[6] | $RFSENSE_{THRES}$ | CW at 433 MHz | — | -50 | — | dBm |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing | $C/I_1$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 51.6 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | 35 | 44.1 | — | dB |
| | | Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | 47 | 61.5 | — | dB |
| | | Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | 45.6 | 53.1 | — | dB |
| | | Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER | — | 35.7 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing | $C/I_2$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 61.5 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 54.6 | — | dB |
| | | Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 62.4 | — | dB |
| | | Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 58.1 | — | dB |
| | | Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER | — | 50.6 | — | dB |
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER | — | 46.5 | — | dB |
| | | Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 51.7 | — | dB |
| | | Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 57.5 | — | dB |
| | | Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER | — | 54.4 | — | dB |
| | | Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER | — | 48 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 75.7 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 77.2 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | — | 92 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Intermod selectivity, 0.1% BER. CW interferers at 12.5 kHz and 25 kHz offsets | $C/I_{IM}$ | Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level | — | 58.8 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -55 | -49 | dBm |
| | | Above 960 MHz | — | -47 | -41 | dBm |
| Max spurious emissions during active receive mode, per ETSI 300-220 Section 8.6 | $SPUR_{RX_ETSI}$ | Below 1000 MHz | — | -63 | -57 | dBm |
| | | Above 1000 MHz | — | -53 | -47 | dBm |
| Max spurious emissions during active receive mode, per ARIB STD T67 Section 3.3(5) | $SPUR_{RX_ARIB}$ | Below 710 MHz, RBW=100kHz | — | -60 | -54 | dBm |

**Note:**

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz, channel spacing = 200 kHz.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
3. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 306.036 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 99.012 kHz, channel spacing = 200 kHz.
5. Definition of reference signal is 9.6 kbps 4GFSK, BT=0.5, inner deviation = 0.8 kHz, RX channel BW = 8.5 kHz, channel spacing = 12.5 kHz.
6. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.10.9 Sub-GHz RF Transmitter characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 315 MHz.

**Table 4.26. Sub-GHz RF Transmitter characteristics for 315 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 195 | — | 358 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA supply connected to DC-DC output | 13.8 | 17.2 | 21.1 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | | -43.9 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = DC-DC output, T = 25 °C | — | 1.8 | — | dB |
| Output power variation vs temperature | $POUT_{VAR_T}$ | -40 to +85C | — | 0.5 | 1.2 | dB |
| | | -40 to +125C | — | 0.7 | 1.5 | dB |
| Output power variation vs RF frequency | $POUT_{VAR_F}$ | T = 25 °C | — | 0.1 | 0.7 | dB |
| Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 303 MHz | $SPUR_{HARM_FCC}$ | In restricted bands, per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |
| | | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 303 MHz | $SPUR_{OOB_FCC}$ | In non-restricted bands, per FCC Part 15.231 | — | -26 | -20 | dBc |
| | | In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209 | — | -52 | -46 | dBm |
| | | In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209 | — | -61 | -56 | dBm |
| | | In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209 | — | -58 | -52 | dBm |
| | | In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209 | — | -47 | -42 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

Not Recommended For New Designs

#### 4.1.10.10 Sub-GHz RF Receiver Characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 315 MHz.

**Table 4.27. Sub-GHz RF Receiver Characteristics for 315 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 195 | — | 358 | dBm |
| Max usable input level, 0.1% BER | $SAT_{2k4}$ | Desired is reference 2.4 kbps GFSK signal[1] | — | 10 | — | dBm |
| Max usable input level, 0.1% BER | $SAT_{38k4}$ | Desired is reference 38.4 kbps GFSK signal[2] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C | — | -123.2 | -120.7 | dBm |
| | | Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER, T > 85 °C | — | — | -120 | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C | — | -111.4 | -108.6 | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C | — | — | -107.9 | dBm |
| | | Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T ≤ 85 °C | — | -98.8 | -95.5 | dBm |
| | | Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T > 85 °C | — | — | -94.5 | dBm |
| Level above which RFSENSE will trigger[4] | $RFSENSE_{TRIG}$ | CW at 315 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[4] | $RFSENSE_{THRES}$ | CW at 315 MHz | — | -50 | — | dBm |
| Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing | $C/I_1$ | Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | 54.1 | 63.6 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 49.9 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing | $C/I_2$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 64.2 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level[2], 0.1% BER | — | 56.2 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 53 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 51.4 | — | dB |
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 75 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 76.5 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | 72.6 | 91.9 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode, per FCC Part 15.109(a) | $SPUR_{RX_FCC}$ | 216-960 MHz | — | -63 | -57 | dBm |
| | | Above 960MHz | — | -53 | -47 | dBm |

**Note:**

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

Not Recommended For New Designs

#### 4.1.10.11 Sub-GHz RF Transmitter Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 169 MHz.

**Table 4.28. Sub-GHz RF Transmitter Characteristics for 169 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RF tuning frequency range | $F_{RANGE}$ | | 169 | — | 170 | MHz |
| Maximum TX Power[1] | $POUT_{MAX}$ | External PA supply = 3.3 V | 18.1 | 19.7 | 22.4 | dBm |
| Minimum active TX Power | $POUT_{MIN}$ | | | -42.6 | — | dBm |
| Output power step size | $POUT_{STEP}$ | output power > 0 dBm | — | 0.5 | — | dB |
| Output power variation vs supply, peak to peak | $POUT_{VAR_V}$ | 1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = 3.3 V, T = 25 °C | — | 4.8 | 5.0 | dB |
| Output power variation vs temperature, peak to peak | $POUT_{VAR_T}$ | -40 to +85 °C at 20 dBm | — | 0.6 | 1.2 | dB |
| | | -40 to +125 °C at 20 dBm | — | 0.8 | 1.5 | dB |
| Spurious emissions of harmonics, Conducted measurement, External PA supply = 3.3 V, Test Frequency = 169 MHz | $SPUR_{HARM_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -42 | — | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)[2] | — | -38 | — | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)[2] | — | -36 | — | dBm |
| Spurious emissions out-of-band, Conducted measurement, External PA supply = 3.3 V, Test Frequency = 169 MHz | $SPUR_{OOB_ETSI}$ | Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) | — | -42 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) | — | -42 | -36 | dBm |
| | | Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) | — | -36 | -30 | dBm |

**Note:**

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. Typical value marginally passes specification. Additional margin can be obtained by increasing the order of the harmonic filter.

Not Recommended For New Designs

#### 4.1.10.12 Sub-GHz RF Receiver Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 169 MHz.

**Table 4.29. Sub-GHz RF Receiver Characteristics for 169 MHz Band**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Tuning frequency range | $F_{RANGE}$ | | 169 | — | 170 | dBm |
| Max usable input level, 0.1% BER | $SAT_{2k4}$ | Desired is reference 2.4 kbps GFSK signal[1] | — | 10 | — | dBm |
| Max usable input level, 0.1% BER | $SAT_{38k4}$ | Desired is reference 38.4 kbps GFSK signal[2] | — | 10 | — | dBm |
| Sensitivity | SENS | Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER | — | -124 | — | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C | — | -112.2 | -108 | dBm |
| | | Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C | — | — | -107 | dBm |
| | | Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T ≤ 85 °C | — | -99.2 | -96 | dBm |
| | | Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T > 85 °C | — | — | -95 | dBm |
| Level above which RFSENSE will trigger[4] | $RFSENSE_{TRIG}$ | CW at 169 MHz | — | -28.1 | — | dBm |
| Level below which RFSENSE will not trigger[4] | $RFSENSE_{THRES}$ | CW at 169 MHz | — | -50 | — | dBm |
| Adjacent channel selectivity, Interferer is CW at ± 1 x channel-spacing | $C/I_1$ | Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 64.8 | — | dB |
| | | Desired is 38.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | 43.3 | 51.4 | — | dB |
| Alternate channel selectivity, Interferer is CW at ± 2 x channel-spacing | $C/I_2$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 67.4 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 60.6 | — | dB |
| Image rejection, Interferer is CW at image frequency | $C/I_{IMAGE}$ | Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER | — | 47.1 | — | dB |
| | | Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER | — | 47.1 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level | $C/I_{BLOCKER}$ | Interferer CW at Desired ± 1 MHz | — | 73.4 | — | dB |
| | | Interferer CW at Desired ± 2 MHz | — | 75 | — | dB |
| | | Interferer CW at Desired ± 10 MHz | 80 | 90.1 | — | dB |
| Upper limit of input power range over which RSSI resolution is maintained | $RSSI_{MAX}$ | | — | — | 5 | dBm |
| Lower limit of input power range over which RSSI resolution is maintained | $RSSI_{MIN}$ | | -98 | — | — | dBm |
| RSSI resolution | $RSSI_{RES}$ | Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range | — | 0.25 | — | dBm |
| Max spurious emissions during active receive mode | $SPUR_{RX}$ | 30 MHz to 1 GHz | — | -63 | -57 | dBm |
| | | 1 GHz to 12 GHz | — | -53 | -47 | dBm |

**Note:**

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

### 4.1.11 Modem

**Table 4.30. Modem**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receive bandwidth | $BW_{RX}$ | Configurable range with 38.4 MHz crystal | 0.1 | — | 2530 | kHz |
| IF frequency | $f_{IF}$ | Configurable range with 38.4 MHz crystal. Selected steps available. | 150 | — | 1371 | kHz |
| DSSS symbol length | $SL_{DSSS}$ | Configurable in steps of 1 chip | 2 | — | 32 | chips |
| DSSS bits per symbol | $BPS_{DSSS}$ | Configurable | 1 | — | 4 | bits/ symbol |

Not Recommended For New Designs

### 4.1.12 Oscillators

#### 4.1.12.1 Low-Frequency Crystal Oscillator (LFXO)

**Table 4.31. Low-Frequency Crystal Oscillator (LFXO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal frequency | $f_{LFXO}$ | | — | 32.768 | — | kHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{LFXO}$ | | — | — | 70 | kΩ |
| Supported range of crystal load capacitance [1] | $C_{LFXO_CL}$ | | 6 | — | 18 | pF |
| On-chip tuning cap range [2] | $C_{LFXO_T}$ | On each of LFXTAL_N and LFXTAL_P pins | 8 | — | 40 | pF |
| On-chip tuning cap step size | $SS_{LFXO}$ | | — | 0.25 | — | pF |
| Current consumption after startup [3] | $I_{LFXO}$ | ESR = 70 kOhm, $C_L$ = 7 pF, GAIN[4] = 2, AGC[4] = 1 | — | 273 | — | nA |
| Start- up time | $t_{LFXO}$ | ESR = 70 kOhm, $C_L$ = 7 pF, GAIN[4] = 2 | — | 308 | — | ms |

**Note:**

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{LFXO_T}$ /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

Not Recommended For New Designs

#### 4.1.12.2 High-Frequency Crystal Oscillator (HFXO)

**Table 4.32. High-Frequency Crystal Oscillator (HFXO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal frequency | $f_{HFXO}$ | 38.4 MHz required for radio transceiver operation | 38 | 38.4 | 40 | MHz |
| Supported crystal equivalent series resistance (ESR) | $ESR_{HFXO_38M4}$ | Crystal frequency 38.4 MHz | — | — | 60 | Ω |
| Supported range of crystal load capacitance [1] | $C_{HFXO_CL}$ | | 6 | — | 12 | pF |
| On-chip tuning cap range [2] | $C_{HFXO_T}$ | On each of HFXTAL_N and HFXTAL_P pins | 9 | 20 | 25 | pF |
| On-chip tuning capacitance step | $SS_{HFXO}$ | | — | 0.04 | — | pF |
| Startup time | $t_{HFXO}$ | 38.4 MHz, ESR = 50 Ohm, $C_L$ = 10 pF | — | 300 | — | µs |
| Frequency tolerance for the crystal | $FT_{HFXO}$ | 38.4 MHz, ESR = 50 Ohm, $C_L$ = 10 pF | -40 | — | 40 | ppm |

**Note:**
1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{HFXO_T}$ /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

#### 4.1.12.3 Low-Frequency RC Oscillator (LFRCO)

**Table 4.33. Low-Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{LFRCO}$ | ENVREF[2] = 1, T ≤ 85 °C | 31.3 | 32.768 | 33.6 | kHz |
| | | ENVREF[2] = 1, T > 85 °C | 31.6 | 32.768 | 36.8 | kHz |
| | | ENVREF[2] = 0, T ≤ 85 °C | 31.3 | 32.768 | 33.4 | kHz |
| | | ENVREF[2] = 0, T > 85 °C | 30 | 32.768 | 33.4 | kHz |
| Startup time | $t_{LFRCO}$ | | — | 500 | — | µs |
| Current consumption [1] | $I_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | — | 342 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 494 | — | nA |

**Note:**
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

Not Recommended For New Designs

#### 4.1.12.4 High-Frequency RC Oscillator (HFRCO)

**Table 4.34. High-Frequency RC Oscillator (HFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency accuracy | $f_{HFRCO_ACC}$ | At production calibrated frequencies, across supply voltage and temperature | -2.5 | — | 2.5 | % |
| Start-up time | $t_{HFRCO}$ | $f_{HFRCO} \geq 19$ MHz | — | 300 | — | ns |
| | | $4 < f_{HFRCO} < 19$ MHz | — | 1 | — | µs |
| | | $f_{HFRCO} \leq 4$ MHz | — | 2.5 | — | µs |
| Current consumption on all supplies | $I_{HFRCO}$ | $f_{HFRCO}$ = 38 MHz | — | 231 | 260 | µA |
| | | $f_{HFRCO}$ = 32 MHz | — | 193 | 218 | µA |
| | | $f_{HFRCO}$ = 26 MHz | — | 165 | 186 | µA |
| | | $f_{HFRCO}$ = 19 MHz | — | 137 | 155 | µA |
| | | $f_{HFRCO}$ = 16 MHz | — | 118 | 131 | µA |
| | | $f_{HFRCO}$ = 13 MHz | — | 106 | 119 | µA |
| | | $f_{HFRCO}$ = 7 MHz | — | 83 | 94 | µA |
| | | $f_{HFRCO}$ = 4 MHz | — | 31 | 40 | µA |
| | | $f_{HFRCO}$ = 2 MHz | — | 27 | 37 | µA |
| | | $f_{HFRCO}$ = 1 MHz | — | 25 | 35 | µA |
| Coarse trim step size (% of period) | $SS_{HFRCO_COARSE}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{HFRCO_FINE}$ | | — | 0.1 | — | % |
| Period jitter | $PJ_{HFRCO}$ | | — | 0.2 | — | % RMS |
| Frequency limits | $f_{HFRCO_BAND}$ | FREQRANGE = 0, FINETUNINGEN = 0 | 3.47 | — | 6.15 | MHz |
| | | FREQRANGE = 3, FINETUNINGEN = 0 | 6.24 | — | 11.45 | MHz |
| | | FREQRANGE = 6, FINETUNINGEN = 0 | 11.3 | — | 19.8 | MHz |
| | | FREQRANGE = 7, FINETUNINGEN = 0 | 13.45 | — | 22.8 | MHz |
| | | FREQRANGE = 8, FINETUNINGEN = 0 | 16.5 | — | 29.0 | MHz |
| | | FREQRANGE = 10, FINETUNINGEN = 0 | 23.11 | — | 40.63 | MHz |
| | | FREQRANGE = 11, FINETUNINGEN = 0 | 27.27 | — | 48 | MHz |
| | | FREQRANGE = 12, FINETUNINGEN = 0 | 33.33 | — | 54 | MHz |

Not Recommended For New Designs

#### 4.1.12.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

**Table 4.35. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency accuracy | $f_{AUXHFRCO_ACC}$ | At production calibrated frequencies, across supply voltage and temperature | -3 | — | 3 | % |
| Start-up time | $t_{AUXHFRCO}$ | $f_{AUXHFRCO} \geq 19$ MHz | — | 400 | — | ns |
| | | $4 < f_{AUXHFRCO} < 19$ MHz | — | 1.4 | — | µs |
| | | $f_{AUXHFRCO} \leq 4$ MHz | — | 2.5 | — | µs |
| Current consumption on all supplies | $I_{AUXHFRCO}$ | $f_{AUXHFRCO}$ = 38 MHz | — | 237 | 265 | µA |
| | | $f_{AUXHFRCO}$ = 32 MHz | — | 194 | 218 | µA |
| | | $f_{AUXHFRCO}$ = 26 MHz | — | 165 | 186 | µA |
| | | $f_{AUXHFRCO}$ = 19 MHz | — | 131 | 148 | µA |
| | | $f_{AUXHFRCO}$ = 16 MHz | — | 119 | 134 | µA |
| | | $f_{AUXHFRCO}$ = 13 MHz | — | 92 | 104 | µA |
| | | $f_{AUXHFRCO}$ = 7 MHz | — | 61 | 70 | µA |
| | | $f_{AUXHFRCO}$ = 4 MHz | — | 34 | 42 | µA |
| | | $f_{AUXHFRCO}$ = 2 MHz | — | 29 | 37 | µA |
| | | $f_{AUXHFRCO}$ = 1 MHz | — | 26 | 34 | µA |
| Coarse trim step size (% of period) | $SS_{AUXHFRCO_COARSE}$ | | — | 0.8 | — | % |
| Fine trim step size (% of period) | $SS_{AUXHFRCO_FINE}$ | | — | 0.1 | — | % |
| Period jitter | $PJ_{AUXHFRCO}$ | | — | 0.2 | — | % RMS |

#### 4.1.12.6 Ultra-low Frequency RC Oscillator (ULFRCO)

**Table 4.36. Ultra-low Frequency RC Oscillator (ULFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{ULFRCO}$ | | 0.95 | 1 | 1.07 | kHz |

Not Recommended For New Designs

### 4.1.13 Flash Memory Characteristics[5]

**Table 4.37. Flash Memory Characteristics[5]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Flash erase cycles before failure | $EC_{FLASH}$ | | 10000 | — | — | cycles |
| Flash data retention | $RET_{FLASH}$ | T ≤ 85 °C | 10 | — | — | years |
| | | T ≤ 125 °C | 10 | — | — | years |
| Word (32-bit) programming time | $t_{W_PROG}$ | Burst write, 128 words, average time per word | 20 | 26.1 | 30 | µs |
| | | Single word | 60 | 68.5 | 80 | µs |
| Page erase time[4] | $t_{PERASE}$ | | 20 | 28.8 | 40 | ms |
| Mass erase time[1] | $t_{MERASE}$ | | 20 | 28.7 | 40 | ms |
| Device erase time[2] [3] | $t_{DERASE}$ | T ≤ 85 °C | — | 54.4 | 70 | ms |
| | | T ≤ 125 °C | — | 54.4 | 75 | ms |
| Erase current[6] | $I_{ERASE}$ | Page Erase | — | — | 1.6 | mA |
| Write current[6] | $I_{WRITE}$ | | — | — | 3.5 | mA |
| Supply voltage during flash erase and write | $V_{FLASH}$ | | 1.62 | — | 3.6 | V |

**Note:**

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

Not Recommended For New Designs

### 4.1.14 General-Purpose I/O (GPIO)

**Table 4.38. General-Purpose I/O (GPIO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | GPIO pins | — | — | IOVDD*0.3 | V |
| Input high voltage | $V_{IH}$ | GPIO pins | IOVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | $V_{OH}$ | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | $V_{OL}$ | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | $I_{IOLEAK}$ | All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | 30 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | 50 | nA |
| | | All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C | — | — | 110 | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T > 85 °C | — | — | 250 | nA |
| Input leakage current on 5VTOL pads above IOVDD | $I_{5VTOLLEAK}$ | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | 15 | µA |
| I/O pin pull-up/pull-down resistor | $R_{PUD}$ | | 30 | 40 | 65 | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 15 | 25 | 45 | ns |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output fall time, From 70% to 30% of $V_{IO}$ | $t_{IOOF}$ | $C_L$ = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6 | — | 1.8 | — | ns |
| | | $C_L$ = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6 | — | 4.5 | — | ns |
| Output rise time, From 30% to 70% of $V_{IO}$ | $t_{IOOR}$ | $C_L$ = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1] | — | 2.2 | — | ns |
| | | $C_L$ = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6 | — | 7.4 | — | ns |

**Note:**
1. In GPIO_Pn_CTRL register.

Not Recommended For New Designs

### 4.1.15 Voltage Monitor (VMON)

**Table 4.39. Voltage Monitor (VMON)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current (including I_SENSE) | $I_{VMON}$ | In EM0 or EM1, 1 supply monitored, T ≤ 85 °C | — | 6.3 | 8 | µA |
| | | In EM0 or EM1, 1 supply monitored, T > 85 °C | — | — | 11 | µA |
| | | In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C | — | 12.5 | 15 | µA |
| | | In EM0 or EM1, 4 supplies monitored, T > 85 °C | — | — | 18 | µA |
| | | In EM2, EM3 or EM4, 1 supply monitored and above threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 1 supply monitored and below threshold | — | 62 | — | nA |
| | | In EM2, EM3 or EM4, 4 supplies monitored and all above threshold | — | 99 | — | nA |
| | | In EM2, EM3 or EM4, 4 supplies monitored and all below threshold | — | 99 | — | nA |
| Loading of monitored supply | $I_{SENSE}$ | In EM0 or EM1 | — | 2 | — | µA |
| | | In EM2, EM3 or EM4 | — | 2 | — | nA |
| Threshold range | $V_{VMON_RANGE}$ | | 1.62 | — | 3.4 | V |
| Threshold step size | $N_{VMON_STESP}$ | Coarse | — | 200 | — | mV |
| | | Fine | — | 20 | — | mV |
| Response time | $t_{VMON_RES}$ | Supply drops at 1V/µs rate | — | 460 | — | ns |
| Hysteresis | $V_{VMON_HYST}$ | | — | 26 | — | mV |

Not Recommended For New Designs

### 4.1.16 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

**Table 4.40. Analog to Digital Converter (ADC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | $V_{RESOLUTION}$ | | 6 | — | 12 | Bits |
| Input voltage range[5] | $V_{ADCIN}$ | Single ended | — | — | $V_{FS}$ | V |
| | | Differential | $-V_{FS}/2$ | — | $V_{FS}/2$ | V |
| Input range of external reference voltage, single ended and differential | $V_{ADCREFIN_P}$ | | 1 | — | $V_{AVDD}$ | V |
| Power supply rejection[2] | $PSRR_{ADC}$ | At DC | — | 80 | — | dB |
| Analog input common mode rejection ratio | $CMRR_{ADC}$ | At DC | — | 80 | — | dB |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[4] = KEEPADCWARM | $I_{ADC_CONTINUOUS_LP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3] | — | 270 | 304 | µA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3] | — | 125 | — | µA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3] | — | 80 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL | $I_{ADC_NORMAL_LP}$ | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3] | — | 45 | — | µA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3] | — | 8 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC | $I_{ADC_STANDBY_LP}$ | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3] | — | 105 | — | µA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3] | — | 70 | — | µA |
| Current from all supplies, using internal reference buffer. Continuous operation. WARMUPMODE[4] = KEEPADCWARM | $I_{ADC_CONTINUOUS_HP}$ | 1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3] | — | 325 | — | µA |
| | | 250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3] | — | 175 | — | µA |
| | | 62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3] | — | 125 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL | $I_{ADC_NORMAL_HP}$ | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3] | — | 85 | — | µA |
| | | 5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3] | — | 16 | — | µA |
| Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC | $I_{ADC_STANDBY_HP}$ | 125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3] | — | 160 | — | µA |
| | | 35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3] | — | 125 | — | µA |
| Current from HFPERCLK | $I_{ADC_CLK}$ | HFPERCLK = 16 MHz | — | 150 | — | µA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC clock frequency | $f_{ADCCLK}$ | | — | — | 16 | MHz |
| Throughput rate | $f_{ADCRATE}$ | | — | — | 1 | Msps |
| Conversion time[1] | $t_{ADCCONV}$ | 6 bit | — | 7 | — | cycles |
| | | 8 bit | — | 9 | — | cycles |
| | | 12 bit | — | 13 | — | cycles |
| Startup time of reference generator and ADC core | $t_{ADCSTART}$ | WARMUPMODE[4] = NORMAL | — | — | 5 | µs |
| | | WARMUPMODE[4] = KEEPIN-STANDBY | — | — | 2 | µs |
| | | WARMUPMODE[4] = KEEPINSLO-WACC | — | — | 1 | µs |
| SNDR at 1Msps and $f_{IN}$ = 10kHz | $SNDR_{ADC}$ | Internal reference[7], differential measurement | 58 | 67 | — | dB |
| | | External reference[6], differential measurement | — | 68 | — | dB |
| Spurious-free dynamic range (SFDR) | $SFDR_{ADC}$ | 1 MSamples/s, 10 kHz full-scale sine wave | — | 75 | — | dB |
| Differential non-linearity (DNL) | $DNL_{ADC}$ | 12 bit resolution, No missing co-des | -1 | — | 2 | LSB |
| Integral non-linearity (INL), End point method | $INL_{ADC}$ | 12 bit resolution | -6 | — | 6 | LSB |
| Offset error | $V_{ADCOFFSETERR}$ | | -3 | 0 | 3 | LSB |
| Gain error in ADC | $V_{ADCGAIN}$ | Using internal reference | — | -0.2 | 3.5 | % |
| | | Using external reference | — | -1 | — | % |
| Temperature sensor slope | $V_{TS_SLOPE}$ | | — | -1.84 | — | mV/°C |

**Note:**

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

Not Recommended For New Designs

### 4.1.17 Analog Comparator (ACMP)

**Table 4.41. Analog Comparator (ACMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{ACMPIN}$ | ACMPVDD = ACMPn_CTRL_PWRSEL [1] | — | — | $V_{ACMPVDD}$ | V |
| Supply voltage | $V_{ACMPVDD}$ | BIASPROG[4] ≤ 0x10 or FULLBIAS[4] = 0 | 1.8 | — | $V_{VREGVDD_MAX}$ | V |
| | | 0x10 < BIASPROG[4] ≤ 0x20 and FULLBIAS[4] = 1 | 2.1 | — | $V_{VREGVDD_MAX}$ | V |
| Active current not including voltage reference[2] | $I_{ACMP}$ | BIASPROG[4] = 1, FULLBIAS[4] = 0 | — | 50 | — | nA |
| | | BIASPROG[4] = 0x10, FULLBIAS[4] = 0 | — | 306 | — | nA |
| | | BIASPROG[4] = 0x02, FULLBIAS[4] = 1 | — | 6.1 | 10 | µA |
| | | BIASPROG[4] = 0x20, FULLBIAS[4] = 1 | — | 74 | 92 | µA |
| Current consumption of internal voltage reference[2] | $I_{ACMPREF}$ | VLP selected as input using 2.5 V Reference / 4 (0.625 V) | — | 50 | — | nA |
| | | VLP selected as input using VDD | — | 20 | — | nA |
| | | VBDIV selected as input using 1.25 V reference / 1 | — | 4.1 | — | µA |
| | | VADIV selected as input using VDD/1 | — | 2.4 | — | µA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Hysteresis ($V_{CM}$ = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1) | $V_{ACMPHYST}$ | HYSTSEL[5] = HYST0 | -3 | 0 | 3 | mV |
| | | HYSTSEL[5] = HYST1 | 5 | 18 | 27 | mV |
| | | HYSTSEL[5] = HYST2 | 12 | 33 | 50 | mV |
| | | HYSTSEL[5] = HYST3 | 17 | 46 | 67 | mV |
| | | HYSTSEL[5] = HYST4 | 23 | 57 | 86 | mV |
| | | HYSTSEL[5] = HYST5 | 26 | 68 | 104 | mV |
| | | HYSTSEL[5] = HYST6 | 30 | 79 | 130 | mV |
| | | HYSTSEL[5] = HYST7 | 34 | 90 | 155 | mV |
| | | HYSTSEL[5] = HYST8 | -3 | 0 | 3 | mV |
| | | HYSTSEL[5] = HYST9 | -27 | -18 | -5 | mV |
| | | HYSTSEL[5] = HYST10 | -50 | -33 | -12 | mV |
| | | HYSTSEL[5] = HYST11 | -67 | -45 | -17 | mV |
| | | HYSTSEL[5] = HYST12 | -86 | -57 | -23 | mV |
| | | HYSTSEL[5] = HYST13 | -104 | -67 | -26 | mV |
| | | HYSTSEL[5] = HYST14 | -130 | -78 | -30 | mV |
| | | HYSTSEL[5] = HYST15 | -155 | -88 | -34 | mV |
| Comparator delay[3] | $t_{ACMPDELAY}$ | BIASPROG[4] = 1, FULLBIAS[4] = 0 | — | 30 | 95 | µs |
| | | BIASPROG[4] = 0x10, FULLBIAS[4] = 0 | — | 3.7 | 10 | µs |
| | | BIASPROG[4] = 0x02, FULLBIAS[4] = 1 | — | 360 | 1000 | ns |
| | | BIASPROG[4] = 0x20, FULLBIAS[4] = 1 | — | 35 | — | ns |
| Offset voltage | $V_{ACMPOFFSET}$ | BIASPROG[4] =0x10, FULLBIAS[4] = 1 | -35 | — | 35 | mV |
| Reference voltage | $V_{ACMPREF}$ | Internal 1.25 V reference | 1 | 1.25 | 1.47 | V |
| | | Internal 2.5 V reference | 1.98 | 2.5 | 2.8 | V |
| Capacitive sense internal resistance | $R_{CSRES}$ | CSRESSEL[6] = 0 | — | infinite | — | kΩ |
| | | CSRESSEL[6] = 1 | — | 15 | — | kΩ |
| | | CSRESSEL[6] = 2 | — | 27 | — | kΩ |
| | | CSRESSEL[6] = 3 | — | 39 | — | kΩ |
| | | CSRESSEL[6] = 4 | — | 51 | — | kΩ |
| | | CSRESSEL[6] = 5 | — | 102 | — | kΩ |
| | | CSRESSEL[6] = 6 | — | 164 | — | kΩ |
| | | CSRESSEL[6] = 7 | — | 239 | — | kΩ |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

Not Recommended For New Designs

### 4.1.18 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

**Table 4.42. Digital to Analog Converter (VDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{DACOUT}$ | Single-Ended | 0 | — | $V_{VREF}$ | V |
| | | Differential[2] | $-V_{VREF}$ | — | $V_{VREF}$ | V |
| Current consumption including references (2 channels)[1] | $I_{DAC}$ | 500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4 | — | 396 | — | µA |
| | | 44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4 | — | 72 | — | µA |
| | | 200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02 | — | 1.2 | — | µA |
| Current from HFPERCLK[4] | $I_{DAC_CLK}$ | | — | 5 | — | µA/MHz |
| Sample rate | $SR_{DAC}$ | | — | — | 500 | ksps |
| DAC clock frequency | $f_{DAC}$ | | — | — | 1 | MHz |
| Conversion time | $t_{DACCONV}$ | $f_{DAC}$ = 1MHz | 2 | — | — | µs |
| Settling time | $t_{DACSETTLE}$ | 50% fs step settling to 5 LSB | — | 2.5 | — | µs |
| Startup time | $t_{DACSTARTUP}$ | Enable to 90% fs output, settling to 10 LSB | — | — | 12 | µs |
| Output impedance | $R_{OUT}$ | DRIVESTRENGTH = 2, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -8 mA < $I_{OUT}$ < 8 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -400 µA < $I_{OUT}$ < 400 µA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 2, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -2 mA < $I_{OUT}$ < 2 mA, Full supply range | — | 2 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -100 µA < $I_{OUT}$ < 100 µA, Full supply range | — | 2 | — | Ω |
| Power supply rejection ratio[6] | PSRR | Vout = 50% fs. DC | — | 65.5 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz | $SNDR_{DAC}$ | 500 ksps, single-ended, internal 1.25V reference | — | 60.4 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 61.6 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 64.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 63.3 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 64.4 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 65.8 | — | dB |
| Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz | $SNDR_{DAC_BAND}$ | 500 ksps, single-ended, internal 1.25V reference | — | 65.3 | — | dB |
| | | 500 ksps, single-ended, internal 2.5V reference | — | 66.7 | — | dB |
| | | 500 ksps, single-ended, 3.3V VDD reference | — | 70.0 | — | dB |
| | | 500 ksps, differential, internal 1.25V reference | — | 67.8 | — | dB |
| | | 500 ksps, differential, internal 2.5V reference | — | 69.0 | — | dB |
| | | 500 ksps, differential, 3.3V VDD reference | — | 68.5 | — | dB |
| Total harmonic distortion | THD | | — | 70.2 | — | dB |
| Differential non-linearity[3] | $DNL_{DAC}$ | | -0.99 | — | 1 | LSB |
| Intergral non-linearity | $INL_{DAC}$ | | -4 | — | 4 | LSB |
| Offset error[5] | $V_{OFFSET}$ | T = 25 °C | -8 | — | 8 | mV |
| | | Across operating temperature range | -25 | — | 25 | mV |
| Gain error[5] | $V_{GAIN}$ | T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -2.5 | — | 2.5 | % |
| | | T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5) | -5 | — | 5 | % |
| | | T = 25 °C, External reference (REFSEL = VDD or EXT) | -1.8 | — | 1.8 | % |
| | | Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN) | -3.5 | — | 3.5 | % |
| | | Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5) | -7.5 | — | 7.5 | % |
| | | Across operating temperature range, External reference (REFSEL = VDD or EXT) | -2.0 | — | 2.0 | % |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External load capactiance, OUTSCALE=0 | $C_{LOAD}$ | | — | — | 75 | pF |

**Note:**

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Not Recommended For New Designs

### 4.1.19 Current Digital to Analog Converter (IDAC)

**Table 4.43. Current Digital to Analog Converter (IDAC)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Number of ranges | $N_{IDAC_RANGES}$ | | — | 4 | — | ranges |
| Output current | $I_{IDAC_OUT}$ | RANGSEL[1] = RANGE0 | 0.05 | — | 1.6 | µA |
| | | RANGSEL[1] = RANGE1 | 1.6 | — | 4.7 | µA |
| | | RANGSEL[1] = RANGE2 | 0.5 | — | 16 | µA |
| | | RANGSEL[1] = RANGE3 | 2 | — | 64 | µA |
| Linear steps within each range | $N_{IDAC_STEPS}$ | | — | 32 | — | steps |
| Step size | $SS_{IDAC}$ | RANGSEL[1] = RANGE0 | — | 50 | — | nA |
| | | RANGSEL[1] = RANGE1 | — | 100 | — | nA |
| | | RANGSEL[1] = RANGE2 | — | 500 | — | nA |
| | | RANGSEL[1] = RANGE3 | — | 2 | — | µA |
| Total accuracy, STEPSEL[1] = 0x10 | $ACC_{IDAC}$ | EM0 or EM1, AVDD=3.3 V, T = 25 °C | -3 | — | 3 | % |
| | | EM0 or EM1, Across operating temperature range | -18 | — | 22 | % |
| | | EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C | — | -2 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C | — | -1.7 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.8 | — | % |
| | | EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C | — | -0.7 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C | — | -0.6 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |
| | | EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C | — | -0.5 | — | % |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Start up time | $t_{IDAC_SU}$ | Output within 1% of steady state value | — | 5 | — | µs |
| Settling time, (output settled within 1% of steady state value), | $t_{IDAC_SETTLE}$ | Range setting is changed | — | 5 | — | µs |
| | | Step value is changed | — | 1 | — | µs |
| Current consumption[2] | $I_{IDAC}$ | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | 15 | µA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | 18 | µA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.050 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.075 | — | µA |
| | | EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C | — | 11 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C | — | 13 | — | µA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | $I_{COMP_SRC}$ | RANGESEL1=0, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mv) | — | 0.11 | — | % |
| | | RANGESEL1=1, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mV) | — | 0.06 | — | % |
| | | RANGESEL1=2, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-150 mV) | — | 0.04 | — | % |
| | | RANGESEL1=3, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-250 mV) | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | $I_{COMP_SINK}$ | RANGESEL1=0, output voltage = 100 mV | — | 0.12 | — | % |
| | | RANGESEL1=1, output voltage = 100 mV | — | 0.05 | — | % |
| | | RANGESEL1=2, output voltage = 150 mV | — | 0.04 | — | % |
| | | RANGESEL1=3, output voltage = 250 mV | — | 0.03 | — | % |

**Note:**

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

Not Recommended For New Designs

### 4.1.20 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, $C_{LOAD}$ = 75 pF with OUTSCALE = 0, or $C_{LOAD}$ = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[8] [1].

**Table 4.44. Operational Amplifier (OPAMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (from AVDD) | $V_{OPA}$ | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | $V_{IN}$ | HCMDIS = 0, Rail-to-rail input range | $V_{VSS}$ | — | $V_{OPA}$ | V |
| | | HCMDIS = 1 | $V_{VSS}$ | — | $V_{OPA}$-1.2 | V |
| Input impedance | $R_{IN}$ | | 100 | — | — | MΩ |
| Output voltage | $V_{OUT}$ | | $V_{VSS}$ | — | $V_{OPA}$ | V |
| Load capacitance[2] | $C_{LOAD}$ | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | $R_{OUT}$ | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -8 mA < $I_{OUT}$ < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -400 µA < $I_{OUT}$ < 400 µA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -2 mA < $I_{OUT}$ < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -100 µA < $I_{OUT}$ < 100 µA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | $G_{CL}$ | Buffer connection | 0.99 | 1 | 1.01 | - |
| | | 3x Gain connection | 2.93 | 2.99 | 3.05 | - |
| | | 16x Gain connection | 15.07 | 15.7 | 16.33 | - |
| Active current[4] | $I_{OPA}$ | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | µA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | µA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | µA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | µA |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Open-loop gain | $G_{OL}$ | DRIVESTRENGTH = 3 | — | 135 | — | dB |
| | | DRIVESTRENGTH = 2 | — | 137 | — | dB |
| | | DRIVESTRENGTH = 1 | — | 121 | — | dB |
| | | DRIVESTRENGTH = 0 | — | 109 | — | dB |
| Loop unit-gain frequency[7] | UGF | DRIVESTRENGTH = 3, Buffer connection | — | 3.38 | — | MHz |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 0.9 | — | MHz |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 132 | — | kHz |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 34 | — | kHz |
| | | DRIVESTRENGTH = 3, 3x Gain connection | — | 2.57 | — | MHz |
| | | DRIVESTRENGTH = 2, 3x Gain connection | — | 0.71 | — | MHz |
| | | DRIVESTRENGTH = 1, 3x Gain connection | — | 113 | — | kHz |
| | | DRIVESTRENGTH = 0, 3x Gain connection | — | 28 | — | kHz |
| Phase margin | PM | DRIVESTRENGTH = 3, Buffer connection | — | 67 | — | ° |
| | | DRIVESTRENGTH = 2, Buffer connection | — | 69 | — | ° |
| | | DRIVESTRENGTH = 1, Buffer connection | — | 63 | — | ° |
| | | DRIVESTRENGTH = 0, Buffer connection | — | 68 | — | ° |
| Output voltage noise | $N_{OUT}$ | DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz | — | 146 | — | µVrms |
| | | DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz | — | 163 | — | µVrms |
| | | DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz | — | 170 | — | µVrms |
| | | DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz | — | 176 | — | µVrms |
| | | DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz | — | 313 | — | µVrms |
| | | DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz | — | 271 | — | µVrms |
| | | DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz | — | 247 | — | µVrms |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz | — | 245 | — | µVrms |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slew rate[5] | SR | DRIVESTRENGTH = 3, INCBW=1[3] | — | 4.7 | — | V/µs |
| | | DRIVESTRENGTH = 3, INCBW=0 | — | 1.5 | — | V/µs |
| | | DRIVESTRENGTH = 2, INCBW=1[3] | — | 1.27 | — | V/µs |
| | | DRIVESTRENGTH = 2, INCBW=0 | — | 0.42 | — | V/µs |
| | | DRIVESTRENGTH = 1, INCBW=1[3] | — | 0.17 | — | V/µs |
| | | DRIVESTRENGTH = 1, INCBW=0 | — | 0.058 | — | V/µs |
| | | DRIVESTRENGTH = 0, INCBW=1[3] | — | 0.044 | — | V/µs |
| | | DRIVESTRENGTH = 0, INCBW=0 | — | 0.015 | — | V/µs |
| Startup time[6] | $T_{START}$ | DRIVESTRENGTH = 2 | — | — | 12 | µs |
| Input offset voltage | $V_{OSI}$ | DRIVESTRENGTH = 2 or 3, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 1 or 0, T = 25 °C | -2 | — | 2 | mV |
| | | DRIVESTRENGTH = 2 or 3, across operating temperature range | -12 | — | 12 | mV |
| | | DRIVESTRENGTH = 1 or 0, across operating temperature range | -30 | — | 30 | mV |
| DC power supply rejection ratio[9] | $PSRR_{DC}$ | Input referred | — | 70 | — | dB |
| DC common-mode rejection ratio[9] | $CMRR_{DC}$ | Input referred | — | 70 | — | dB |
| Total harmonic distortion | $THD_{OPA}$ | DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, $V_{OUT}$ = 0.1 V to $V_{OPA}$ - 0.1 V | — | 90 | — | dB |
| | | DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, $V_{OUT}$ = 0.1 V to $V_{OPA}$ - 0.1 V | — | 90 | — | dB |

Not Recommended For New Designs

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 1.5 V. Nominal voltage gain is 3.
2. If the maximum $C_{LOAD}$ is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. Step between 0.2V and $V_{OPA}$-0.2V, 10%-90% rising/falling range.
6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 0.5 V.
9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}$-1.4V to $V_{OPA}$-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

### 4.1.21 Pulse Counter (PCNT)

**Table 4.45. Pulse Counter (PCNT)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input frequency | $F_{IN}$ | Asynchronous Single and Quadrature Modes | — | — | 10 | MHz |
| | | Sampled Modes with Debounce filter set to 0. | — | — | 8 | kHz |

### 4.1.22 Analog Port (APORT)

**Table 4.46. Analog Port (APORT)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply current[2] [1] | $I_{APORT}$ | Operation in EM0/EM1 | — | 7 | — | µA |
| | | Operation in EM2/EM3 | — | 63 | — | nA |

**Note:**

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

Not Recommended For New Designs

### 4.1.23 I2C

#### 4.1.23.1 I2C Standard-mode (Sm)[1]

**Table 4.47. I2C Standard-mode (Sm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 100 | kHz |
| SCL clock low time | $t_{LOW}$ | | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 4 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 250 | — | — | ns |
| SDA hold time[3] | $t_{HD_DAT}$ | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 4.7 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 4 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 4 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 4.7 | — | — | µs |

**Note:**
1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD_DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

Not Recommended For New Designs

#### 4.1.23.2 I2C Fast-mode (Fm)[1]

**Table 4.48. I2C Fast-mode (Fm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL clock low time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 100 | — | — | ns |
| SDA hold time[3] | $t_{HD_DAT}$ | | 100 | — | 900 | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.6 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.6 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | — | — | µs |

**Note:**

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

Not Recommended For New Designs

#### 4.1.23.3 I2C Fast-mode Plus (Fm+)[1]

**Table 4.49. I2C Fast-mode Plus (Fm+)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 1000 | kHz |
| SCL clock low time | $t_{LOW}$ | | 0.5 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.26 | — | — | µs |
| SDA set-up time | $t_{SU_DAT}$ | | 50 | — | — | ns |
| SDA hold time | $t_{HD_DAT}$ | | 100 | — | — | ns |
| Repeated START condition set-up time | $t_{SU_STA}$ | | 0.26 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD_STA}$ | | 0.26 | — | — | µs |
| STOP condition set-up time | $t_{SU_STO}$ | | 0.26 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 0.5 | — | — | µs |

**Note:**
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

Not Recommended For New Designs

### 4.1.24 USART SPI

#### SPI Master Timing

**Table 4.50. SPI Master Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1] [3] [2] | $t_{SCLK}$ | | 2 * $t_{HFPERCLK}$ | — | — | ns |
| CS to MOSI [1] [3] | $t_{CS_MO}$ | | -34 | — | 34 | ns |
| SCLK to MOSI [1] [3] | $t_{SCLK_MO}$ | | -17.5 | — | 17.5 | ns |
| MISO setup time [1] [3] | $t_{SU_MI}$ | IOVDD = 1.62 V | 94 | — | — | ns |
| | | IOVDD = 3.0 V | 48 | — | — | ns |
| MISO hold time [1] [3] | $t_{H_MI}$ | | -9 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

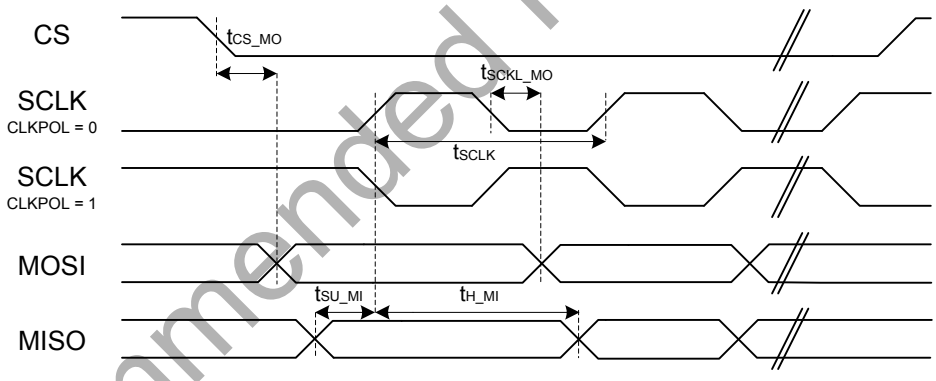


**Figure 4.1. SPI Master Timing Diagram**

Not Recommended For New Designs

### SPI Slave Timing

**Table 4.51. SPI Slave Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1] [3] [2] | $t_{SCLK}$ | | 6 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK high time[1] [3] [2] | $t_{SCLK_HI}$ | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| SCLK low time[1] [3] [2] | $t_{SCLK_LO}$ | | 2.5 * $t_{HFPERCLK}$ | — | — | ns |
| CS active to MISO [1] [3] | $t_{CS_ACT_MI}$ | | 4 | — | 70 | ns |
| CS disable to MISO [1] [3] | $t_{CS_DIS_MI}$ | | 4 | — | 50 | ns |
| MOSI setup time [1] [3] | $t_{SU_MO}$ | | 12.5 | — | — | ns |
| MOSI hold time [1] [3] [2] | $t_{H_MO}$ | | 13 | — | — | ns |
| SCLK to MISO [1] [3] [2] | $t_{SCLK_MI}$ | | 6 + 1.5 * $t_{HFPERCLK}$ | — | 45 + 2.5 * $t_{HFPERCLK}$ | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

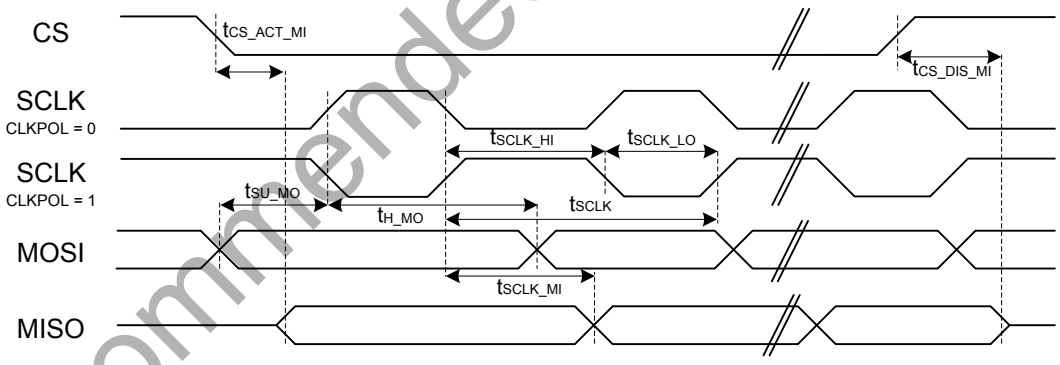


**Figure 4.2. SPI Slave Timing Diagram**

## 4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

Not Recommended For New Designs

### 4.2.1 Supply Current

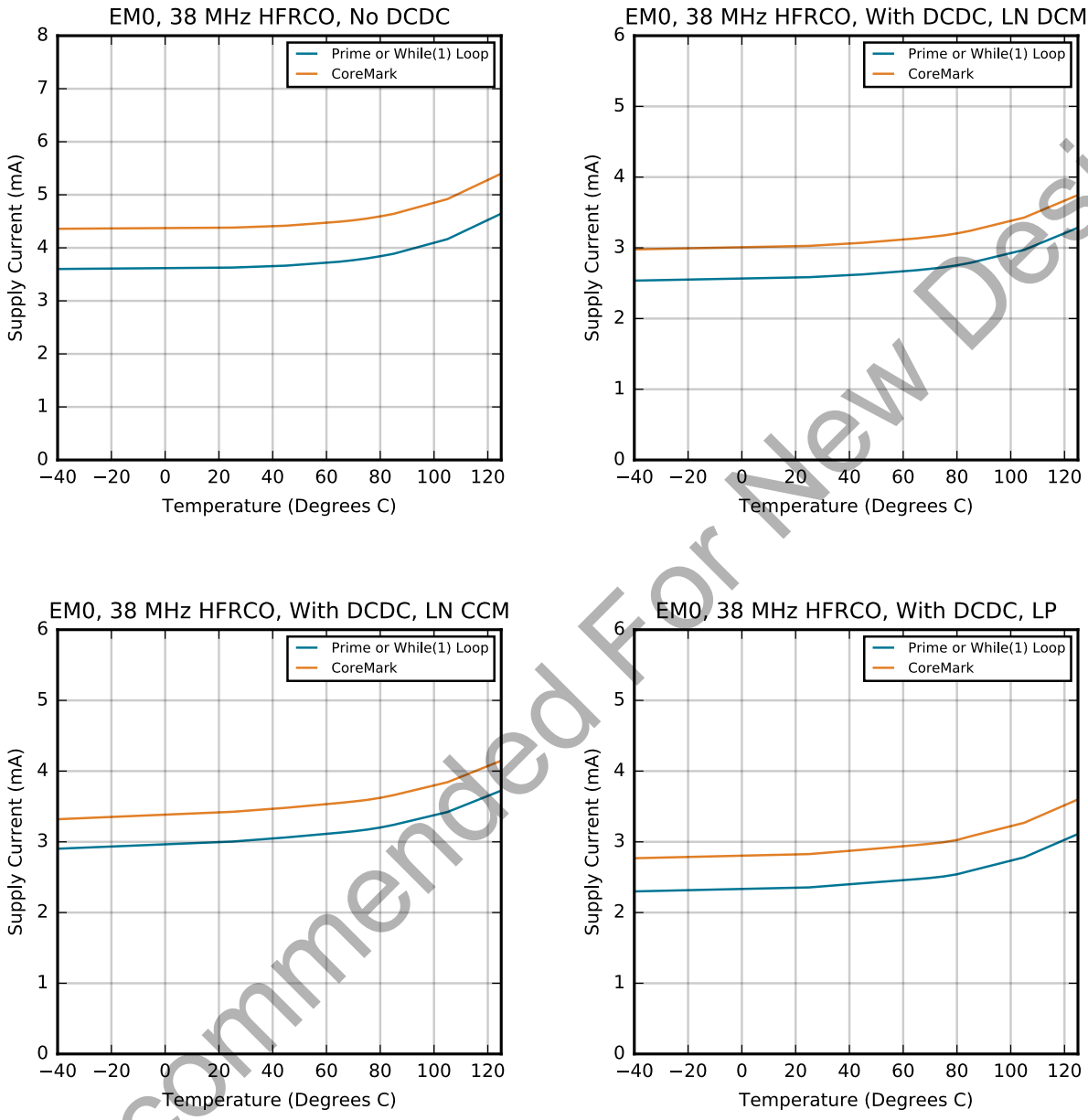


**Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature**

Not Recommended For New Designs

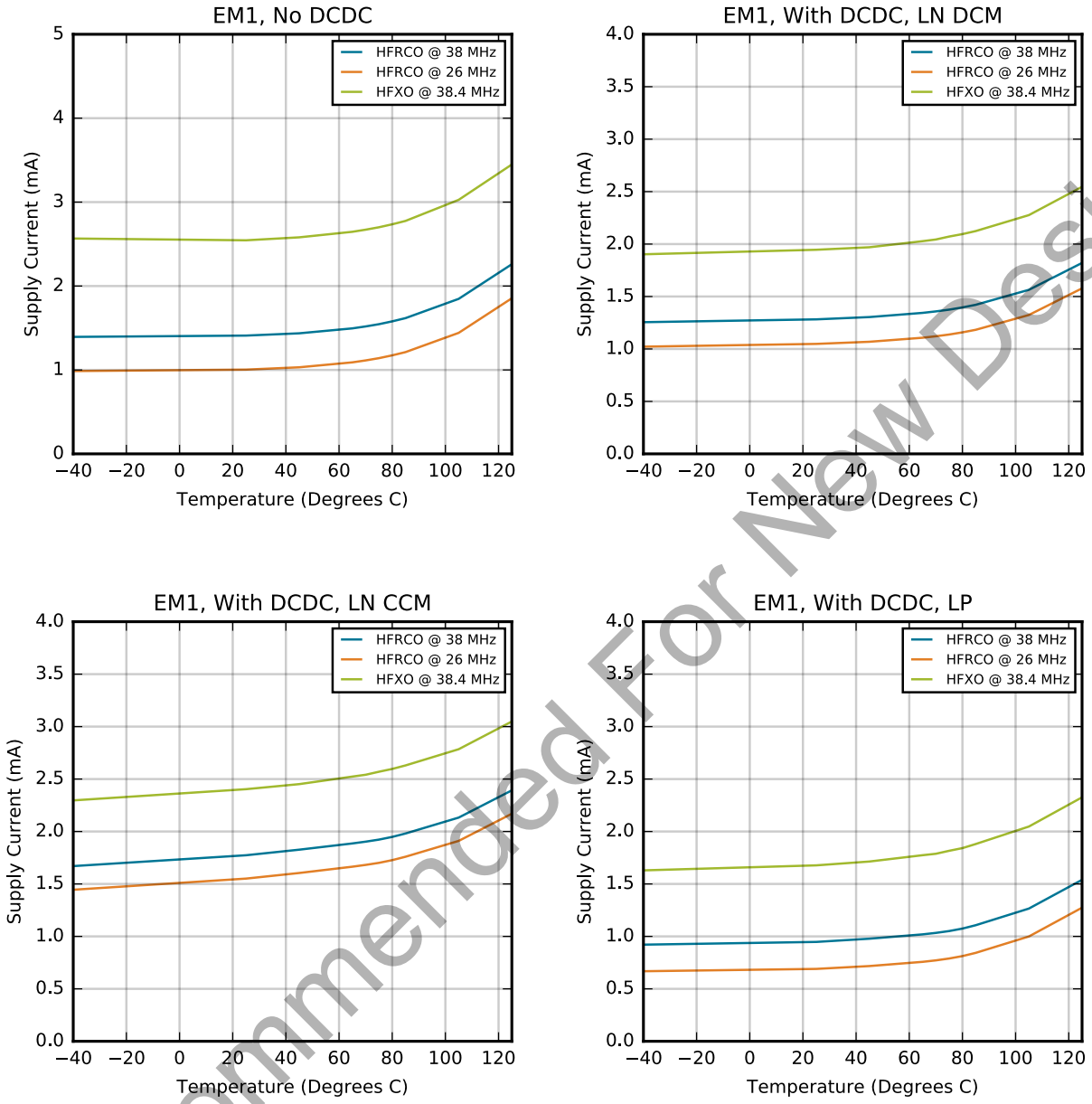


**Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature**

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Not Recommended For New Designs

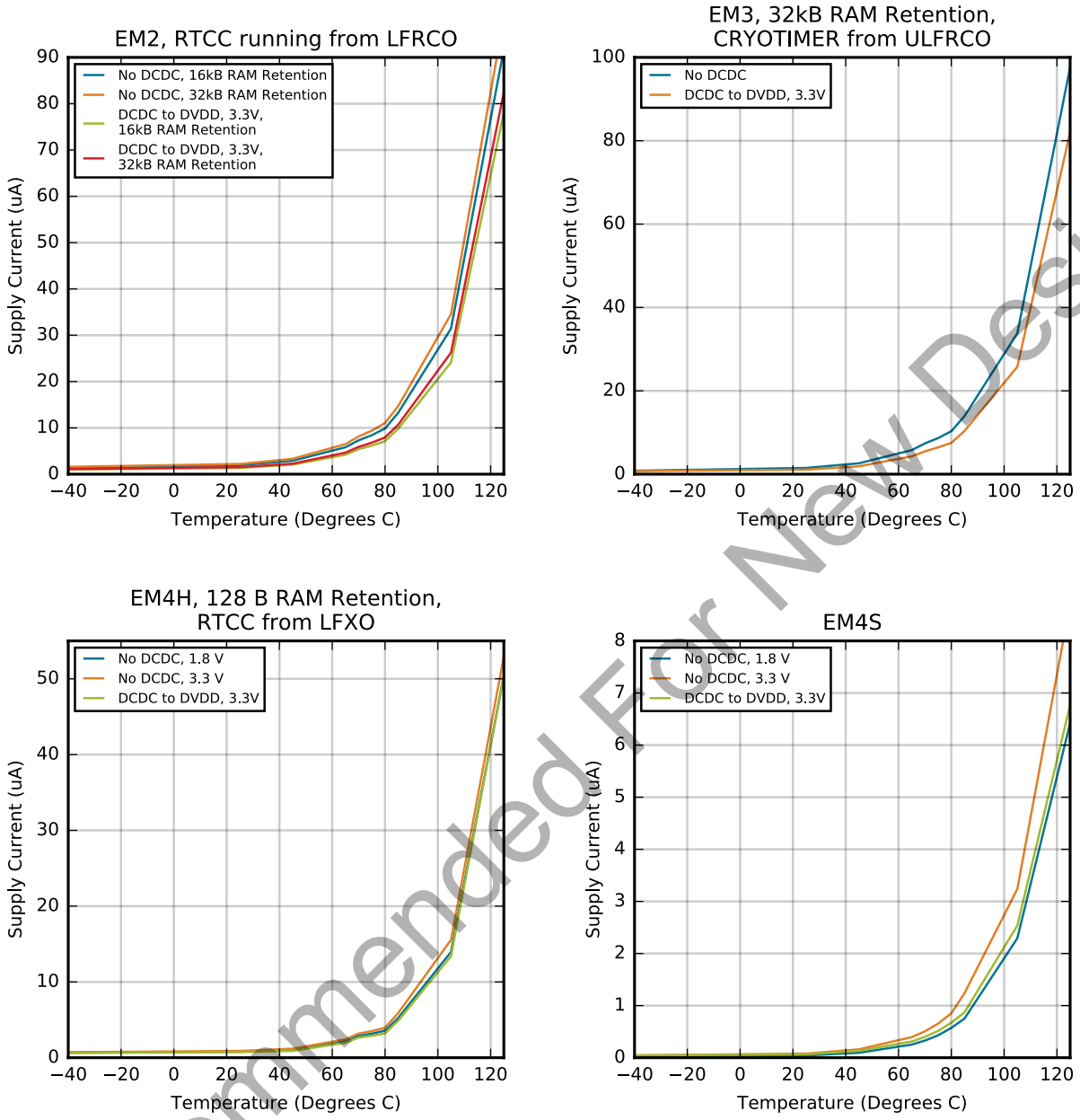


**Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature**

Not Recommended For New Designs

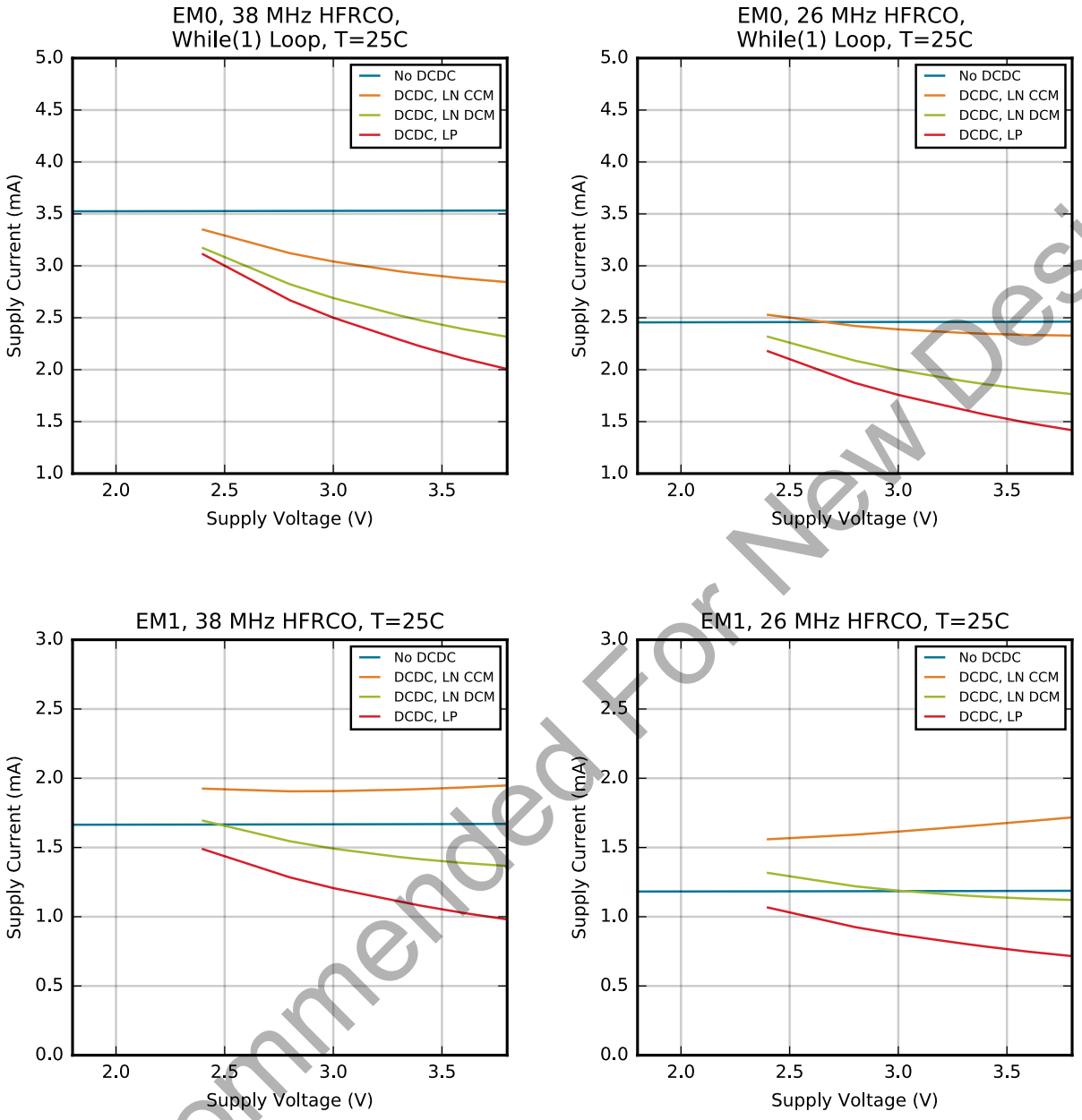


**Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply**

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Not Recommended For New Designs

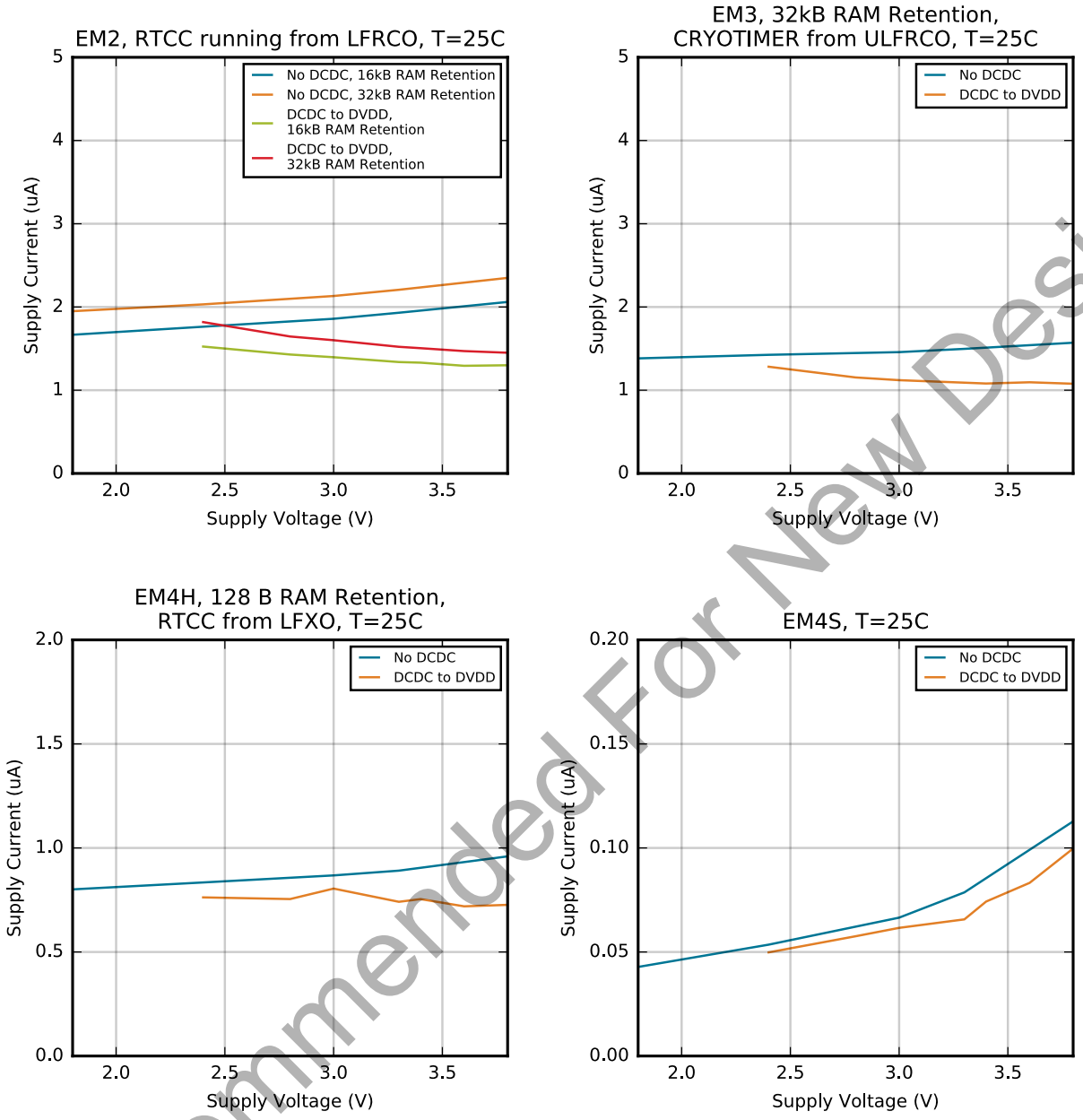


**Figure 4.7. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply**

Not Recommended For New Designs

### 4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

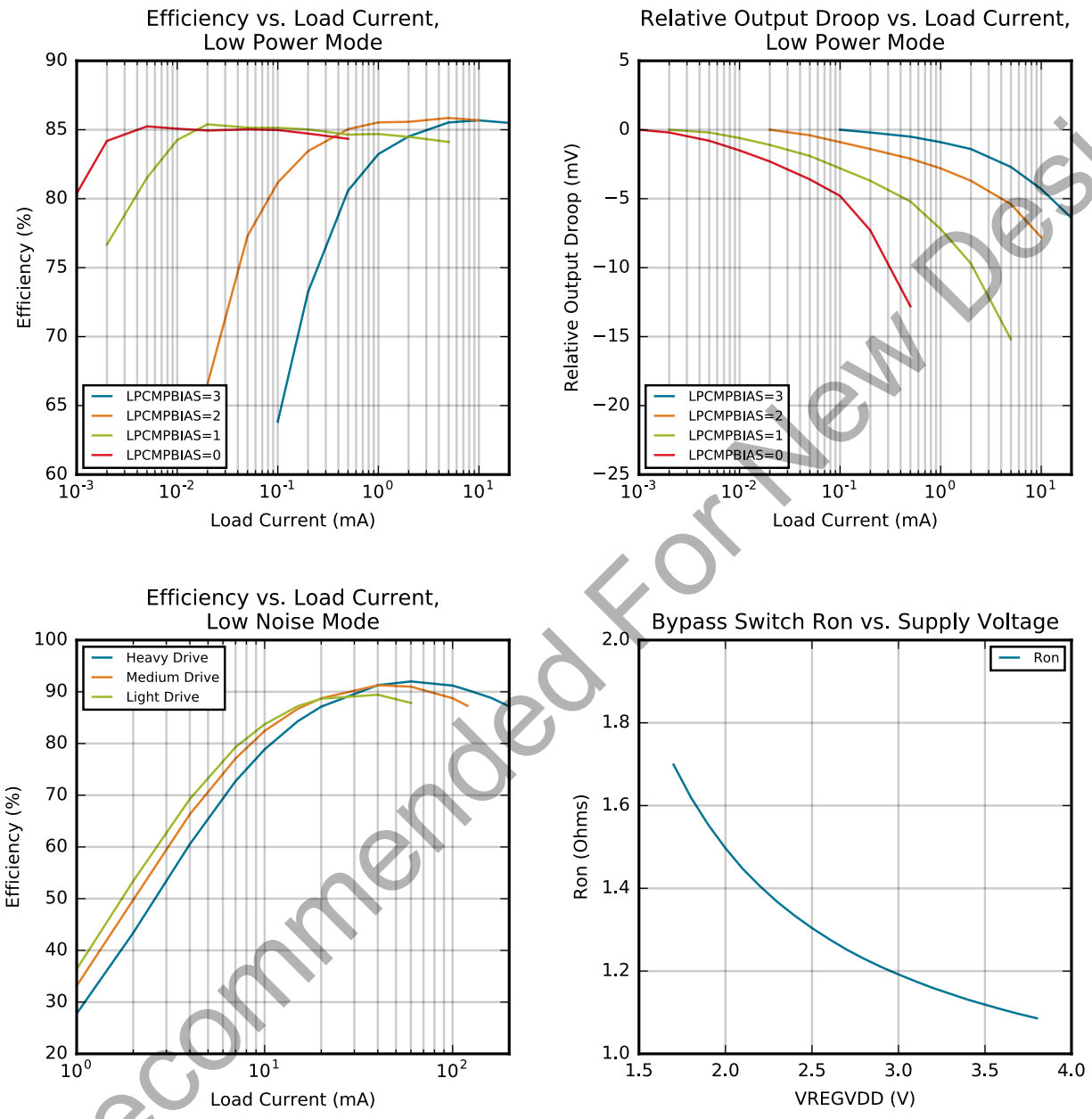


**Figure 4.8. DC-DC Converter Typical Performance Characteristics**

Not Recommended For New Designs

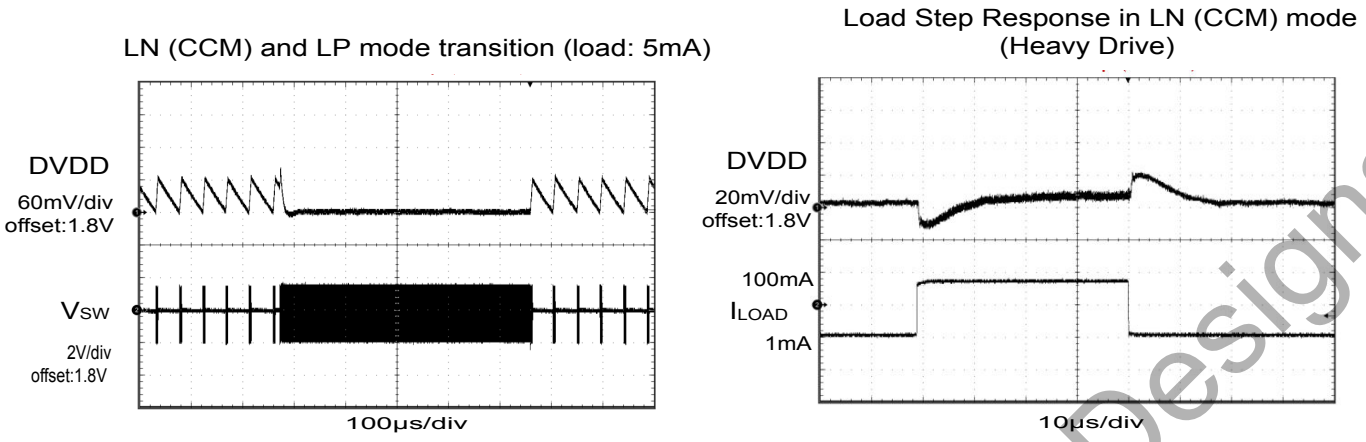


**Figure 4.9. DC-DC Converter Transition Waveforms**

Not Recommended For New Designs

### 4.2.3 2.4 GHz Radio

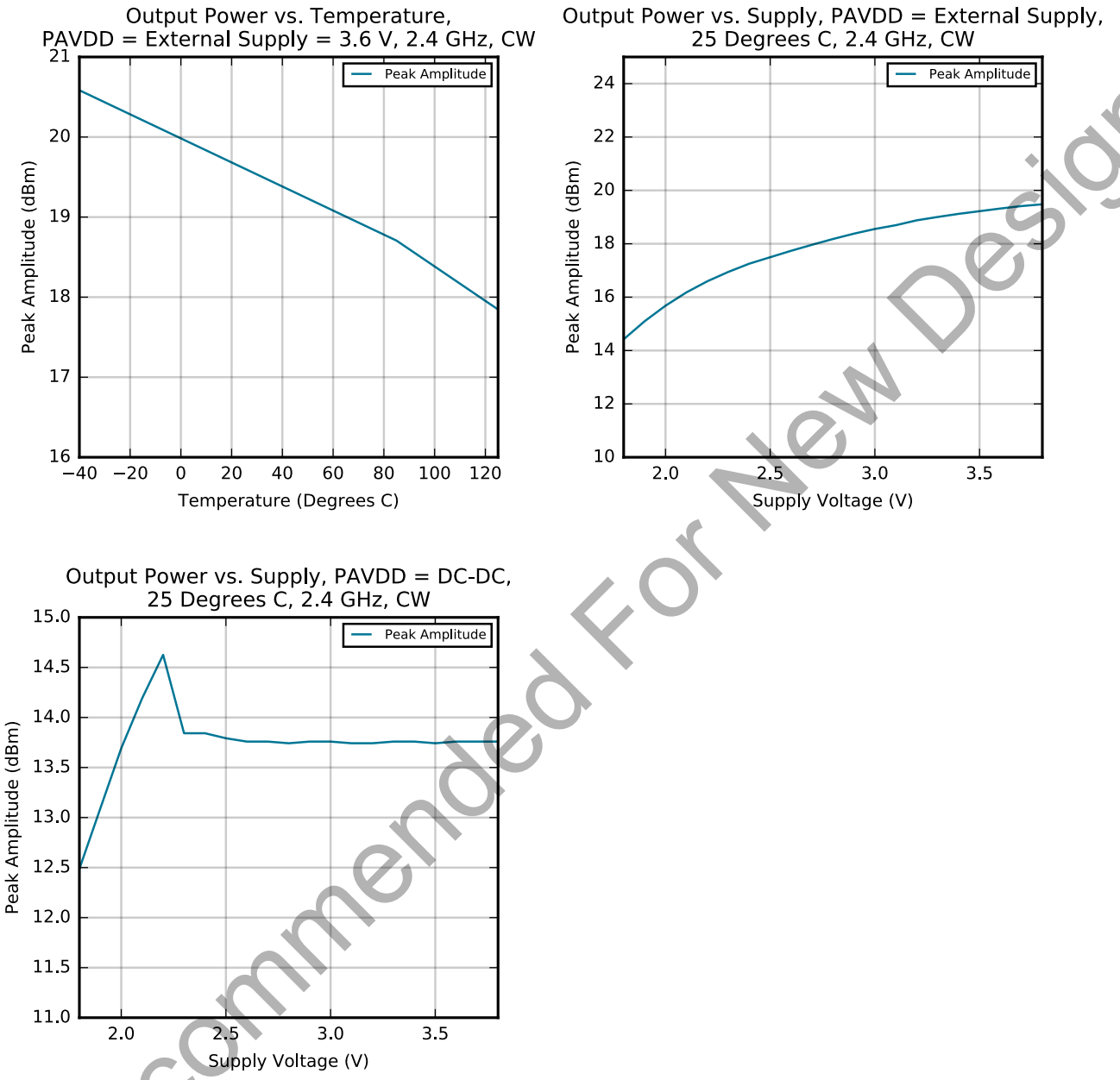


**Figure 4.10. 2.4 GHz RF Transmitter Output Power**

Not Recommended For New Designs

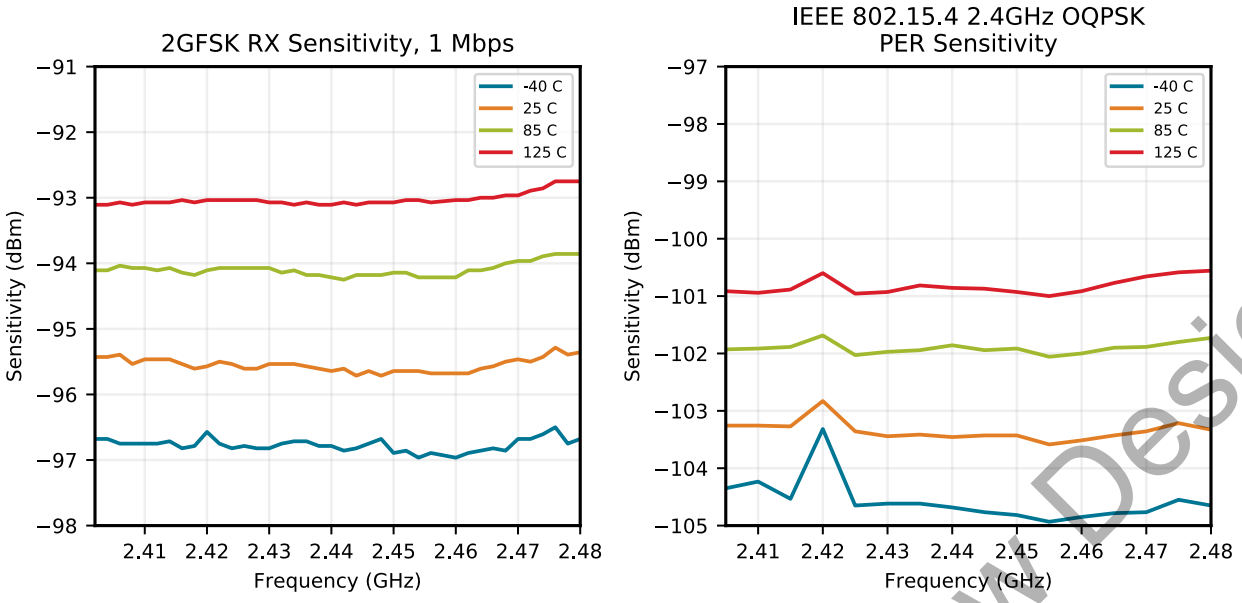


**Figure 4.11. 2.4 GHz RF Receiver Sensitivity**

Not Recommended For New Designs

# 5. Typical Connection Diagrams

## 5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

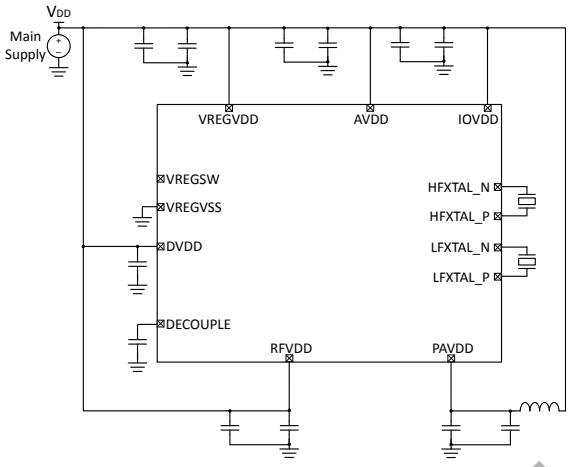


**Figure 5.1. EFR32MG14 Typical Application Circuit: Direct Supply Configuration without DC-DC converter**

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

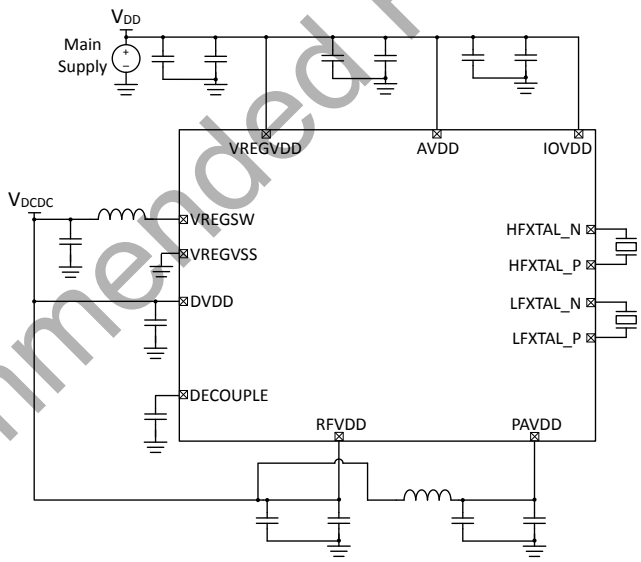


**Figure 5.2. EFR32MG14 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC)**

Not Recommended For New Designs

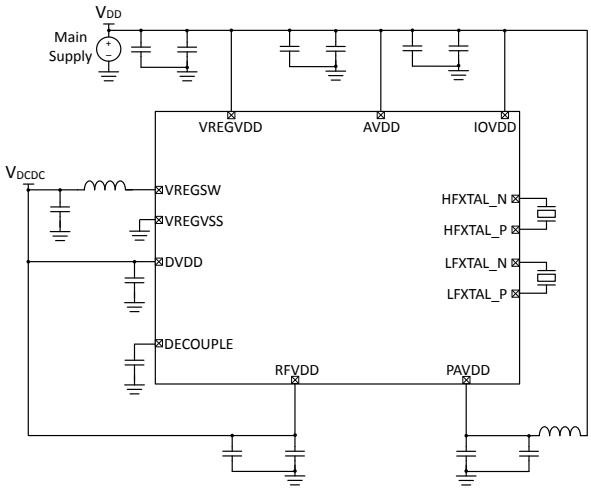


**Figure 5.3. EFR32MG14 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDD)**

Not Recommended For New Designs

### 5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 112 for applications in the 2.4 GHz band, and in Figure 5.5 Typical Sub-GHz RF impedance-matching network circuits on page 112 for applications in the sub-GHz band. Application-specific component values can be found in the EFR32xG13 Reference Manual. For low RF transmit power applications less than 13 dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13 dBm).

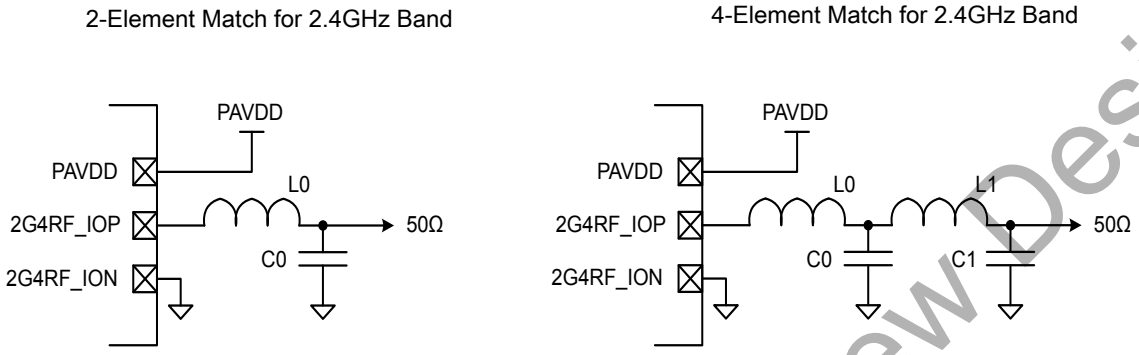


**Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits**

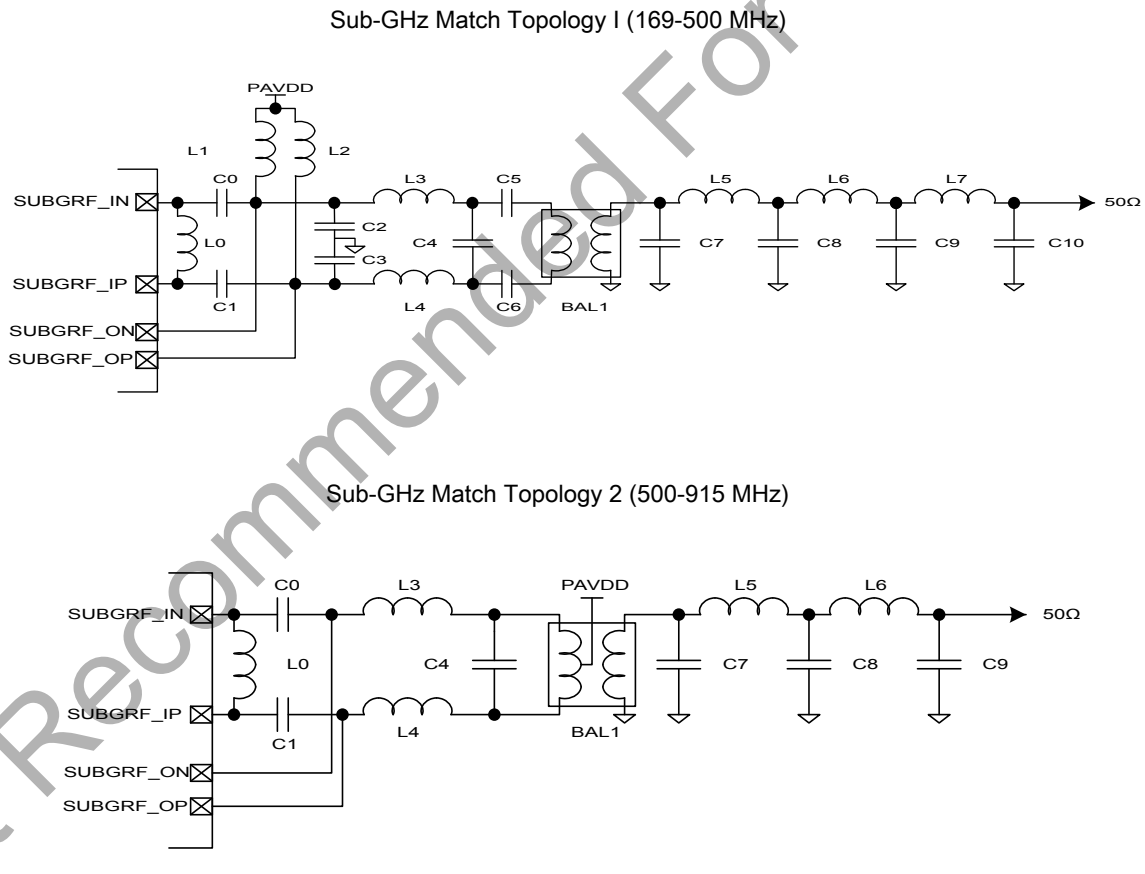


**Figure 5.5. Typical Sub-GHz RF impedance-matching network circuits**

Not Recommended For New Designs

### 5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

Not Recommended For New Designs

# 6. Pin Definitions

## 6.1 QFN48 2.4 GHz and Sub-GHz Device Pinout

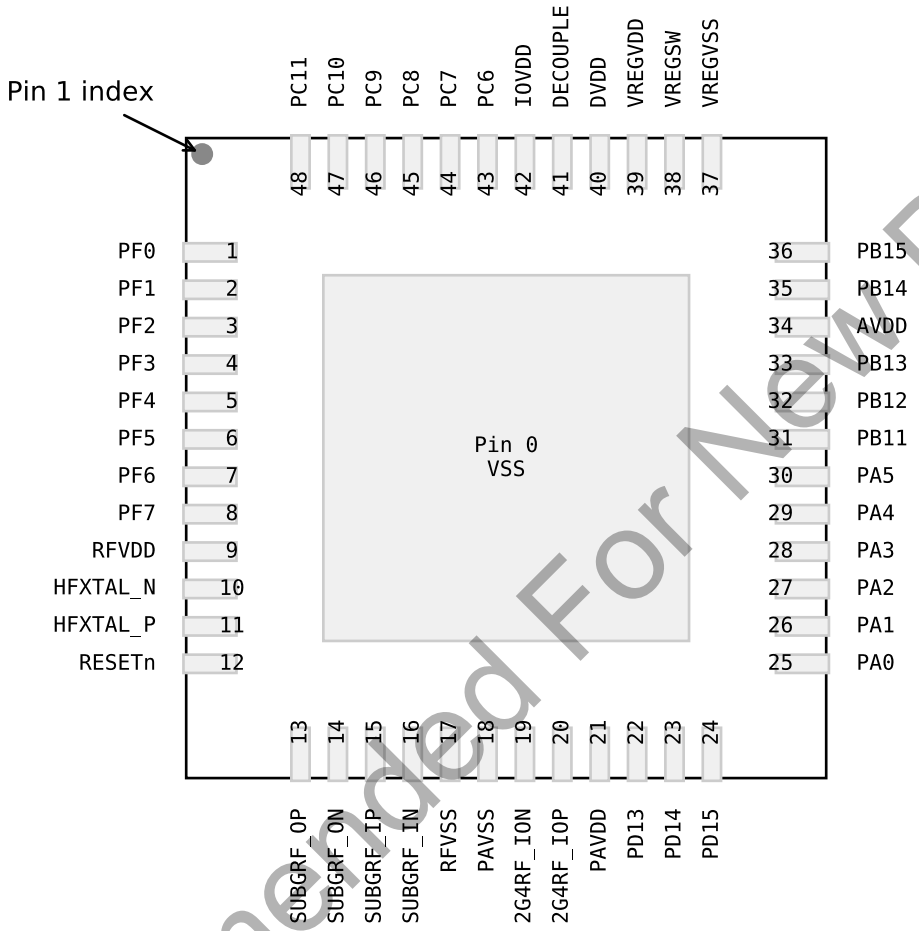


**Figure 6.1. QFN48 2.4 GHz and Sub-GHz Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 GPIO Functionality Table or 6.6 Alternate Functionality Overview.

**Table 6.1. QFN48 2.4 GHz and Sub-GHz Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PF0 | 1 | GPIO (5V) |
| PF1 | 2 | GPIO (5V) | PF2 | 3 | GPIO (5V) |
| PF3 | 4 | GPIO (5V) | PF4 | 5 | GPIO (5V) |
| PF5 | 6 | GPIO (5V) | PF6 | 7 | GPIO (5V) |
| PF7 | 8 | GPIO (5V) | RFVDD | 9 | Radio power supply |
| HFXTAL_N | 10 | High Frequency Crystal input pin. | HFXTAL_P | 11 | High Frequency Crystal output pin. |

Not Recommended For New Designs

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RESETn | 12 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | SUBGRF_OP | 13 | Sub GHz Differential RF output, positive path. |
| SUBGRF_ON | 14 | Sub GHz Differential RF output, negative path. | SUBGRF_IP | 15 | Sub GHz Differential RF input, positive path. |
| SUBGRF_IN | 16 | Sub GHz Differential RF input, negative path. | RFVSS | 17 | Radio Ground |
| PAVSS | 18 | Power Amplifier (PA) voltage regulator VSS | 2G4RF_ION | 19 | 2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded. |
| 2G4RF_IOP | 20 | 2.4 GHz Differential RF input/output, positive path. | PAVDD | 21 | Power Amplifier (PA) voltage regulator VDD input |
| PD13 | 22 | GPIO | PD14 | 23 | GPIO |
| PD15 | 24 | GPIO | PA0 | 25 | GPIO |
| PA1 | 26 | GPIO | PA2 | 27 | GPIO |
| PA3 | 28 | GPIO | PA4 | 29 | GPIO |
| PA5 | 30 | GPIO (5V) | PB11 | 31 | GPIO (5V) |
| PB12 | 32 | GPIO (5V) | PB13 | 33 | GPIO (5V) |
| AVDD | 34 | Analog power supply. | PB14 | 35 | GPIO |
| PB15 | 36 | GPIO | VREGVSS | 37 | Voltage regulator VSS |
| VREGSW | 38 | DCDC regulator switching node | VREGVDD | 39 | Voltage regulator VDD input |
| DVDD | 40 | Digital power supply. | DECOUPLE | 41 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| IOVDD | 42 | Digital IO power supply. | PC6 | 43 | GPIO (5V) |
| PC7 | 44 | GPIO (5V) | PC8 | 45 | GPIO (5V) |
| PC9 | 46 | GPIO (5V) | PC10 | 47 | GPIO (5V) |
| PC11 | 48 | GPIO (5V) | | | |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, and PB13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Not Recommended For New Designs

### 6.2 QFN48 2.4 GHz Device Pinout

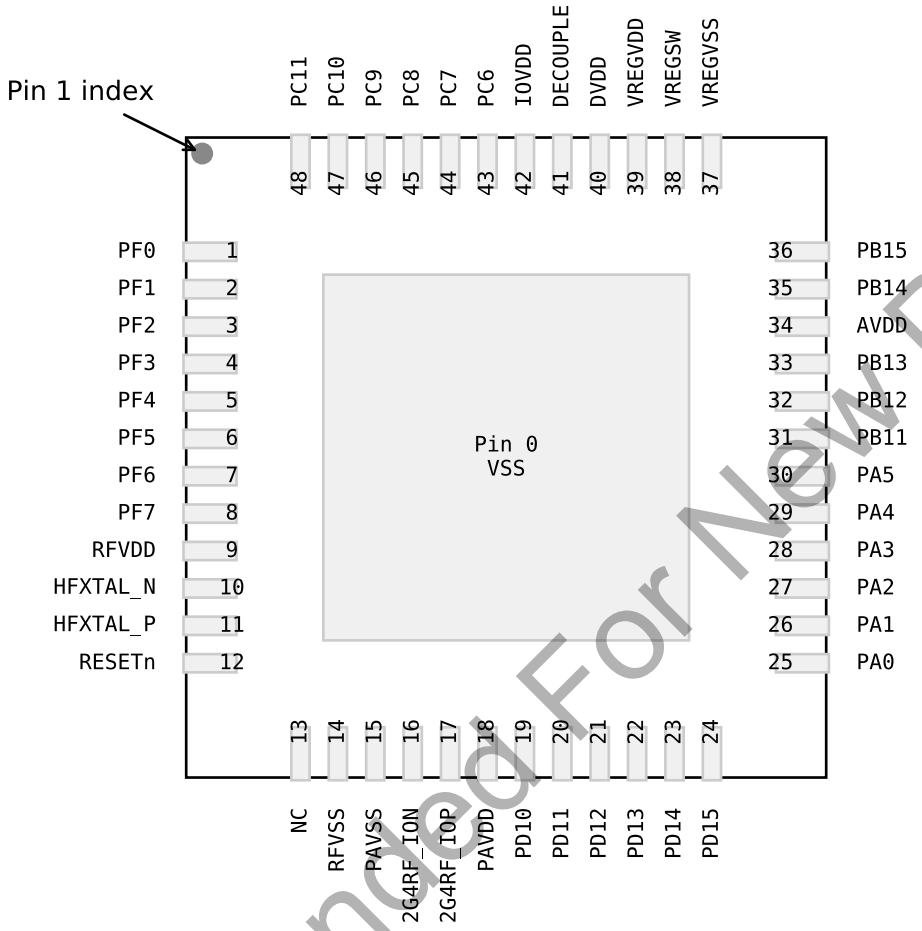


**Figure 6.2. QFN48 2.4 GHz Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 GPIO Functionality Table or 6.6 Alternate Functionality Overview.

**Table 6.2. QFN48 2.4 GHz Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PF0 | 1 | GPIO (5V) |
| PF1 | 2 | GPIO (5V) | PF2 | 3 | GPIO (5V) |
| PF3 | 4 | GPIO (5V) | PF4 | 5 | GPIO (5V) |
| PF5 | 6 | GPIO (5V) | PF6 | 7 | GPIO (5V) |
| PF7 | 8 | GPIO (5V) | RFVDD | 9 | Radio power supply |
| HFXTAL_N | 10 | High Frequency Crystal input pin. | HFXTAL_P | 11 | High Frequency Crystal output pin. |

Not Recommended For New Designs

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RESETn | 12 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | NC | 13 | No Connect. |
| RFVSS | 14 | Radio Ground | PAVSS | 15 | Power Amplifier (PA) voltage regulator VSS |
| 2G4RF_ION | 16 | 2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded. | 2G4RF_IOP | 17 | 2.4 GHz Differential RF input/output, positive path. |
| PAVDD | 18 | Power Amplifier (PA) voltage regulator VDD input | PD10 | 19 | GPIO (5V) |
| PD11 | 20 | GPIO (5V) | PD12 | 21 | GPIO (5V) |
| PD13 | 22 | GPIO | PD14 | 23 | GPIO |
| PD15 | 24 | GPIO | PA0 | 25 | GPIO |
| PA1 | 26 | GPIO | PA2 | 27 | GPIO |
| PA3 | 28 | GPIO | PA4 | 29 | GPIO |
| PA5 | 30 | GPIO (5V) | PB11 | 31 | GPIO (5V) |
| PB12 | 32 | GPIO (5V) | PB13 | 33 | GPIO (5V) |
| AVDD | 34 | Analog power supply. | PB14 | 35 | GPIO |
| PB15 | 36 | GPIO | VREGVSS | 37 | Voltage regulator VSS |
| VREGSW | 38 | DCDC regulator switching node | VREGVDD | 39 | Voltage regulator VDD input |
| DVDD | 40 | Digital power supply. | DECOUPLE | 41 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| IOVDD | 42 | Digital IO power supply. | PC6 | 43 | GPIO (5V) |
| PC7 | 44 | GPIO (5V) | PC8 | 45 | GPIO (5V) |
| PC9 | 46 | GPIO (5V) | PC10 | 47 | GPIO (5V) |
| PC11 | 48 | GPIO (5V) | | | |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, and PB13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Not Recommended For New Designs

### 6.3 QFN48 Sub-GHz Device Pinout

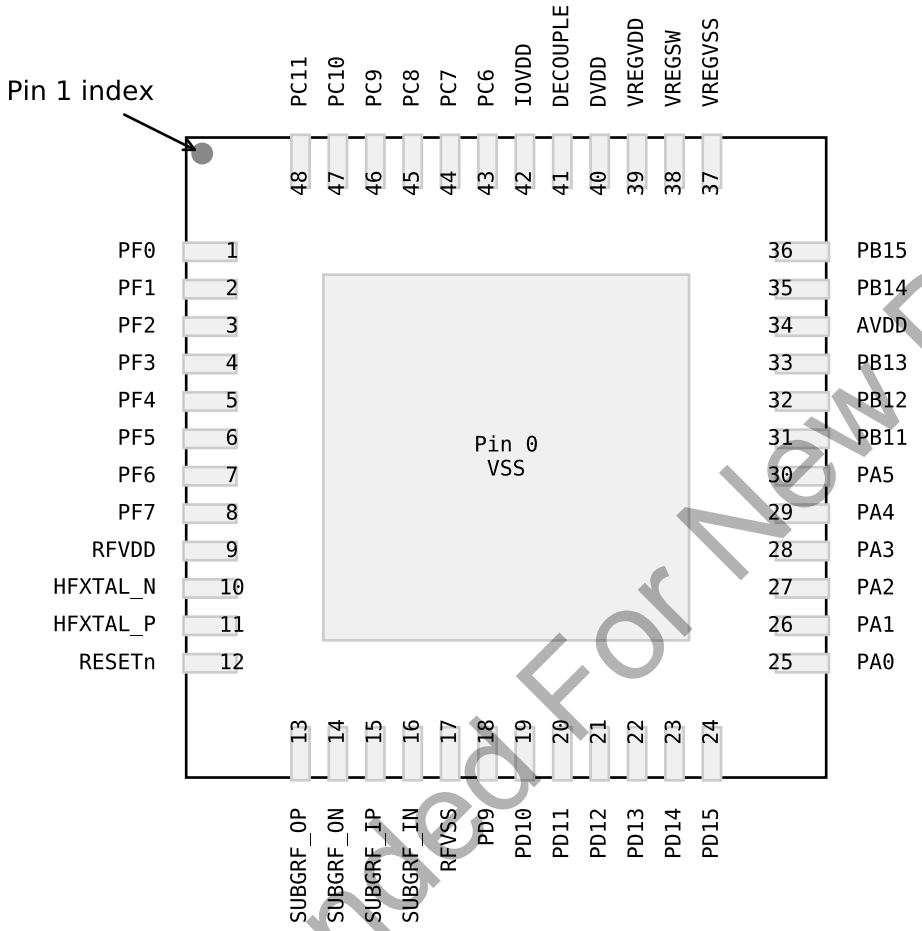


**Figure 6.3. QFN48 Sub-GHz Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 GPIO Functionality Table or 6.6 Alternate Functionality Overview.

**Table 6.3. QFN48 Sub-GHz Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PF0 | 1 | GPIO (5V) |
| PF1 | 2 | GPIO (5V) | PF2 | 3 | GPIO (5V) |
| PF3 | 4 | GPIO (5V) | PF4 | 5 | GPIO (5V) |
| PF5 | 6 | GPIO (5V) | PF6 | 7 | GPIO (5V) |
| PF7 | 8 | GPIO (5V) | RFVDD | 9 | Radio power supply |
| HFXTAL_N | 10 | High Frequency Crystal input pin. | HFXTAL_P | 11 | High Frequency Crystal output pin. |

Not Recommended For New Designs

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| RESETn | 12 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | SUBGRF_OP | 13 | Sub GHz Differential RF output, positive path. |
| SUBGRF_ON | 14 | Sub GHz Differential RF output, negative path. | SUBGRF_IP | 15 | Sub GHz Differential RF input, positive path. |
| SUBGRF_IN | 16 | Sub GHz Differential RF input, negative path. | RFVSS | 17 | Radio Ground |
| PD9 | 18 | GPIO (5V) | PD10 | 19 | GPIO (5V) |
| PD11 | 20 | GPIO (5V) | PD12 | 21 | GPIO (5V) |
| PD13 | 22 | GPIO | PD14 | 23 | GPIO |
| PD15 | 24 | GPIO | PA0 | 25 | GPIO |
| PA1 | 26 | GPIO | PA2 | 27 | GPIO |
| PA3 | 28 | GPIO | PA4 | 29 | GPIO |
| PA5 | 30 | GPIO (5V) | PB11 | 31 | GPIO (5V) |
| PB12 | 32 | GPIO (5V) | PB13 | 33 | GPIO (5V) |
| AVDD | 34 | Analog power supply. | PB14 | 35 | GPIO |
| PB15 | 36 | GPIO | VREGVSS | 37 | Voltage regulator VSS |
| VREGSW | 38 | DCDC regulator switching node | VREGVDD | 39 | Voltage regulator VDD input |
| DVDD | 40 | Digital power supply. | DECOUPLE | 41 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| IOVDD | 42 | Digital IO power supply. | PC6 | 43 | GPIO (5V) |
| PC7 | 44 | GPIO (5V) | PC8 | 45 | GPIO (5V) |
| PC9 | 46 | GPIO (5V) | PC10 | 47 | GPIO (5V) |
| PC11 | 48 | GPIO (5V) | | | |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, and PB13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Not Recommended For New Designs

### 6.4 QFN32 2.4 GHz Device Pinout

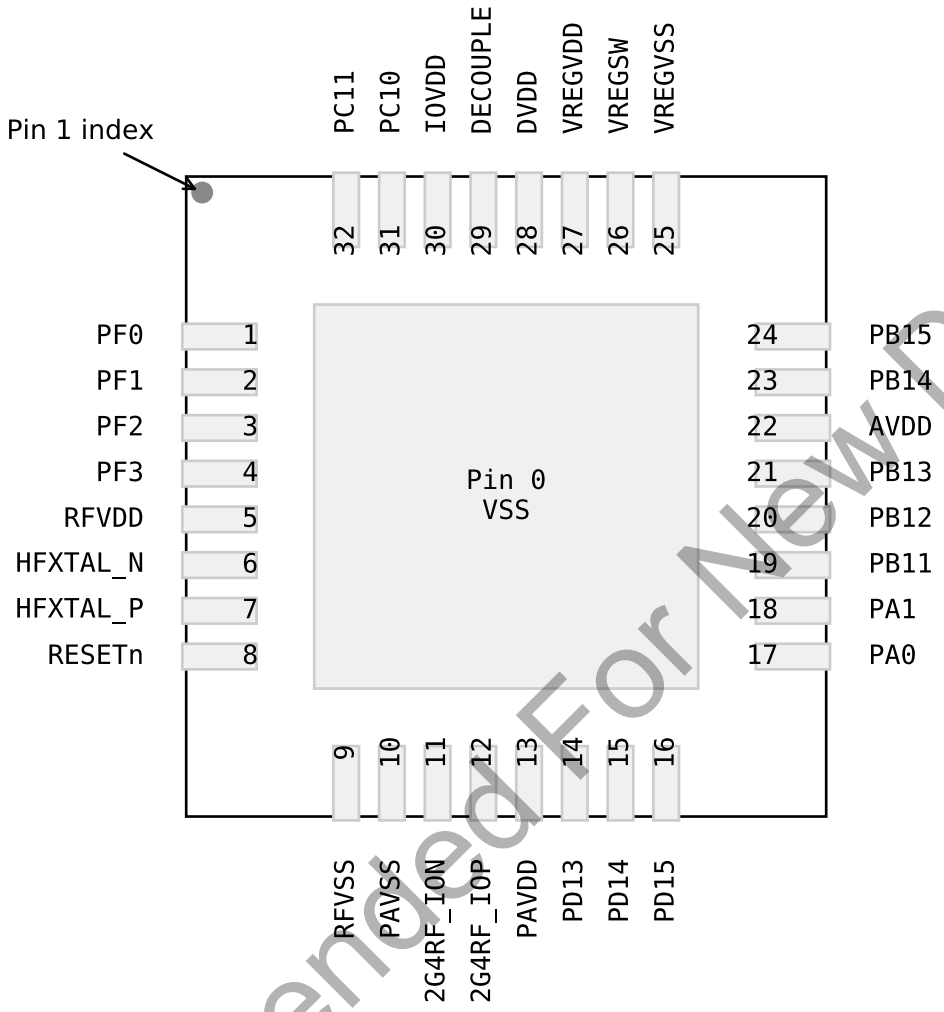


**Figure 6.4. QFN32 2.4 GHz Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 GPIO Functionality Table or 6.6 Alternate Functionality Overview.

**Table 6.4. QFN32 2.4 GHz Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PF0 | 1 | GPIO (5V) |
| PF1 | 2 | GPIO (5V) | PF2 | 3 | GPIO (5V) |
| PF3 | 4 | GPIO (5V) | RFVDD | 5 | Radio power supply |
| HFXTAL_N | 6 | High Frequency Crystal input pin. | HFXTAL_P | 7 | High Frequency Crystal output pin. |
| RESETn | 8 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | RFVSS | 9 | Radio Ground |

Not Recommended For New Designs

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PAVSS | 10 | Power Amplifier (PA) voltage regulator VSS | 2G4RF_ION | 11 | 2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded. |
| 2G4RF_IOP | 12 | 2.4 GHz Differential RF input/output, positive path. | PAVDD | 13 | Power Amplifier (PA) voltage regulator VDD input |
| PD13 | 14 | GPIO | PD14 | 15 | GPIO |
| PD15 | 16 | GPIO | PA0 | 17 | GPIO |
| PA1 | 18 | GPIO | PB11 | 19 | GPIO (5V) |
| PB12 | 20 | GPIO (5V) | PB13 | 21 | GPIO (5V) |
| AVDD | 22 | Analog power supply. | PB14 | 23 | GPIO |
| PB15 | 24 | GPIO | VREGVSS | 25 | Voltage regulator VSS |
| VREGSW | 26 | DCDC regulator switching node | VREGVDD | 27 | Voltage regulator VDD input |
| DVDD | 28 | Digital power supply. | DECOUPLE | 29 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| IOVDD | 30 | Digital IO power supply. | PC10 | 31 | GPIO (5V) |
| PC11 | 32 | GPIO (5V) | | | |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, and PB13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Not Recommended For New Designs

### 6.5 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 6.6 Alternate Functionality Overview for a list of GPIO locations available for each function.

**Table 6.5. GPIO Functionality Table**

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PA0 | BUSDY BUSCX ADC0_EXTN | TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31 | US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31 | FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28 | CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8 |
| PA1 | BUSCY BUSDX ADC0_EXTP VDAC0_EXT | TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0 | US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0 | FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29 | CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9 |
| PA2 | VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P | TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1 | US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1 | FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MODEM_ANT1 #30 | PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PA3 | BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT | TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE-TIM0_OUT0 #3 LE-TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2 | US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2 | FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31 | PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8 |
| PA4 | VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N | TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3 | US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3 | FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0 | PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12 |
| PA5 | VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX | TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC1 #3 WTIM0_CC2 #1 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4 | US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4 | FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1 | CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PB11 | BUSCY BUSDX | TIM0_CC0 #6<br>TIM0_CC1 #5<br>TIM0_CC2 #4<br>TIM0_CDTI0 #3<br>TIM0_CDTI1 #2<br>TIM0_CDTI2 #1<br>TIM1_CC0 #6<br>TIM1_CC1 #5<br>TIM1_CC2 #4<br>TIM1_CC3 #3<br>WTIM0_CC0 #15<br>WTIM0_CC1 #13<br>WTIM0_CC2 #11<br>WTIM0_CDTI0 #7<br>WTIM0_CDTI1 #5<br>WTIM0_CDTI2 #3<br>LETIM0_OUT0 #6<br>LETIM0_OUT1 #5<br>PCNT0_S0IN #6<br>PCNT0_S1IN #5 | US0_TX #6 US0_RX #5 US0_CLK #4<br>US0_CS #3<br>US0_CTS #2<br>US0_RTS #1<br>US1_TX #6 US1_RX #5 US1_CLK #4<br>US1_CS #3<br>US1_CTS #2<br>US1_RTS #1<br>LEU0_TX #6<br>LEU0_RX #5<br>I2C0_SDA #6<br>I2C0_SCL #5 | FRC_DCLK #6<br>FRC_DOUT #5<br>FRC_DFRAME #4<br>MODEM_DCLK #6<br>MODEM_DIN #5<br>MODEM_DOUT #4<br>MODEM_ANT0 #3<br>MODEM_ANT1 #2 | PRS_CH6 #6<br>PRS_CH7 #5<br>PRS_CH8 #4<br>PRS_CH9 #3<br>ACMP0_O #6<br>ACMP1_O #6 |
| PB12 | BUSDY BUSCX | TIM0_CC0 #7<br>TIM0_CC1 #6<br>TIM0_CC2 #5<br>TIM0_CDTI0 #4<br>TIM0_CDTI1 #3<br>TIM0_CDTI2 #2<br>TIM1_CC0 #7<br>TIM1_CC1 #6<br>TIM1_CC2 #5<br>TIM1_CC3 #4<br>WTIM0_CC0 #16<br>WTIM0_CC1 #14<br>WTIM0_CC2 #12<br>WTIM0_CDTI0 #8<br>WTIM0_CDTI1 #6<br>WTIM0_CDTI2 #4<br>LETIM0_OUT0 #7<br>LETIM0_OUT1 #6<br>PCNT0_S0IN #7<br>PCNT0_S1IN #6 | US0_TX #7 US0_RX #6 US0_CLK #5<br>US0_CS #4<br>US0_CTS #3<br>US0_RTS #2<br>US1_TX #7 US1_RX #6 US1_CLK #5<br>US1_CS #4<br>US1_CTS #3<br>US1_RTS #2<br>LEU0_TX #7<br>LEU0_RX #6<br>I2C0_SDA #7<br>I2C0_SCL #6 | FRC_DCLK #7<br>FRC_DOUT #6<br>FRC_DFRAME #5<br>MODEM_DCLK #7<br>MODEM_DIN #6<br>MODEM_DOUT #5<br>MODEM_ANT0 #4<br>MODEM_ANT1 #3 | PRS_CH6 #7<br>PRS_CH7 #6<br>PRS_CH8 #5<br>PRS_CH9 #4<br>ACMP0_O #7<br>ACMP1_O #7 |
| PB13 | BUSCY BUSDX | TIM0_CC0 #8<br>TIM0_CC1 #7<br>TIM0_CC2 #6<br>TIM0_CDTI0 #5<br>TIM0_CDTI1 #4<br>TIM0_CDTI2 #3<br>TIM1_CC0 #8<br>TIM1_CC1 #7<br>TIM1_CC2 #6<br>TIM1_CC3 #5<br>WTIM0_CC0 #17<br>WTIM0_CC1 #15<br>WTIM0_CC2 #13<br>WTIM0_CDTI0 #9<br>WTIM0_CDTI1 #7<br>WTIM0_CDTI2 #5<br>LETIM0_OUT0 #8<br>LETIM0_OUT1 #7<br>PCNT0_S0IN #8<br>PCNT0_S1IN #7 | US0_TX #8 US0_RX #7 US0_CLK #6<br>US0_CS #5<br>US0_CTS #4<br>US0_RTS #3<br>US1_TX #8 US1_RX #7 US1_CLK #6<br>US1_CS #5<br>US1_CTS #4<br>US1_RTS #3<br>LEU0_TX #8<br>LEU0_RX #7<br>I2C0_SDA #8<br>I2C0_SCL #7 | FRC_DCLK #8<br>FRC_DOUT #7<br>FRC_DFRAME #6<br>MODEM_DCLK #8<br>MODEM_DIN #7<br>MODEM_DOUT #6<br>MODEM_ANT0 #5<br>MODEM_ANT1 #4 | CMU_CLKI0 #0<br>PRS_CH6 #8<br>PRS_CH7 #7<br>PRS_CH8 #6<br>PRS_CH9 #5<br>ACMP0_O #8<br>ACMP1_O #8<br>DBG_SWO #1<br>GPIO_EM4WU9 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PB14 | BUSDY BUSCX LFXTAL_N | TIM0_CC0 #9<br>TIM0_CC1 #8<br>TIM0_CC2 #7<br>TIM0_CDTI0 #6<br>TIM0_CDTI1 #5<br>TIM0_CDTI2 #4<br>TIM1_CC0 #9<br>TIM1_CC1 #8<br>TIM1_CC2 #7<br>TIM1_CC3 #6<br>WTIM0_CC0 #18<br>WTIM0_CC1 #16<br>WTIM0_CC2 #14<br>WTIM0_CDTI0 #10<br>WTIM0_CDTI1 #8<br>WTIM0_CDTI2 #6<br>LETIM0_OUT0 #9<br>LETIM0_OUT1 #8<br>PCNT0_S0IN #9<br>PCNT0_S1IN #8 | US0_TX #9 US0_RX #8 US0_CLK #7<br>US0_CS #6<br>US0_CTS #5<br>US0_RTS #4<br>US1_TX #9 US1_RX #8 US1_CLK #7<br>US1_CS #6<br>US1_CTS #5<br>US1_RTS #4<br>LEU0_TX #9<br>LEU0_RX #8<br>I2C0_SDA #9<br>I2C0_SCL #8 | FRC_DCLK #9<br>FRC_DOUT #8<br>FRC_DFRAME #7<br>MODEM_DCLK #9<br>MODEM_DIN #8<br>MODEM_DOUT #7<br>MODEM_ANT0 #6<br>MODEM_ANT1 #5 | CMU_CLK1 #1<br>PRS_CH6 #9<br>PRS_CH7 #8<br>PRS_CH8 #7<br>PRS_CH9 #6<br>ACMP0_O #9<br>ACMP1_O #9 |
| PB15 | BUSCY BUSDX LFXTAL_P | TIM0_CC0 #10<br>TIM0_CC1 #9<br>TIM0_CC2 #8<br>TIM0_CDTI0 #7<br>TIM0_CDTI1 #6<br>TIM0_CDTI2 #5<br>TIM1_CC0 #10<br>TIM1_CC1 #9<br>TIM1_CC2 #8<br>TIM1_CC3 #7<br>WTIM0_CC0 #19<br>WTIM0_CC1 #17<br>WTIM0_CC2 #15<br>WTIM0_CDTI0 #11<br>WTIM0_CDTI1 #9<br>WTIM0_CDTI2 #7<br>LETIM0_OUT0 #10<br>LETIM0_OUT1 #9<br>PCNT0_S0IN #10<br>PCNT0_S1IN #9 | US0_TX #10<br>US0_RX #9<br>US0_CLK #8<br>US0_CS #7<br>US0_CTS #6<br>US0_RTS #5<br>US1_TX #10<br>US1_RX #9<br>US1_CLK #8<br>US1_CS #7<br>US1_CTS #6<br>US1_RTS #5<br>LEU0_TX #10<br>LEU0_RX #9<br>I2C0_SDA #10<br>I2C0_SCL #9 | FRC_DCLK #10<br>FRC_DOUT #9<br>FRC_DFRAME #8<br>MODEM_DCLK #10<br>MODEM_DIN #9<br>MODEM_DOUT #8<br>MODEM_ANT0 #7<br>MODEM_ANT1 #6 | CMU_CLK0 #1<br>PRS_CH6 #10<br>PRS_CH7 #9<br>PRS_CH8 #8<br>PRS_CH9 #7<br>ACMP0_O #10<br>ACMP1_O #10 |
| PC6 | BUSBY BUSAX | TIM0_CC0 #11<br>TIM0_CC1 #10<br>TIM0_CC2 #9<br>TIM0_CDTI0 #8<br>TIM0_CDTI1 #7<br>TIM0_CDTI2 #6<br>TIM1_CC0 #11<br>TIM1_CC1 #10<br>TIM1_CC2 #9<br>TIM1_CC3 #8<br>WTIM0_CC0 #26<br>WTIM0_CC1 #24<br>WTIM0_CC2 #22<br>WTIM0_CDTI0 #18<br>WTIM0_CDTI1 #16<br>WTIM0_CDTI2 #14<br>LETIM0_OUT0 #11<br>LETIM0_OUT1 #10<br>PCNT0_S0IN #11<br>PCNT0_S1IN #10 | US0_TX #11<br>US0_RX #10<br>US0_CLK #9<br>US0_CS #8<br>US0_CTS #7<br>US0_RTS #6<br>US1_TX #11<br>US1_RX #10<br>US1_CLK #9<br>US1_CS #8<br>US1_CTS #7<br>US1_RTS #6<br>LEU0_TX #11<br>LEU0_RX #10<br>I2C0_SDA #11<br>I2C0_SCL #10 | FRC_DCLK #11<br>FRC_DOUT #10<br>FRC_DFRAME #9<br>MODEM_DCLK #11<br>MODEM_DIN #10<br>MODEM_DOUT #9<br>MODEM_ANT0 #8<br>MODEM_ANT1 #7 | CMU_CLK0 #2<br>CMU_CLKI0 #2<br>PRS_CH0 #8<br>PRS_CH9 #11<br>PRS_CH10 #0<br>PRS_CH11 #5<br>ACMP0_O #11<br>ACMP1_O #11 |

Not Recommended For New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PC7 | BUSAY BUSBX | TIM0_CC0 #12<br>TIM0_CC1 #11<br>TIM0_CC2 #10<br>TIM0_CDTI0 #9<br>TIM0_CDTI1 #8<br>TIM0_CDTI2 #7<br>TIM1_CC0 #12<br>TIM1_CC1 #11<br>TIM1_CC2 #10<br>TIM1_CC3 #9<br>WTIM0_CC0 #27<br>WTIM0_CC1 #25<br>WTIM0_CC2 #23<br>WTIM0_CDTI0 #19<br>WTIM0_CDTI1 #17<br>WTIM0_CDTI2 #15<br>LETIM0_OUT0 #12<br>LETIM0_OUT1 #11<br>PCNT0_S0IN #12<br>PCNT0_S1IN #11 | US0_TX #12<br>US0_RX #11<br>US0_CLK #10<br>US0_CS #9<br>US0_CTS #8<br>US0_RTS #7<br>US1_TX #12<br>US1_RX #11<br>US1_CLK #10<br>US1_CS #9<br>US1_CTS #8<br>US1_RTS #7<br>LEU0_TX #12<br>LEU0_RX #11<br>I2C0_SDA #12<br>I2C0_SCL #11 | FRC_DCLK #12<br>FRC_DOUT #11<br>FRC_DFRAME #10<br>MODEM_DCLK #12<br>MODEM_DIN #11<br>MODEM_DOUT #10<br>MODEM_ANT0 #9<br>MODEM_ANT1 #8 | CMU_CLK1 #2<br>PRS_CH0 #9<br>PRS_CH9 #12<br>PRS_CH10 #1<br>PRS_CH11 #0<br>ACMP0_O #12<br>ACMP1_O #12 |
| PC8 | BUSBY BUSAX | TIM0_CC0 #13<br>TIM0_CC1 #12<br>TIM0_CC2 #11<br>TIM0_CDTI0 #10<br>TIM0_CDTI1 #9<br>TIM0_CDTI2 #8<br>TIM1_CC0 #13<br>TIM1_CC1 #12<br>TIM1_CC2 #11<br>TIM1_CC3 #10<br>WTIM0_CC0 #28<br>WTIM0_CC1 #26<br>WTIM0_CC2 #24<br>WTIM0_CDTI0 #20<br>WTIM0_CDTI1 #18<br>WTIM0_CDTI2 #16<br>LETIM0_OUT0 #13<br>LETIM0_OUT1 #12<br>PCNT0_S0IN #13<br>PCNT0_S1IN #12 | US0_TX #13<br>US0_RX #12<br>US0_CLK #11<br>US0_CS #10<br>US0_CTS #9<br>US0_RTS #8<br>US1_TX #13<br>US1_RX #12<br>US1_CLK #11<br>US1_CS #10<br>US1_CTS #9<br>US1_RTS #8<br>LEU0_TX #13<br>LEU0_RX #12<br>I2C0_SDA #13<br>I2C0_SCL #12 | FRC_DCLK #13<br>FRC_DOUT #12<br>FRC_DFRAME #11<br>MODEM_DCLK #13<br>MODEM_DIN #12<br>MODEM_DOUT #11<br>MODEM_ANT0 #10<br>MODEM_ANT1 #9 | PRS_CH0 #10<br>PRS_CH9 #13<br>PRS_CH10 #2<br>PRS_CH11 #1<br>ACMP0_O #13<br>ACMP1_O #13 |
| PC9 | BUSAY BUSBX | TIM0_CC0 #14<br>TIM0_CC1 #13<br>TIM0_CC2 #12<br>TIM0_CDTI0 #11<br>TIM0_CDTI1 #10<br>TIM0_CDTI2 #9<br>TIM1_CC0 #14<br>TIM1_CC1 #13<br>TIM1_CC2 #12<br>TIM1_CC3 #11<br>WTIM0_CC0 #29<br>WTIM0_CC1 #27<br>WTIM0_CC2 #25<br>WTIM0_CDTI0 #21<br>WTIM0_CDTI1 #19<br>WTIM0_CDTI2 #17<br>LETIM0_OUT0 #14<br>LETIM0_OUT1 #13<br>PCNT0_S0IN #14<br>PCNT0_S1IN #13 | US0_TX #14<br>US0_RX #13<br>US0_CLK #12<br>US0_CS #11<br>US0_CTS #10<br>US0_RTS #9<br>US1_TX #14<br>US1_RX #13<br>US1_CLK #12<br>US1_CS #11<br>US1_CTS #10<br>US1_RTS #9<br>LEU0_TX #14<br>LEU0_RX #13<br>I2C0_SDA #14<br>I2C0_SCL #13 | FRC_DCLK #14<br>FRC_DOUT #13<br>FRC_DFRAME #12<br>MODEM_DCLK #14<br>MODEM_DIN #13<br>MODEM_DOUT #12<br>MODEM_ANT0 #11<br>MODEM_ANT1 #10 | PRS_CH0 #11<br>PRS_CH9 #14<br>PRS_CH10 #3<br>PRS_CH11 #2<br>ACMP0_O #14<br>ACMP1_O #14 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PC10 | BUSBY BUSAX | TIM0_CC0 #15<br>TIM0_CC1 #14<br>TIM0_CC2 #13<br>TIM0_CDTI0 #12<br>TIM0_CDTI1 #11<br>TIM0_CDTI2 #10<br>TIM1_CC0 #15<br>TIM1_CC1 #14<br>TIM1_CC2 #13<br>TIM1_CC3 #12<br>WTIM0_CC0 #30<br>WTIM0_CC1 #28<br>WTIM0_CC2 #26<br>WTIM0_CDTI0 #22<br>WTIM0_CDTI1 #20<br>WTIM0_CDTI2 #18<br>LETIM0_OUT0 #15<br>LETIM0_OUT1 #14<br>PCNT0_S0IN #15<br>PCNT0_S1IN #14 | US0_TX #15<br>US0_RX #14<br>US0_CLK #13<br>US0_CS #12<br>US0_CTS #11<br>US0_RTS #10<br>US1_TX #15<br>US1_RX #14<br>US1_CLK #13<br>US1_CS #12<br>US1_CTS #11<br>US1_RTS #10<br>LEU0_TX #15<br>LEU0_RX #14<br>I2C0_SDA #15<br>I2C0_SCL #14 | FRC_DCLK #15<br>FRC_DOUT #14<br>FRC_DFRAME #13<br>MODEM_DCLK #15<br>MODEM_DIN #14<br>MODEM_DOUT #13<br>MODEM_ANT0 #12<br>MODEM_ANT1 #11 | CMU_CLK1 #3<br>PRS_CH0 #12<br>PRS_CH9 #15<br>PRS_CH10 #4<br>PRS_CH11 #3<br>ACMP0_O #15<br>ACMP1_O #15<br>GPIO_EM4WU12 |
| PC11 | BUSAY BUSBX | TIM0_CC0 #16<br>TIM0_CC1 #15<br>TIM0_CC2 #14<br>TIM0_CDTI0 #13<br>TIM0_CDTI1 #12<br>TIM0_CDTI2 #11<br>TIM1_CC0 #16<br>TIM1_CC1 #15<br>TIM1_CC2 #14<br>TIM1_CC3 #13<br>WTIM0_CC0 #31<br>WTIM0_CC1 #29<br>WTIM0_CC2 #27<br>WTIM0_CDTI0 #23<br>WTIM0_CDTI1 #21<br>WTIM0_CDTI2 #19<br>LETIM0_OUT0 #16<br>LETIM0_OUT1 #15<br>PCNT0_S0IN #16<br>PCNT0_S1IN #15 | US0_TX #16<br>US0_RX #15<br>US0_CLK #14<br>US0_CS #13<br>US0_CTS #12<br>US0_RTS #11<br>US1_TX #16<br>US1_RX #15<br>US1_CLK #14<br>US1_CS #13<br>US1_CTS #12<br>US1_RTS #11<br>LEU0_TX #16<br>LEU0_RX #15<br>I2C0_SDA #16<br>I2C0_SCL #15 | FRC_DCLK #16<br>FRC_DOUT #15<br>FRC_DFRAME #14<br>MODEM_DCLK #16<br>MODEM_DIN #15<br>MODEM_DOUT #14<br>MODEM_ANT0 #13<br>MODEM_ANT1 #12 | CMU_CLK0 #3<br>PRS_CH0 #13<br>PRS_CH9 #16<br>PRS_CH10 #5<br>PRS_CH11 #4<br>ACMP0_O #16<br>ACMP1_O #16<br>DBG_SWO #3 |
| PD9 | BUSCY BUSDX | TIM0_CC0 #17<br>TIM0_CC1 #16<br>TIM0_CC2 #15<br>TIM0_CDTI0 #14<br>TIM0_CDTI1 #13<br>TIM0_CDTI2 #12<br>TIM1_CC0 #17<br>TIM1_CC1 #16<br>TIM1_CC2 #15<br>TIM1_CC3 #14<br>WTIM0_CC1 #31<br>WTIM0_CC2 #29<br>WTIM0_CDTI0 #25<br>WTIM0_CDTI1 #23<br>WTIM0_CDTI2 #21<br>LETIM0_OUT0 #17<br>LETIM0_OUT1 #16<br>PCNT0_S0IN #17<br>PCNT0_S1IN #16 | US0_TX #17<br>US0_RX #16<br>US0_CLK #15<br>US0_CS #14<br>US0_CTS #13<br>US0_RTS #12<br>US1_TX #17<br>US1_RX #16<br>US1_CLK #15<br>US1_CS #14<br>US1_CTS #13<br>US1_RTS #12<br>LEU0_TX #17<br>LEU0_RX #16<br>I2C0_SDA #17<br>I2C0_SCL #16 | FRC_DCLK #17<br>FRC_DOUT #16<br>FRC_DFRAME #15<br>MODEM_DCLK #17<br>MODEM_DIN #16<br>MODEM_DOUT #15<br>MODEM_ANT0 #14<br>MODEM_ANT1 #13 | CMU_CLK0 #4<br>PRS_CH3 #8<br>PRS_CH4 #0<br>PRS_CH5 #6<br>PRS_CH6 #11<br>ACMP0_O #17<br>ACMP1_O #17<br>LES_CH1 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PD10 | BUSDY BUSCX | TIM0_CC0 #18<br>TIM0_CC1 #17<br>TIM0_CC2 #16<br>TIM0_CDTI0 #15<br>TIM0_CDTI1 #14<br>TIM0_CDTI2 #13<br>TIM1_CC0 #18<br>TIM1_CC1 #17<br>TIM1_CC2 #16<br>TIM1_CC3 #15<br>WTIM0_CC2 #30<br>WTIM0_CDTI0 #26<br>WTIM0_CDTI1 #24<br>WTIM0_CDTI2 #22<br>LETIM0_OUT0 #18<br>LETIM0_OUT1 #17<br>PCNT0_S0IN #18<br>PCNT0_S1IN #17 | US0_TX #18<br>US0_RX #17<br>US0_CLK #16<br>US0_CS #15<br>US0_CTS #14<br>US0_RTS #13<br>US1_TX #18<br>US1_RX #17<br>US1_CLK #16<br>US1_CS #15<br>US1_CTS #14<br>US1_RTS #13<br>LEU0_TX #18<br>LEU0_RX #17<br>I2C0_SDA #18<br>I2C0_SCL #17 | FRC_DCLK #18<br>FRC_DOUT #17<br>FRC_DFRAME #16<br>MODEM_DCLK #18<br>MODEM_DIN #17<br>MODEM_DOUT #16<br>MODEM_ANT0 #15<br>MODEM_ANT1 #14 | CMU_CLK1 #4<br>PRS_CH3 #9<br>PRS_CH4 #1<br>PRS_CH5 #0<br>PRS_CH6 #12<br>ACMP0_O #18<br>ACMP1_O #18<br>LES_CH2 |
| PD11 | BUSCY BUSDX | TIM0_CC0 #19<br>TIM0_CC1 #18<br>TIM0_CC2 #17<br>TIM0_CDTI0 #16<br>TIM0_CDTI1 #15<br>TIM0_CDTI2 #14<br>TIM1_CC0 #19<br>TIM1_CC1 #18<br>TIM1_CC2 #17<br>TIM1_CC3 #16<br>WTIM0_CC2 #31<br>WTIM0_CDTI0 #27<br>WTIM0_CDTI1 #25<br>WTIM0_CDTI2 #23<br>LETIM0_OUT0 #19<br>LETIM0_OUT1 #18<br>PCNT0_S0IN #19<br>PCNT0_S1IN #18 | US0_TX #19<br>US0_RX #18<br>US0_CLK #17<br>US0_CS #16<br>US0_CTS #15<br>US0_RTS #14<br>US1_TX #19<br>US1_RX #18<br>US1_CLK #17<br>US1_CS #16<br>US1_CTS #15<br>US1_RTS #14<br>LEU0_TX #19<br>LEU0_RX #18<br>I2C0_SDA #19<br>I2C0_SCL #18 | FRC_DCLK #19<br>FRC_DOUT #18<br>FRC_DFRAME #17<br>MODEM_DCLK #19<br>MODEM_DIN #18<br>MODEM_DOUT #17<br>MODEM_ANT0 #16<br>MODEM_ANT1 #15 | PRS_CH3 #10<br>PRS_CH4 #2<br>PRS_CH5 #1<br>PRS_CH6 #13<br>ACMP0_O #19<br>ACMP1_O #19<br>LES_CH3 |
| PD12 | VDAC0_OUT1ALT / OPA1_OUTALT #0<br>BUSDY BUSCX | TIM0_CC0 #20<br>TIM0_CC1 #19<br>TIM0_CC2 #18<br>TIM0_CDTI0 #17<br>TIM0_CDTI1 #16<br>TIM0_CDTI2 #15<br>TIM1_CC0 #20<br>TIM1_CC1 #19<br>TIM1_CC2 #18<br>TIM1_CC3 #17<br>WTIM0_CDTI0 #28<br>WTIM0_CDTI1 #26<br>WTIM0_CDTI2 #24<br>LETIM0_OUT0 #20<br>LETIM0_OUT1 #19<br>PCNT0_S0IN #20<br>PCNT0_S1IN #19 | US0_TX #20<br>US0_RX #19<br>US0_CLK #18<br>US0_CS #17<br>US0_CTS #16<br>US0_RTS #15<br>US1_TX #20<br>US1_RX #19<br>US1_CLK #18<br>US1_CS #17<br>US1_CTS #16<br>US1_RTS #15<br>LEU0_TX #20<br>LEU0_RX #19<br>I2C0_SDA #20<br>I2C0_SCL #19 | FRC_DCLK #20<br>FRC_DOUT #19<br>FRC_DFRAME #18<br>MODEM_DCLK #20<br>MODEM_DIN #19<br>MODEM_DOUT #18<br>MODEM_ANT0 #17<br>MODEM_ANT1 #16 | PRS_CH3 #11<br>PRS_CH4 #3<br>PRS_CH5 #2<br>PRS_CH6 #14<br>ACMP0_O #20<br>ACMP1_O #20<br>LES_CH4 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PD13 | VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P | TIM0_CC0 #21<br>TIM0_CC1 #20<br>TIM0_CC2 #19<br>TIM0_CDTI0 #18<br>TIM0_CDTI1 #17<br>TIM0_CDTI2 #16<br>TIM1_CC0 #21<br>TIM1_CC1 #20<br>TIM1_CC2 #19<br>TIM1_CC3 #18<br>WTIM0_CDTI0 #29<br>WTIM0_CDTI1 #27<br>WTIM0_CDTI2 #25<br>LETIM0_OUT0 #21<br>LETIM0_OUT1 #20<br>PCNT0_S0IN #21<br>PCNT0_S1IN #20 | US0_TX #21<br>US0_RX #20<br>US0_CLK #19<br>US0_CS #18<br>US0_CTS #17<br>US0_RTS #16<br>US1_TX #21<br>US1_RX #20<br>US1_CLK #19<br>US1_CS #18<br>US1_CTS #17<br>US1_RTS #16<br>LEU0_TX #21<br>LEU0_RX #20<br>I2C0_SDA #21<br>I2C0_SCL #20 | FRC_DCLK #21<br>FRC_DOUT #20<br>FRC_DFRAME #19<br>MODEM_DCLK #21<br>MODEM_DIN #20<br>MODEM_DOUT #19<br>MODEM_ANT0 #18<br>MODEM_ANT1 #17 | PRS_CH3 #12<br>PRS_CH4 #4<br>PRS_CH5 #3<br>PRS_CH6 #15<br>ACMP0_O #21<br>ACMP1_O #21<br>LES_CH5 |
| PD14 | BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT | TIM0_CC0 #22<br>TIM0_CC1 #21<br>TIM0_CC2 #20<br>TIM0_CDTI0 #19<br>TIM0_CDTI1 #18<br>TIM0_CDTI2 #17<br>TIM1_CC0 #22<br>TIM1_CC1 #21<br>TIM1_CC2 #20<br>TIM1_CC3 #19<br>WTIM0_CDTI0 #30<br>WTIM0_CDTI1 #28<br>WTIM0_CDTI2 #26<br>LETIM0_OUT0 #22<br>LETIM0_OUT1 #21<br>PCNT0_S0IN #22<br>PCNT0_S1IN #21 | US0_TX #22<br>US0_RX #21<br>US0_CLK #20<br>US0_CS #19<br>US0_CTS #18<br>US0_RTS #17<br>US1_TX #22<br>US1_RX #21<br>US1_CLK #20<br>US1_CS #19<br>US1_CTS #18<br>US1_RTS #17<br>LEU0_TX #22<br>LEU0_RX #21<br>I2C0_SDA #22<br>I2C0_SCL #21 | FRC_DCLK #22<br>FRC_DOUT #21<br>FRC_DFRAME #20<br>MODEM_DCLK #22<br>MODEM_DIN #21<br>MODEM_DOUT #20<br>MODEM_ANT0 #19<br>MODEM_ANT1 #18 | CMU_CLK0 #5<br>PRS_CH3 #13<br>PRS_CH4 #5<br>PRS_CH5 #4<br>PRS_CH6 #16<br>ACMP0_O #22<br>ACMP1_O #22<br>LES_CH6<br>GPIO_EM4WU4 |
| PD15 | VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N | TIM0_CC0 #23<br>TIM0_CC1 #22<br>TIM0_CC2 #21<br>TIM0_CDTI0 #20<br>TIM0_CDTI1 #19<br>TIM0_CDTI2 #18<br>TIM1_CC0 #23<br>TIM1_CC1 #22<br>TIM1_CC2 #21<br>TIM1_CC3 #20<br>WTIM0_CDTI0 #31<br>WTIM0_CDTI1 #29<br>WTIM0_CDTI2 #27<br>LETIM0_OUT0 #23<br>LETIM0_OUT1 #22<br>PCNT0_S0IN #23<br>PCNT0_S1IN #22 | US0_TX #23<br>US0_RX #22<br>US0_CLK #21<br>US0_CS #20<br>US0_CTS #19<br>US0_RTS #18<br>US1_TX #23<br>US1_RX #22<br>US1_CLK #21<br>US1_CS #20<br>US1_CTS #19<br>US1_RTS #18<br>LEU0_TX #23<br>LEU0_RX #22<br>I2C0_SDA #23<br>I2C0_SCL #22 | FRC_DCLK #23<br>FRC_DOUT #22<br>FRC_DFRAME #21<br>MODEM_DCLK #23<br>MODEM_DIN #22<br>MODEM_DOUT #21<br>MODEM_ANT0 #20<br>MODEM_ANT1 #19 | CMU_CLK1 #5<br>PRS_CH3 #14<br>PRS_CH4 #6<br>PRS_CH5 #5<br>PRS_CH6 #17<br>ACMP0_O #23<br>ACMP1_O #23<br>LES_CH7<br>DBG_SWO #2 |

Not Recommended For New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PF0 | BUSBY BUSAX | TIM0_CC0 #24<br>TIM0_CC1 #23<br>TIM0_CC2 #22<br>TIM0_CDTI0 #21<br>TIM0_CDTI1 #20<br>TIM0_CDTI2 #19<br>TIM1_CC0 #24<br>TIM1_CC1 #23<br>TIM1_CC2 #22<br>TIM1_CC3 #21<br>WTIM0_CDTI1 #30<br>WTIM0_CDTI2 #28<br>LETIM0_OUT0 #24<br>LETIM0_OUT1 #23<br>PCNT0_S0IN #24<br>PCNT0_S1IN #23 | US0_TX #24<br>US0_RX #23<br>US0_CLK #22<br>US0_CS #21<br>US0_CTS #20<br>US0_RTS #19<br>US1_TX #24<br>US1_RX #23<br>US1_CLK #22<br>US1_CS #21<br>US1_CTS #20<br>US1_RTS #19<br>LEU0_TX #24<br>LEU0_RX #23<br>I2C0_SDA #24<br>I2C0_SCL #23 | FRC_DCLK #24<br>FRC_DOUT #23<br>FRC_DFRAME #22<br>MODEM_DCLK #24<br>MODEM_DIN #23<br>MODEM_DOUT #22<br>MODEM_ANT0 #21<br>MODEM_ANT1 #20 | PRS_CH0 #0<br>PRS_CH1 #7<br>PRS_CH2 #6<br>PRS_CH3 #5<br>ACMP0_O #24<br>ACMP1_O #24<br>DBG_SWCLKTCK<br>BOOT_TX |
| PF1 | BUSAY BUSBX | TIM0_CC0 #25<br>TIM0_CC1 #24<br>TIM0_CC2 #23<br>TIM0_CDTI0 #22<br>TIM0_CDTI1 #21<br>TIM0_CDTI2 #20<br>TIM1_CC0 #25<br>TIM1_CC1 #24<br>TIM1_CC2 #23<br>TIM1_CC3 #22<br>WTIM0_CDTI1 #31<br>WTIM0_CDTI2 #29<br>LETIM0_OUT0 #25<br>LETIM0_OUT1 #24<br>PCNT0_S0IN #25<br>PCNT0_S1IN #24 | US0_TX #25<br>US0_RX #24<br>US0_CLK #23<br>US0_CS #22<br>US0_CTS #21<br>US0_RTS #20<br>US1_TX #25<br>US1_RX #24<br>US1_CLK #23<br>US1_CS #22<br>US1_CTS #21<br>US1_RTS #20<br>LEU0_TX #25<br>LEU0_RX #24<br>I2C0_SDA #25<br>I2C0_SCL #24 | FRC_DCLK #25<br>FRC_DOUT #24<br>FRC_DFRAME #23<br>MODEM_DCLK #25<br>MODEM_DIN #24<br>MODEM_DOUT #23<br>MODEM_ANT0 #22<br>MODEM_ANT1 #21 | PRS_CH0 #1<br>PRS_CH1 #0<br>PRS_CH2 #7<br>PRS_CH3 #6<br>ACMP0_O #25<br>ACMP1_O #25<br>DBG_SWDIOTMS<br>BOOT_RX |
| PF2 | BUSBY BUSAX | TIM0_CC0 #26<br>TIM0_CC1 #25<br>TIM0_CC2 #24<br>TIM0_CDTI0 #23<br>TIM0_CDTI1 #22<br>TIM0_CDTI2 #21<br>TIM1_CC0 #26<br>TIM1_CC1 #25<br>TIM1_CC2 #24<br>TIM1_CC3 #23<br>WTIM0_CDTI2 #30<br>LETIM0_OUT0 #26<br>LETIM0_OUT1 #25<br>PCNT0_S0IN #26<br>PCNT0_S1IN #25 | US0_TX #26<br>US0_RX #25<br>US0_CLK #24<br>US0_CS #23<br>US0_CTS #22<br>US0_RTS #21<br>US1_TX #26<br>US1_RX #25<br>US1_CLK #24<br>US1_CS #23<br>US1_CTS #22<br>US1_RTS #21<br>LEU0_TX #26<br>LEU0_RX #25<br>I2C0_SDA #26<br>I2C0_SCL #25 | FRC_DCLK #26<br>FRC_DOUT #25<br>FRC_DFRAME #24<br>MODEM_DCLK #26<br>MODEM_DIN #25<br>MODEM_DOUT #24<br>MODEM_ANT0 #23<br>MODEM_ANT1 #22 | CMU_CLK0 #6<br>PRS_CH0 #2<br>PRS_CH1 #1<br>PRS_CH2 #0<br>PRS_CH3 #7<br>ACMP0_O #26<br>ACMP1_O #26<br>DBG_TDO<br>DBG_SWO #0<br>GPIO_EM4WU0 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PF3 | BUSAY BUSBX | TIM0_CC0 #27<br>TIM0_CC1 #26<br>TIM0_CC2 #25<br>TIM0_CDTI0 #24<br>TIM0_CDTI1 #23<br>TIM0_CDTI2 #22<br>TIM1_CC0 #27<br>TIM1_CC1 #26<br>TIM1_CC2 #25<br>TIM1_CC3 #24<br>WTIM0_CDTI2 #31<br>LETIM0_OUT0 #27<br>LETIM0_OUT1 #26<br>PCNT0_S0IN #27<br>PCNT0_S1IN #26 | US0_TX #27<br>US0_RX #26<br>US0_CLK #25<br>US0_CS #24<br>US0_CTS #23<br>US0_RTS #22<br>US1_TX #27<br>US1_RX #26<br>US1_CLK #25<br>US1_CS #24<br>US1_CTS #23<br>US1_RTS #22<br>LEU0_TX #27<br>LEU0_RX #26<br>I2C0_SDA #27<br>I2C0_SCL #26 | FRC_DCLK #27<br>FRC_DOUT #26<br>FRC_DFRAME #25<br>MODEM_DCLK #27<br>MODEM_DIN #26<br>MODEM_DOUT #25<br>MODEM_ANT0 #24<br>MODEM_ANT1 #23 | CMU_CLK1 #6<br>PRS_CH0 #3<br>PRS_CH1 #2<br>PRS_CH2 #1<br>PRS_CH3 #0<br>ACMP0_O #27<br>ACMP1_O #27<br>DBG_TDI |
| PF4 | BUSBY BUSAX | TIM0_CC0 #28<br>TIM0_CC1 #27<br>TIM0_CC2 #26<br>TIM0_CDTI0 #25<br>TIM0_CDTI1 #24<br>TIM0_CDTI2 #23<br>TIM1_CC0 #28<br>TIM1_CC1 #27<br>TIM1_CC2 #26<br>TIM1_CC3 #25 LE-<br>TIM0_OUT0 #28 LE-<br>TIM0_OUT1 #27<br>PCNT0_S0IN #28<br>PCNT0_S1IN #27 | US0_TX #28<br>US0_RX #27<br>US0_CLK #26<br>US0_CS #25<br>US0_CTS #24<br>US0_RTS #23<br>US1_TX #28<br>US1_RX #27<br>US1_CLK #26<br>US1_CS #25<br>US1_CTS #24<br>US1_RTS #23<br>LEU0_TX #28<br>LEU0_RX #27<br>I2C0_SDA #28<br>I2C0_SCL #27 | FRC_DCLK #28<br>FRC_DOUT #27<br>FRC_DFRAME #26<br>MODEM_DCLK #28<br>MODEM_DIN #27<br>MODEM_DOUT #26<br>MODEM_ANT0 #25<br>MODEM_ANT1 #24 | PRS_CH0 #4<br>PRS_CH1 #3<br>PRS_CH2 #2<br>PRS_CH3 #1<br>ACMP0_O #28<br>ACMP1_O #28 |
| PF5 | BUSAY BUSBX | TIM0_CC0 #29<br>TIM0_CC1 #28<br>TIM0_CC2 #27<br>TIM0_CDTI0 #26<br>TIM0_CDTI1 #25<br>TIM0_CDTI2 #24<br>TIM1_CC0 #29<br>TIM1_CC1 #28<br>TIM1_CC2 #27<br>TIM1_CC3 #26 LE-<br>TIM0_OUT0 #29 LE-<br>TIM0_OUT1 #28<br>PCNT0_S0IN #29<br>PCNT0_S1IN #28 | US0_TX #29<br>US0_RX #28<br>US0_CLK #27<br>US0_CS #26<br>US0_CTS #25<br>US0_RTS #24<br>US1_TX #29<br>US1_RX #28<br>US1_CLK #27<br>US1_CS #26<br>US1_CTS #25<br>US1_RTS #24<br>LEU0_TX #29<br>LEU0_RX #28<br>I2C0_SDA #29<br>I2C0_SCL #28 | FRC_DCLK #29<br>FRC_DOUT #28<br>FRC_DFRAME #27<br>MODEM_DCLK #29<br>MODEM_DIN #28<br>MODEM_DOUT #27<br>MODEM_ANT0 #26<br>MODEM_ANT1 #25 | PRS_CH0 #5<br>PRS_CH1 #4<br>PRS_CH2 #3<br>PRS_CH3 #2<br>ACMP0_O #29<br>ACMP1_O #29 |

Not Recommended for New Designs

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | Timers | Communication | Radio | Other |
| PF6 | BUSBY BUSAX | TIM0_CC0 #30<br>TIM0_CC1 #29<br>TIM0_CC2 #28<br>TIM0_CDTI0 #27<br>TIM0_CDTI1 #26<br>TIM0_CDTI2 #25<br>TIM1_CC0 #30<br>TIM1_CC1 #29<br>TIM1_CC2 #28<br>TIM1_CC3 #27 LE-<br>TIM0_OUT0 #30 LE-<br>TIM0_OUT1 #29<br>PCNT0_S0IN #30<br>PCNT0_S1IN #29 | US0_TX #30<br>US0_RX #29<br>US0_CLK #28<br>US0_CS #27<br>US0_CTS #26<br>US0_RTS #25<br>US1_TX #30<br>US1_RX #29<br>US1_CLK #28<br>US1_CS #27<br>US1_CTS #26<br>US1_RTS #25<br>LEU0_TX #30<br>LEU0_RX #29<br>I2C0_SDA #30<br>I2C0_SCL #29 | FRC_DCLK #30<br>FRC_DOUT #29<br>FRC_DFRAME #28<br>MODEM_DCLK #30<br>MODEM_DIN #29<br>MODEM_DOUT #28<br>MODEM_ANT0 #27<br>MODEM_ANT1 #26 | CMU_CLK1 #7<br>PRS_CH0 #6<br>PRS_CH1 #5<br>PRS_CH2 #4<br>PRS_CH3 #3<br>ACMP0_O #30<br>ACMP1_O #30 |
| PF7 | BUSAY BUSBX | TIM0_CC0 #31<br>TIM0_CC1 #30<br>TIM0_CC2 #29<br>TIM0_CDTI0 #28<br>TIM0_CDTI1 #27<br>TIM0_CDTI2 #26<br>TIM1_CC0 #31<br>TIM1_CC1 #30<br>TIM1_CC2 #29<br>TIM1_CC3 #28 LE-<br>TIM0_OUT0 #31 LE-<br>TIM0_OUT1 #30<br>PCNT0_S0IN #31<br>PCNT0_S1IN #30 | US0_TX #31<br>US0_RX #30<br>US0_CLK #29<br>US0_CS #28<br>US0_CTS #27<br>US0_RTS #26<br>US1_TX #31<br>US1_RX #30<br>US1_CLK #29<br>US1_CS #28<br>US1_CTS #27<br>US1_RTS #26<br>LEU0_TX #31<br>LEU0_RX #30<br>I2C0_SDA #31<br>I2C0_SCL #30 | FRC_DCLK #31<br>FRC_DOUT #30<br>FRC_DFRAME #29<br>MODEM_DCLK #31<br>MODEM_DIN #30<br>MODEM_DOUT #29<br>MODEM_ANT0 #28<br>MODEM_ANT1 #27 | CMU_CLKI0 #1<br>CMU_CLK0 #7<br>PRS_CH0 #7<br>PRS_CH1 #6<br>PRS_CH2 #5<br>PRS_CH3 #4<br>ACMP0_O #31<br>ACMP1_O #31<br>GPIO_EM4WU1 |

Not Recommended for New Designs

### 6.6 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 6.5 GPIO Functionality Table for a list of functions available on each GPIO pin.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 6.6. Alternate Functionality Overview**

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| ACMP0_O | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Analog comparator ACMP0, digital output. |
| ACMP1_O | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Analog comparator ACMP1, digital output. |
| ADC0_EXTN | 0: PA0 | | | | | | | | Analog to digital converter ADC0 external reference input negative pin. |
| ADC0_EXTP | 0: PA1 | | | | | | | | Analog to digital converter ADC0 external reference input positive pin. |
| BOOT_RX | 0: PF1 | | | | | | | | Bootloader RX. |
| BOOT_TX | 0: PF0 | | | | | | | | Bootloader TX. |
| CMU_CLK0 | 0: PA1<br>1: PB15<br>2: PC6<br>3: PC11 | 4: PD9<br>5: PD14<br>6: PF2<br>7: PF7 | | | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA0<br>1: PB14<br>2: PC7<br>3: PC10 | 4: PD10<br>5: PD15<br>6: PF3<br>7: PF6 | | | | | | | Clock Management Unit, clock output number 1. |
| CMU_CLKI0 | 0: PB13<br>1: PF7<br>2: PC6 | 4: PA5 | | | | | | | Clock Management Unit, clock input number 0. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| DBG_SWCLKTCK | 0: PF0 | | | | | | | | Debug-interface Serial Wire clock input and JTAG Test Clock.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull down. |
| DBG_SWDIOTMS | 0: PF1 | | | | | | | | Debug-interface Serial Wire data input / output and JTAG Test Mode Select.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull up. |
| DBG_SWO | 0: PF2<br>1: PB13<br>2: PD15<br>3: PC11 | | | | | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| DBG_TDI | 0: PF3 | | | | | | | | Debug-interface JTAG Test Data In.<br>Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active. |
| DBG_TDO | 0: PF2 | | | | | | | | Debug-interface JTAG Test Data Out.<br>Note that this function becomes available after the first valid JTAG command is received. |
| FRC_DCLK | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Frame Controller, Data Sniffer Clock. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| FRC_DFRAME | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Frame Controller, Data Sniffer Frame active |
| FRC_DOUT | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Frame Controller, Data Sniffer Output. |
| GPIO_EM4WU0 | 0: PF2 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PF7 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PD14 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU8 | 0: PA3 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU9 | 0: PB13 | | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU12 | 0: PC10 | | | | | | | | Pin can be used to wake the system up from EM4 |
| I2C0_SCL | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | I2C0 Serial Data input / output. |
| LES_CH1 | 0: PD9 | | | | | | | | LESENSE channel 1. |
| LES_CH2 | 0: PD10 | | | | | | | | LESENSE channel 2. |
| LES_CH3 | 0: PD11 | | | | | | | | LESENSE channel 3. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| LES_CH4 | 0: PD12 | | | | | | | | LESENSE channel 4. |
| LES_CH5 | 0: PD13 | | | | | | | | LESENSE channel 5. |
| LES_CH6 | 0: PD14 | | | | | | | | LESENSE channel 6. |
| LES_CH7 | 0: PD15 | | | | | | | | LESENSE channel 7. |
| LES_CH8 | 0: PA0 | | | | | | | | LESENSE channel 8. |
| LES_CH9 | 0: PA1 | | | | | | | | LESENSE channel 9. |
| LES_CH10 | 0: PA2 | | | | | | | | LESENSE channel 10. |
| LES_CH11 | 0: PA3 | | | | | | | | LESENSE channel 11. |
| LES_CH12 | 0: PA4 | | | | | | | | LESENSE channel 12. |
| LES_CH13 | 0: PA5 | | | | | | | | LESENSE channel 13. |
| LETIM0_OUT0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | LEUART0 Receive input. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| LEU0_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | 0: PB14 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | 0: PB15 | | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| MODEM_ANT0 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11<br>14: PD9<br>15: PD10 | 16: PD11<br>17: PD12<br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | MODEM antenna control output 0, used for antenna diversity. |
| MODEM_ANT1 | 0: PA4<br>1: PA5<br>2: PB11<br>3: PB12 | 4: PB13<br>5: PB14<br>6: PB15<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11<br>13: PD9<br>14: PD10<br>15: PD11 | 16: PD12<br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | MODEM antenna control output 1, used for antenna diversity. |
| MODEM_DCLK | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | MODEM data clock out. |
| MODEM_DIN | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | MODEM data in. |
| MODEM_DOUT | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | MODEM data out. |
| OPA0_N | 0: PA4 | | | | | | | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PA2 | | | | | | | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD15 | | | | | | | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD13 | | | | | | | | Operational Amplifier 1 external positive input. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PCNT0_S0IN | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | 0: PF0<br>1: PF1<br>2: PF2<br>3: PF3 | 4: PF4<br>5: PF5<br>6: PF6<br>7: PF7 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11 | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | 0: PF1<br>1: PF2<br>2: PF3<br>3: PF4 | 4: PF5<br>5: PF6<br>6: PF7<br>7: PF0 | | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | 0: PF2<br>1: PF3<br>2: PF4<br>3: PF5 | 4: PF6<br>5: PF7<br>6: PF0<br>7: PF1 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | 0: PF3<br>1: PF4<br>2: PF5<br>3: PF6 | 4: PF7<br>5: PF0<br>6: PF1<br>7: PF2 | 8: PD9<br>9: PD10<br>10: PD11<br>11: PD12 | 12: PD13<br>13: PD14<br>14: PD15 | | | | | Peripheral Reflex System PRS, channel 3. |
| PRS_CH4 | 0: PD9<br>1: PD10<br>2: PD11<br>3: PD12 | 4: PD13<br>5: PD14<br>6: PD15 | | | | | | | Peripheral Reflex System PRS, channel 4. |
| PRS_CH5 | 0: PD10<br>1: PD11<br>2: PD12<br>3: PD13 | 4: PD14<br>5: PD15<br>6: PD9 | | | | | | | Peripheral Reflex System PRS, channel 5. |
| PRS_CH6 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PD9 | 12: PD10<br>13: PD11<br>14: PD12<br>15: PD13 | 16: PD14<br>17: PD15 | | | | Peripheral Reflex System PRS, channel 6. |
| PRS_CH7 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PA0 | | | | | | Peripheral Reflex System PRS, channel 7. |
| PRS_CH8 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PA0<br>10: PA1 | | | | | | Peripheral Reflex System PRS, channel 8. |
| PRS_CH9 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PA0<br>9: PA1<br>10: PA2<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11 | | | | Peripheral Reflex System PRS, channel 9. |
| PRS_CH10 | 0: PC6<br>1: PC7<br>2: PC8<br>3: PC9 | 4: PC10<br>5: PC11 | | | | | | | Peripheral Reflex System PRS, channel 10. |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| PRS_CH11 | 0: PC7<br>1: PC8<br>2: PC9<br>3: PC10 | 4: PC11<br>5: PC6 | | | | | | | Peripheral Reflex System PRS, channel 11. |
| TIM0_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11<br>14: PD9<br>15: PD10 | 16: PD11<br>17: PD12<br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | Timer 0 Complimentary Dead Time Insertion channel 0. |
| TIM0_CDTI1 | 0: PA4<br>1: PA5<br>2: PB11<br>3: PB12 | 4: PB13<br>5: PB14<br>6: PB15<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11<br>13: PD9<br>14: PD10<br>15: PD11 | 16: PD12<br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | Timer 0 Complimentary Dead Time Insertion channel 1. |
| TIM0_CDTI2 | 0: PA5<br>1: PB11<br>2: PB12<br>3: PB13 | 4: PB14<br>5: PB15<br>6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | 12: PD9<br>13: PD10<br>14: PD11<br>15: PD12 | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | Timer 0 Complimentary Dead Time Insertion channel 2. |
| TIM1_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | Timer 1 Capture Compare input / output channel 2. |
| TIM1_CC3 | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11<br>14: PD9<br>15: PD10 | 16: PD11<br>17: PD12<br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | Timer 1 Capture Compare input / output channel 3. |
| US0_CLK | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | USART0 clock input / output. |
| US0_CS | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11<br>14: PD9<br>15: PD10 | 16: PD11<br>17: PD12<br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | USART0 chip select input / output. |

Not Recommended for New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US0_CTS | 0: PA4<br>1: PA5<br>2: PB11<br>3: PB12 | 4: PB13<br>5: PB14<br>6: PB15<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11<br>13: PD9<br>14: PD10<br>15: PD11 | 16: PD12<br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | USART0 Clear To Send hardware flow control input. |
| US0_RTS | 0: PA5<br>1: PB11<br>2: PB12<br>3: PB13 | 4: PB14<br>5: PB15<br>6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | 12: PD9<br>13: PD10<br>14: PD11<br>15: PD12 | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | USART0 Request To Send hardware flow control output. |
| US0_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | 4: PB11<br>5: PB12<br>6: PB13<br>7: PB14 | 8: PB15<br>9: PC6<br>10: PC7<br>11: PC8 | 12: PC9<br>13: PC10<br>14: PC11<br>15: PD9 | 16: PD10<br>17: PD11<br>18: PD12<br>19: PD13 | 20: PD14<br>21: PD15<br>22: PF0<br>23: PF1 | 24: PF2<br>25: PF3<br>26: PF4<br>27: PF5 | 28: PF6<br>29: PF7<br>30: PA0<br>31: PA1 | USART1 clock input / output. |
| US1_CS | 0: PA3<br>1: PA4<br>2: PA5<br>3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | 8: PC6<br>9: PC7<br>10: PC8<br>11: PC9 | 12: PC10<br>13: PC11<br>14: PD9<br>15: PD10 | 16: PD11<br>17: PD12<br>18: PD13<br>19: PD14 | 20: PD15<br>21: PF0<br>22: PF1<br>23: PF2 | 24: PF3<br>25: PF4<br>26: PF5<br>27: PF6 | 28: PF7<br>29: PA0<br>30: PA1<br>31: PA2 | USART1 chip select input / output. |
| US1_CTS | 0: PA4<br>1: PA5<br>2: PB11<br>3: PB12 | 4: PB13<br>5: PB14<br>6: PB15<br>7: PC6 | 8: PC7<br>9: PC8<br>10: PC9<br>11: PC10 | 12: PC11<br>13: PD9<br>14: PD10<br>15: PD11 | 16: PD12<br>17: PD13<br>18: PD14<br>19: PD15 | 20: PF0<br>21: PF1<br>22: PF2<br>23: PF3 | 24: PF4<br>25: PF5<br>26: PF6<br>27: PF7 | 28: PA0<br>29: PA1<br>30: PA2<br>31: PA3 | USART1 Clear To Send hardware flow control input. |
| US1_RTS | 0: PA5<br>1: PB11<br>2: PB12<br>3: PB13 | 4: PB14<br>5: PB15<br>6: PC6<br>7: PC7 | 8: PC8<br>9: PC9<br>10: PC10<br>11: PC11 | 12: PD9<br>13: PD10<br>14: PD11<br>15: PD12 | 16: PD13<br>17: PD14<br>18: PD15<br>19: PF0 | 20: PF1<br>21: PF2<br>22: PF3<br>23: PF4 | 24: PF5<br>25: PF6<br>26: PF7<br>27: PA0 | 28: PA1<br>29: PA2<br>30: PA3<br>31: PA4 | USART1 Request To Send hardware flow control output. |
| US1_RX | 0: PA1<br>1: PA2<br>2: PA3<br>3: PA4 | 4: PA5<br>5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15<br>10: PC6<br>11: PC7 | 12: PC8<br>13: PC9<br>14: PC10<br>15: PC11 | 16: PD9<br>17: PD10<br>18: PD11<br>19: PD12 | 20: PD13<br>21: PD14<br>22: PD15<br>23: PF0 | 24: PF1<br>25: PF2<br>26: PF3<br>27: PF4 | 28: PF5<br>29: PF6<br>30: PF7<br>31: PA0 | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |

Not Recommended For New Designs

| Alternate | LOCATION | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | 8 - 11 | 12 - 15 | 16 - 19 | 20 - 23 | 24 - 27 | 28 - 31 | Description |
| US1_TX | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5<br>6: PB11<br>7: PB12 | 8: PB13<br>9: PB14<br>10: PB15<br>11: PC6 | 12: PC7<br>13: PC8<br>14: PC9<br>15: PC10 | 16: PC11<br>17: PD9<br>18: PD10<br>19: PD11 | 20: PD12<br>21: PD13<br>22: PD14<br>23: PD15 | 24: PF0<br>25: PF1<br>26: PF2<br>27: PF3 | 28: PF4<br>29: PF5<br>30: PF6<br>31: PF7 | USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| VDAC0_EXT | 0: PA1 | | | | | | | | Digital to analog converter VDAC0 external reference input pin. |
| VDAC0_OUT0 / OPA0_OUT | 0: PA3 | | | | | | | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUTALT | 0: PA5<br>1: PD13<br>2: PD15 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 0. |
| VDAC0_OUT1 / OPA1_OUT | 0: PD14 | | | | | | | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1ALT / OPA1_OUTALT | 0: PD12<br>1: PA2<br>2: PA4 | | | | | | | | Digital to Analog Converter DAC0 alternative output for channel 1. |
| WTIM0_CC0 | 0: PA0<br>1: PA1<br>2: PA2<br>3: PA3 | 4: PA4<br>5: PA5 | | 15: PB11 | 16: PB12<br>17: PB13<br>18: PB14<br>19: PB15 | | 26: PC6<br>27: PC7 | 28: PC8<br>29: PC9<br>30: PC10<br>31: PC11 | Wide timer 0 Capture Compare input / output channel 0. |
| WTIM0_CC1 | 0: PA2<br>1: PA3<br>2: PA4<br>3: PA5 | | 13: PB11<br>14: PB12<br>15: PB13 | | 16: PB14<br>17: PB15 | | 24: PC6<br>25: PC7<br>26: PC8<br>27: PC9 | 28: PC10<br>29: PC11<br>31: PD9 | Wide timer 0 Capture Compare input / output channel 1. |
| WTIM0_CC2 | 0: PA4<br>1: PA5 | | 11: PB11 | 12: PB12<br>13: PB13<br>14: PB14<br>15: PB15 | | 22: PC6<br>23: PC7 | 24: PC8<br>25: PC9<br>26: PC10<br>27: PC11 | 29: PD9<br>30: PD10<br>31: PD11 | Wide timer 0 Capture Compare input / output channel 2. |
| WTIM0_CDTI0 | | 7: PB11 | 8: PB12<br>9: PB13<br>10: PB14<br>11: PB15 | | 18: PC6<br>19: PC7 | 20: PC8<br>21: PC9<br>22: PC10<br>23: PC11 | 25: PD9<br>26: PD10<br>27: PD11 | 28: PD12<br>29: PD13<br>30: PD14<br>31: PD15 | Wide timer 0 Complimentary Dead Time Insertion channel 0. |
| WTIM0_CDTI1 | | 5: PB11<br>6: PB12<br>7: PB13 | 8: PB14<br>9: PB15 | | 16: PC6<br>17: PC7<br>18: PC8<br>19: PC9 | 20: PC10<br>21: PC11<br>23: PD9 | 24: PD10<br>25: PD11<br>26: PD12<br>27: PD13 | 28: PD14<br>29: PD15<br>30: PF0<br>31: PF1 | Wide timer 0 Complimentary Dead Time Insertion channel 1. |
| WTIM0_CDTI2 | 3: PB11 | 4: PB12<br>5: PB13<br>6: PB14<br>7: PB15 | | 14: PC6<br>15: PC7 | 16: PC8<br>17: PC9<br>18: PC10<br>19: PC11 | 21: PD9<br>22: PD10<br>23: PD11 | 24: PD12<br>25: PD13<br>26: PD14<br>27: PD15 | 28: PF0<br>29: PF1<br>30: PF2<br>31: PF3 | Wide timer 0 Complimentary Dead Time Insertion channel 2. |

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Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

**Table 6.7. Alternate Functionality Priority**

| Alternate Functionality | Location | Priority |
|---|---|---|
| CMU_CLKI0 | 1: PF7 | High Speed |

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### 6.7 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 6.5 APORT Connection Diagram on page 143 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

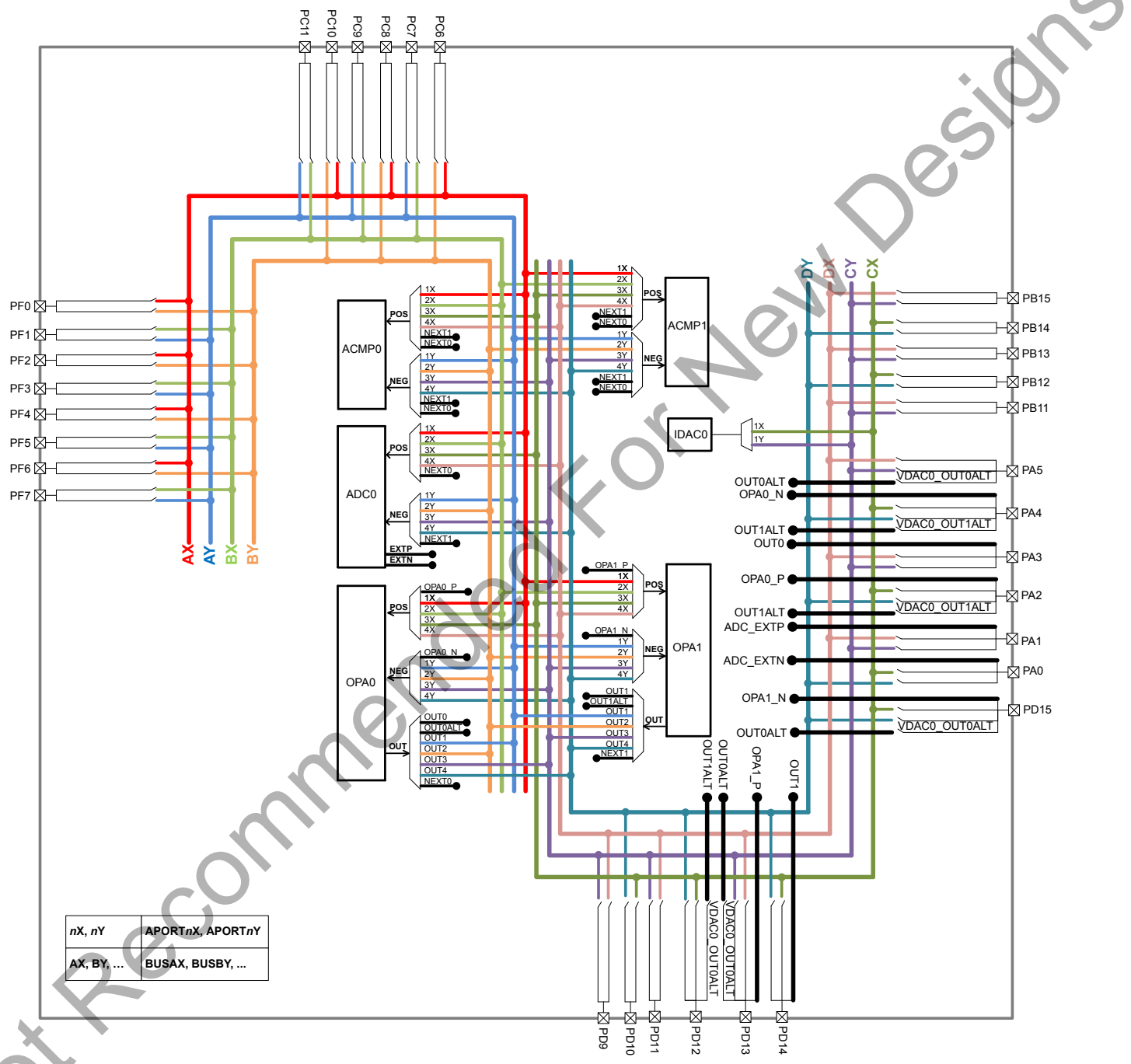


**Figure 6.5. APORT Connection Diagram**

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

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PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

**Table 6.8. ACMP0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT1X | BUSAX | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2X | BUSBX | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |

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**Table 6.9. ACMP1 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT1X | BUSAX | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2X | BUSBX | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |

Not Recommended For New Designs

**Table 6.10. ADC0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT1X | BUSAX | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2X | BUSBX | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |

**Table 6.11. IDAC0 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT1X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| APORT1Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |

Not Recommended For New Designs

**Table 6.12. VDAC0 / OPA Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OPA0_N** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| **OPA0_P** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT2X | BUSBX | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT3X | BUSCX | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |
| APORT4X | BUSDX | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |

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| Port | OPA1_N | | | | OPA1_P | | | | VDAC0_OUT0 / OPA0_OUT | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bus | APORT1Y | APORT2Y | APORT3Y | APORT4Y | APORT1X | APORT2X | APORT3X | APORT4X | APORT1Y | APORT2Y | APORT3Y | APORT4Y |
| | BUSAY | BUSBY | BUSCY | BUSDY | BUSAX | BUSBX | BUSCX | BUSDX | BUSAY | BUSBY | BUSCY | BUSDY |
| CH31 | | | PB15 | | | | | PB15 | | | PB15 | |
| CH30 | | | | PB14 | | | PB14 | | | | | PB14 |
| CH29 | | | PB13 | | | | | PB13 | | | PB13 | |
| CH28 | | | | PB12 | | | PB12 | | | | | PB12 |
| CH27 | | | PB11 | | | | | PB11 | | | PB11 | |
| CH26 | | | | | | | | | | | | |
| CH25 | | | | | | | | | | | | |
| CH24 | | | | | | | | | | | | |
| CH23 | PF7 | | | | | PF7 | | | PF7 | | | |
| CH22 | | PF6 | | | PF6 | | | | | PF6 | | |
| CH21 | PF5 | | | | | PF5 | | | PF5 | | | |
| CH20 | | PF4 | | | PF4 | | | | | PF4 | | |
| CH19 | PF3 | | | | | PF3 | | | PF3 | | | |
| CH18 | | PF2 | | | PF2 | | | | | PF2 | | |
| CH17 | PF1 | | | | | PF1 | | | PF1 | | | |
| CH16 | | PF0 | | | PF0 | | | | | PF0 | | |
| CH15 | | | | | | | | | | | | |
| CH14 | | | | | | | | | | | | |
| CH13 | | | PA5 | | | | | PA5 | | | PA5 | |
| CH12 | | | | PA4 | | | PA4 | | | | | PA4 |
| CH11 | PC11 | | PA3 | | | PC11 | | PA3 | PC11 | | PA3 | |
| CH10 | | PC10 | | PA2 | PC10 | | PA2 | | | PC10 | | PA2 |
| CH9 | PC9 | | PA1 | | | PC9 | | PA1 | PC9 | | PA1 | |
| CH8 | | PC8 | | PA0 | PC8 | | PA0 | | | PC8 | | PA0 |
| CH7 | PC7 | | PD15 | | | PC7 | | PD15 | PC7 | | PD15 | |
| CH6 | | PC6 | | PD14 | PC6 | | PD14 | | | PC6 | | PD14 |
| CH5 | | | PD13 | | | | PD13 | | | | PD13 | |
| CH4 | | | | PD12 | | | PD12 | | | | | PD12 |
| CH3 | | | PD11 | | | | PD11 | | | | PD11 | |
| CH2 | | | | PD10 | | | PD10 | | | | | PD10 |
| CH1 | | | | | | | | | | | | |
| CH0 | | | | | | | | | | | | |

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| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **VDAC0_OUT1 / OPA1_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | | | | | | | | | PF7 | | PF5 | | PF3 | | PF1 | | | | | | PC11 | | PC9 | | PC7 | | | | | | | |
| APORT2Y | BUSBY | | | | | | | | | | PF6 | | PF4 | | PF2 | | PF0 | | | | | | PC10 | | PC8 | | PC6 | | | | | | |
| APORT3Y | BUSCY | PB15 | | PB13 | | PB11 | | | | | | | | | | | | | | PA5 | | PA3 | | PA1 | | PD15 | | PD13 | | PD11 | | | |
| APORT4Y | BUSDY | | PB14 | | PB12 | | | | | | | | | | | | | | | | PA4 | | PA2 | | PA0 | | PD14 | | PD12 | | PD10 | | |

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# 7. QFN48 Package Specifications

## 7.1 QFN48 Package Dimensions

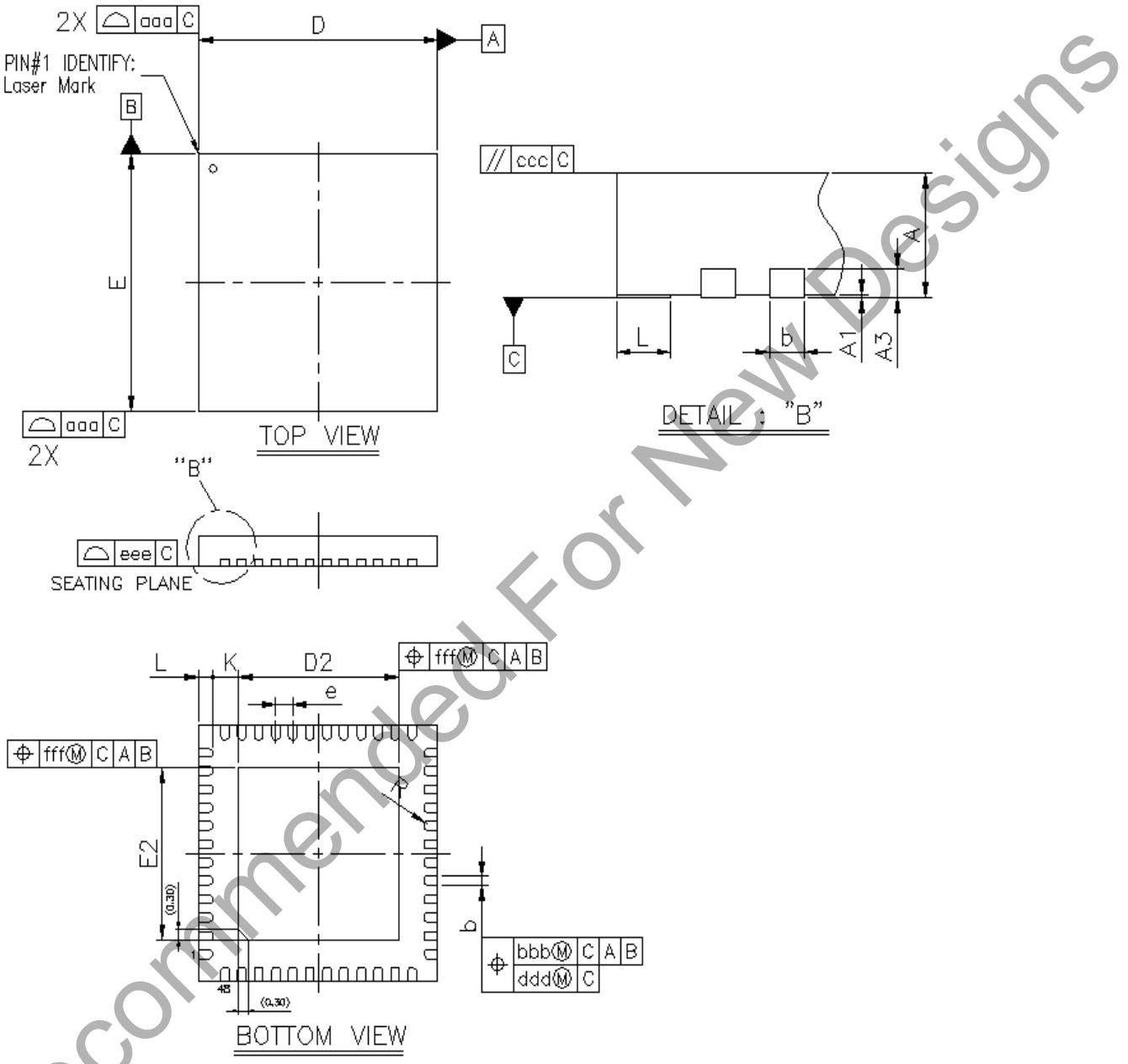


**Figure 7.1. QFN48 Package Drawing**

Not Recommended For New Designs

**Table 7.1. QFN48 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.18 | 0.25 | 0.30 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 4.60 | 4.70 | 4.80 |
| E2 | 4.60 | 4.70 | 4.80 |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.09 | — | 0.14 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Note:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended For New Designs

### 7.2 QFN48 PCB Land Pattern

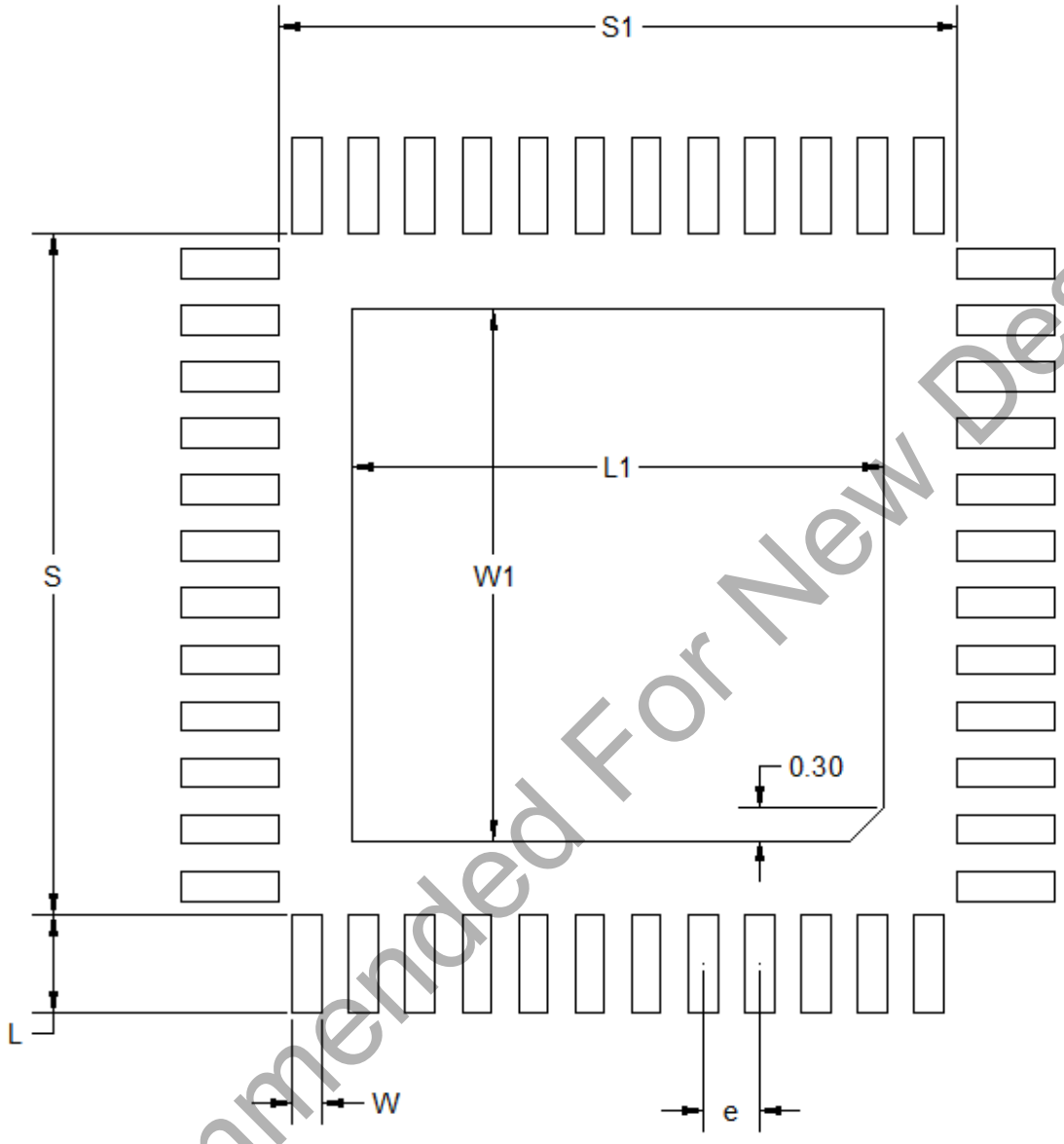


**Figure 7.2. QFN48 PCB Land Pattern Drawing**

Not Recommended For New Designs

**Table 7.2. QFN48 PCB Land Pattern Dimensions**

| Dimension | Typ |
|---|---|
| S1 | 6.01 |
| S | 6.01 |
| L1 | 4.70 |
| W1 | 4.70 |
| e | 0.50 |
| W | 0.26 |
| L | 0.86 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended For New Designs

### 7.3 QFN48 Package Marking

**Figure 7.3. QFN48 Package Marking**

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (1, 2,...)
  4. Device Configuration (1, 2,...)
  5. Performance Grade (P | B | V)
  6. Feature Code (1 to 7)
  7. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  8. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  9. Flash (J = 1024K | H = 512K | G = 256K | F = 128K | E = 64K | D = 32K)
  10. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

Not Recommended For New Designs

# 8. QFN32 Package Specifications

## 8.1 QFN32 Package Dimensions

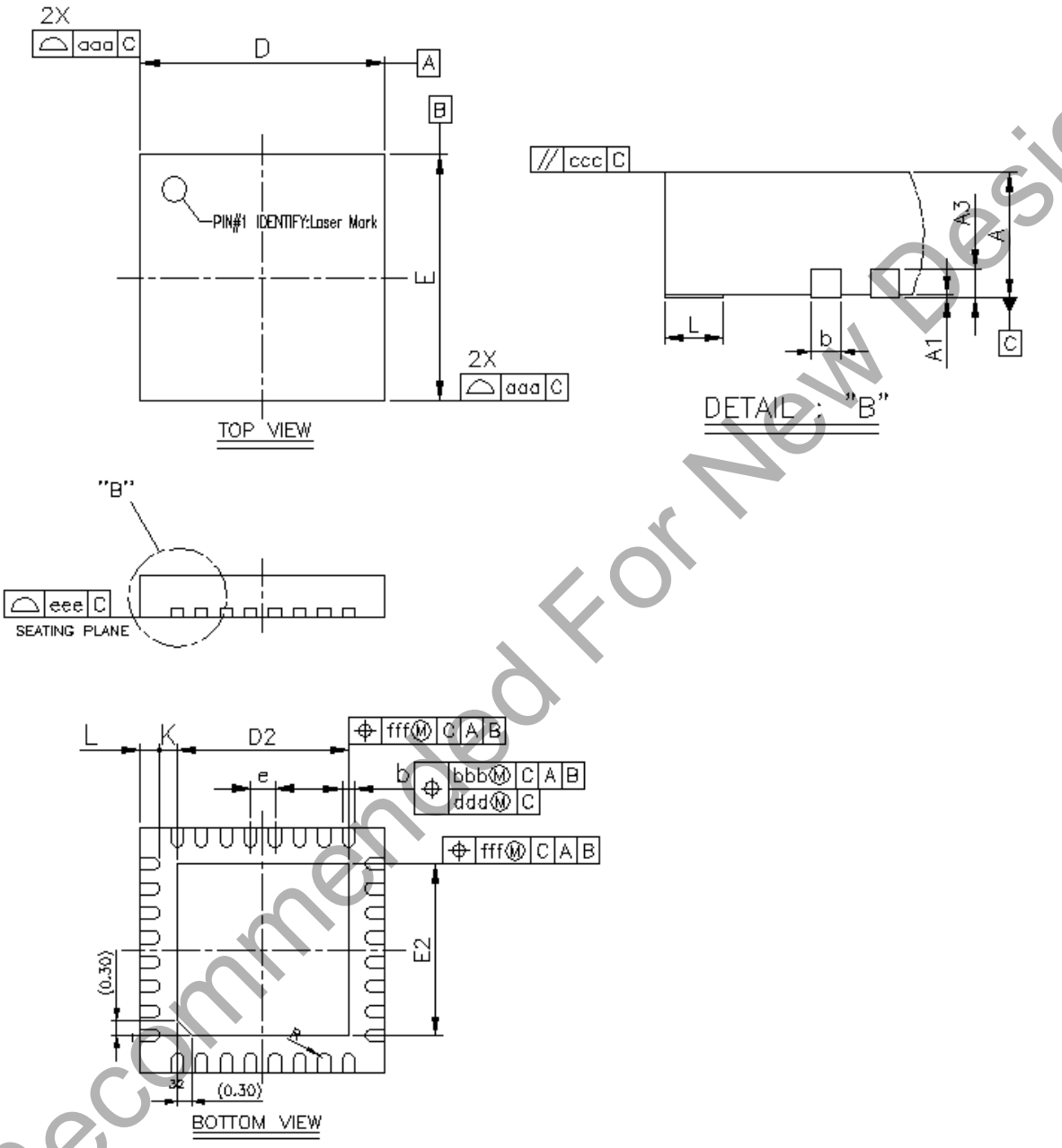


**Figure 8.1. QFN32 Package Drawing**

Not Recommended For New Designs

**Table 8.1. QFN32 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.18 | 0.25 | 0.30 |
| D/E | 4.90 | 5.00 | 5.10 |
| D2/E2 | 3.40 | 3.50 | 3.60 |
| E | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | — | — |
| R | 0.09 | — | 0.14 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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### 8.2 QFN32 PCB Land Pattern

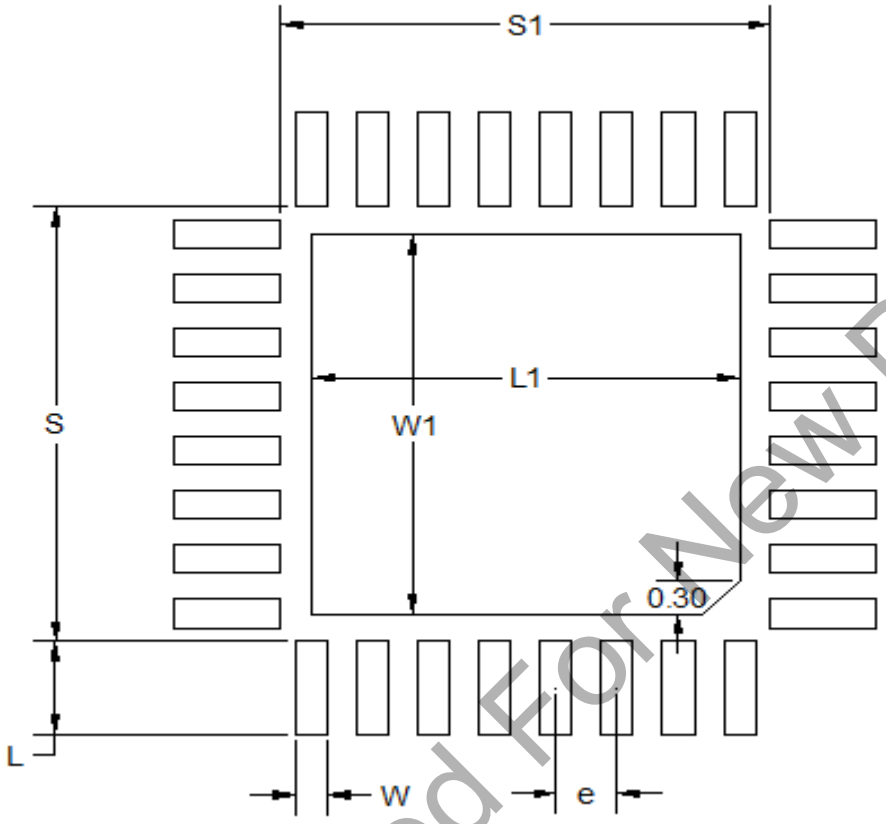


**Figure 8.2. QFN32 PCB Land Pattern Drawing**

Not Recommended For New Designs

**Table 8.2. QFN32 PCB Land Pattern Dimensions**

| Dimension | Typ |
|---|---|
| S1 | 4.01 |
| S | 4.01 |
| L1 | 3.50 |
| W1 | 3.50 |
| e | 0.50 |
| W | 0.26 |
| L | 0.86 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended For New Designs

### 8.3 QFN32 Package Marking

**Figure 8.3. QFN32 Package Marking**

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (1, 2,...)
  4. Device Configuration (1, 2,...)
  5. Performance Grade (P | B | V)
  6. Feature Code (1 to 7)
  7. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  8. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  9. Flash (J = 1024K | H = 512K | G = 256K | F = 128K | E = 64K | D = 32K)
  10. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

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# 9. Revision History

**Revision 1.2**

August, 2018

- Removed TRNG.
- “PAVDD” references in Sub-GHz specification tables clarified to refer to “External PA Supply”. The PAVDD pin is for the 2.4 GHz radio.
- GPIO Functionality table re-sorted to list pins alphabetically by GPIO Name column.
- Added EFR32MG14P731F256GM48-B part number and associated pinout information.

**Revision 1.1**

March, 2018

- Removed PLFRCO.
- Removed 2 Mbps sensitivity plot from Figure 4.11 2.4 GHz RF Receiver Sensitivity on page 109.
- Figure 6.5 APORT Connection Diagram on page 143: Corrected OPA output connections to route through "Y" buses.
- Removed "Confidential" watermark.

**Revision 1.0**

October, 2017

- **Front Page**: Fixed PLFRCO EM mode color.
- **Front Page and Feature List**: Updated highlighted features for consistency across product line.
- Multiprotocol support added to **Ordering Information** descriptions.
- **Ordering Code Key** Figure: Removed L (BGA) from package designation.
- **System Overview**: Memory maps updated with LE peripherals and new formatting.
- **Absolute Maximum Ratings** Table: Added footnote to clarify $V_{DIGPIN}$ specification for 5V tolerant GPIO.
- **General Operating Conditions** Table: Added footnote for additional information on peak current during voltage scaling operations.
- Updated all specification table values, conditions, and footnotes according to latest characterization data, spec standards, and production test limits.
- **Sub-GHz RF Receiver Characteristics for 868 MHz Band** Table: Removed BPSK DSSS signal specifications from table and footnotes.
- **2.4 GHz RF Transmitter Output Power** Figure: Extended temperature range to 125 C.
- **2.4 GHz RF Receiver Sensitivity** Figure: Updated with latest characterization data and added 125 C operational plots.
- Updated pinout table formatting.
- Removed 2 Mbps BLE RX and TX specification tables and associated information.

**Revision 0.1**

June 21, 2017

Initial release.

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