4MHz, High-Current Flash LED Driver

Check for Samples: LM3565

FEATURES

- **High Efficiency Synchronous Boost Converter**
- **Drives 2 LEDs in Series with up to 930 mA**
- **External Strobe Pin for Hardware Enabled Flash**
- **External Torch Pin for Hardware Enabled Torch**
- **Dedicated Transmit Interrupt Pin**
- **8-Bit ADC for LED Voltage and Input Voltage Monitoring**
- **Automatic Diode Current Scale Back**
- **PWM Control in Flash and Assist Modes**
- **Fault Detection and Reporting**
- **400 kHz I^2C-Compatible Interface**
- **16-Bump, 1.990 mm x 1.990 mm x 0.6 mm DSBGA Package (YZR0016AAA)**

APPLICATIONS

- **Camera Phone LED Flash**

DESCRIPTION

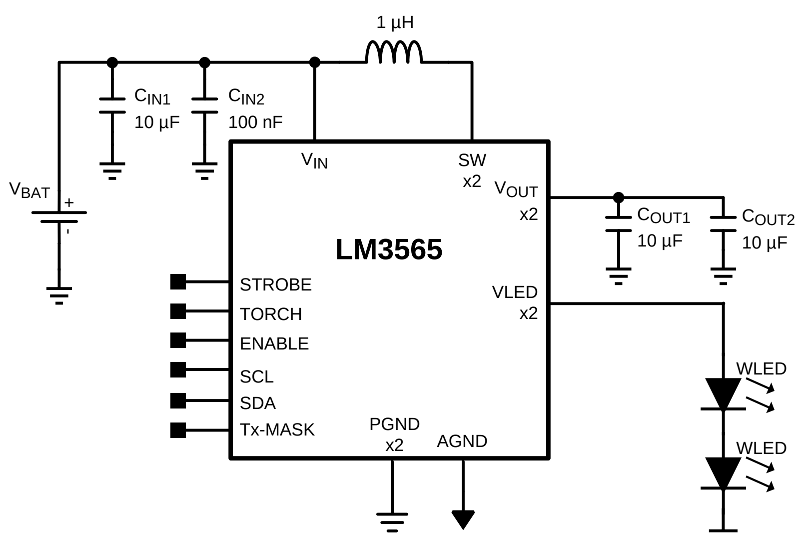
The LM3565 is a 4 MHz fixed-frequency, current mode synchronous boost converter designed to drive two series flash LEDs at 930 mA. A high-voltage current source allows the LEDs to be terminated to the GND plane eliminating the need for an additional return trace back to the IC.

A dedicated Strobe pin provides a direct interface to trigger the flash event, while an external Torch pin provides an additional method for enabling the LEDs in a constant current mode. The LM3565 can adaptively scale the maximum flash level delivered to the LEDs based upon the measured input voltage.

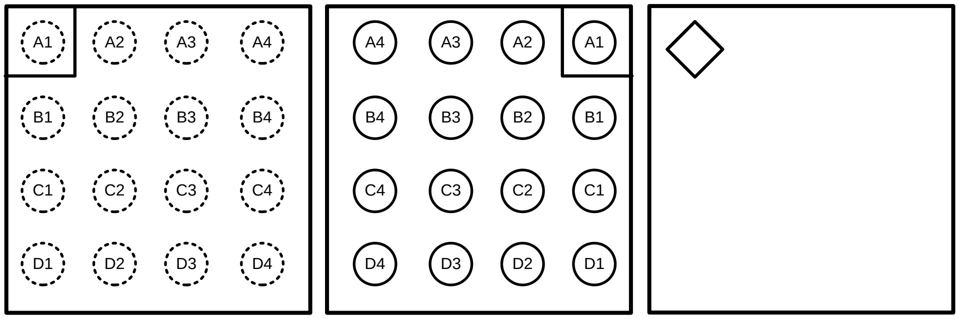
Multiple protection features are available on the LM3565 ranging from over-voltage protection to output short-circuit detection.

The LM3565 has four selectable inductor current limits to help the user select an inductor that is appropriate for the design.

TYPICAL APPLICATION CIRCUIT



CONNECTION DIAGRAM



TOP VIEW (BUMPS FACE DOWN) BOTTOM VIEW (BUMPS FACE UP) PIN A1 LOCATION

PIN FUNCTIONS

PIN		INPUT/OUTPUT (I/O)	DESCRIPTION
NO.	NAME		
A1	PGND		Power GND.
A2	PGND		Power GND.
A3	VIN	I	Input voltage pin of the device. Connect input bypass capacitor very close to this pin.
A4	ENABLE	I	Chip Enable. High = Standby, Low = Shutdown.
B1	SW1	I	Inductor connection.
B2	SW2	I	Inductor connection.
B3	TORCH	I	Hardware Torch Enable Pin.
B4	TX-MASK	I	Hardware Transmit Interrupt Pin.
C1	VOUT1	O	Boost output. Connect output bypass capacitor very close to this pin.
C2	VOUT2	O	Boost output. Tie to VOUT1.
C3	STROBE	I	Strobe signal input pin to synchronize flash pulse in I^2C-compatible mode. This signal usually comes from the camera processor.
C4	SDA	I/O	Serial Data Pin for I^2C-compatible Interface.
D1	LEDOUT1	I/O	LED Current Source Output.
D2	LEDOUT2	I/O	LED Current Source Output. Tie to LEDOUT1.
D3	AGND		A/D Ground Pin.
D4	SCL	I	Serial Clock Pin for I^2C-compatible Interface.

ABSOLUTE MAXIMUM RATINGS(1)(2)

If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

		VALUE		UNIT
		MIN	MAX	
	VIN	–0.3	+6	V
	TORCH, TX-MASK, STROBE, ENABLE, SDA, SCL	–0.3	(V_{IN} +0.3V) +6.0	V
	VOUT1, VOUT2, LEDOUT1, LEDOUT2, SW1, SW2		+10	V
	Continuous power dissipation(3)	Internally Limited		
T_{J-MAX}	Junction temperature		+150	°C
	Storage temperature range	–55	+150	°C
	Maximum lead temperature (soldering)(4)			
	ESD rating, Human Body Model		+2.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 115°C (typ). Thermal shutdown is specified by design.
(4) For detailed soldering specifications and information, refer to Texas Instruments Application Note: AN-1112: DSBGA Wafer Level Chip Scale Package for Recommended Soldering Profiles.

RECOMMENDED OPERATING CONDITIONS(1)(2)

		MIN	NOM	MAX	UNIT
	Input voltage range	+2.5		+5.5	V
	Output voltage range	+5.5		+8.5	V
T_J	Junction temperature range	–30		+125	°C
T_A	Ambient temperature range(3)	–30		+85	°C
THERMAL PROPERTIES					
θ_{JA}	Thermal resistance junction-to-ambient(4)			+62.2	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(4) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm x 76 mm x 1.6 mm with a 2x1 array of thermal vias. The ground plane on the board is 50 mm x 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/3 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1.2W.

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_A = +25°C. Limits in **boldface type** apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ 85°C). Unless otherwise specified: 2.7V ≤ V_{IN} ≤ 4.4V. [1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT AND VOLTAGE SPECIFICATIONS							
$I_{LED\text{-}OUT}$	LED Current accuracy	V_{OUT} =7.5V V_{LED} = 7.2V	60 mA ≤ IL_{ED} ≤ 930 mA	**(–5%)**		**(+5%)**	
V_{CSH}	Current source headroom voltage				300	**350**	mV
V_{OVP}	Over-voltage protection range	Trip Point (Rising)		**9.0**	9.5	**10.0**	V
I_{SD}	Shutdown current					**1**	µA
I_{SB}	Standby current					**1**	µA
I_Q	Operating quiescent current	Part switching			10		mA
UVLO	Under-voltage lock out	Falling V_{IN}		**2.3**	2.4	**2.5**	V
$UVLO_{HYST}$	UVLO Hysteresis	Rising VIN		**50**	100	**150**	mV
I_{LIM}	Peak current limit	CL Reg value = 00		**2.07**	2.3	**2.53**	A
		CL Reg value = 01		**2.34**	2.6	**2.86**	
		CL Reg value = 10		**2.61**	2.9	**3.19**	
		CL Reg value = 11		**2.97**	3.3	**3.63**	
R_{DSON_N}	NFET pin-to-pin Resistance				88		mΩ
R_{DSON_P}	PFET pin-to-pin Resistance				110		mΩ
OSCILLATOR AND TIMING SPECIFICATIONS (NON-I²C-COMPATIBLE INTERFACE TIMING)							
f_{SW}	Switching frequency			**3.8 (–5%)**	4.0	**4.2 (+5%)**	MHz
$t_{R\text{-}STEP}$	LED current ramp up and down				20		µsec
t_{RU}	Current ramp up time	From end of Command to I_{LED} = Fullscale			1.4		msec
$t_{TORCH\text{-}DG}$	Torch deglitching time			**6.3**	9	**11.7**	msec
ANALOG-TO-DIGITAL (A/D) CONVERTER SPECIFICATIONS							
ADCRES	A/D Resolution	Average step size			31.4	**50**	mV
VOFF	Offset error					**1**	Bits
GE	Gain error	V_{LED} = 8 V		**(–2%)**		**(+2%)**	
CONTROL INTERFACE VOLTAGE SPECIFICATIONS							
V_{IL}	Low-level threshold voltage (SCL SDA, ENABLE, TX-MASK, TORCH)					**0.54**	V
V_{IH}	High-level threshold voltage (SCL SDA, ENABLE, TX-MASK, TORCH, STROBE 1.8V)			**1.26**			V
V_{OL}	Low-level output threshold limit (SDA)	I_{LOAD} = 3 mA				**0.4**	V
V_{IL}	Low-level threshold voltage (STROBE 1.2V)					**0.36**	V
V_{IH}	High-level threshold voltage (STROBE 1.2V)			**0.84**			V

(1) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are **not** verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typical specifications are: V_{IN} = 3.6V and T_A = 25°C.
(2) Switching disabled.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_A = +25°C. Limits in **boldface type** apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ 85°C). Unless otherwise specified: 2.7V ≤ V_{IN} ≤ 4.4V. (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INTERFACE TIMING SPECIFICATIONS						
$T_{I2C-Start}$	I^2C-Compatible Logic startup time	I^2C/EN going high		250	**500**	µsec
f_{SCL}	SCL clock frequency				**400**	kHz
t_{LOW}	Low period of SCL clock		**1.3**			µsec
t_{HIGH}	High period of SCL clock		**0.6**			µsec
t_{HD-STA}	Hold time (repeated) START condition		**0.6**			µsec
t_{SU-STA}	Setup time for a repeated START condition		**0.6**			µsec
t_{HD-DAT}	Data hold time		**0**			µsec
t_{SU-DAT}	Data setup time		**100**			nsec
t_R	Rise time for SCL and SDA				**300**	nsec
t_F	Fall time for SCL and SDA				**300**	nsec
t_{SU-STO}	Setup time for stop condition		**0.6**			µsec
t_{BUF}	Bus free time between stop and start condition		**1.3**			µsec
t_{VD-DAT}	Data valid time				**0.9**	µsec
t_{VD-ACK}	Data valid acknowledge time				**0.9**	µsec
C_B	Capacitive load for each bus line		**20+0.1x C_B**		**400**	pF

TYPICAL CHARACTERISTICS

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

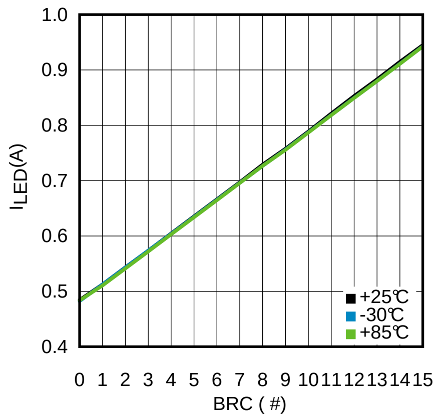


Figure 1. Flash Current vs Brightness Code

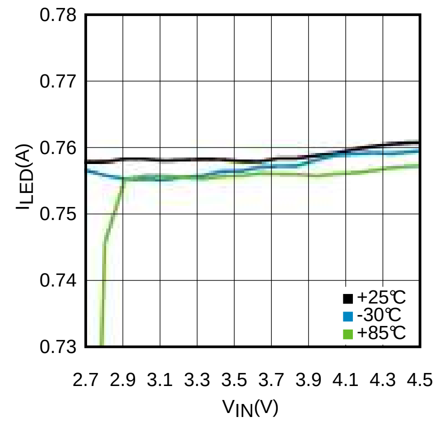


Figure 2. 750mA Flash LED Current vs Input Voltage

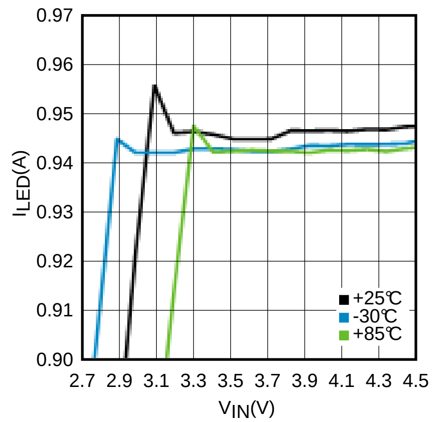


Figure 3. 930mA Flash LED Current vs Input Voltage

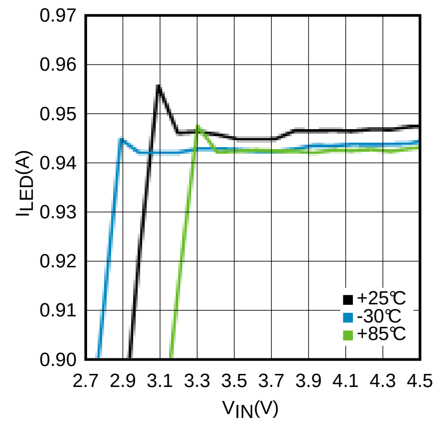


Figure 4. LED Efficiency vs Input Voltage at 750mA

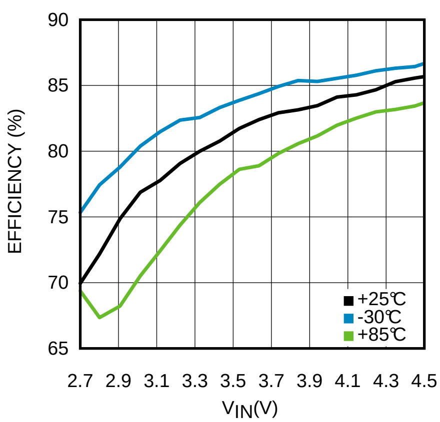


Figure 5. LED Efficiency vs Input Voltage at 930mA

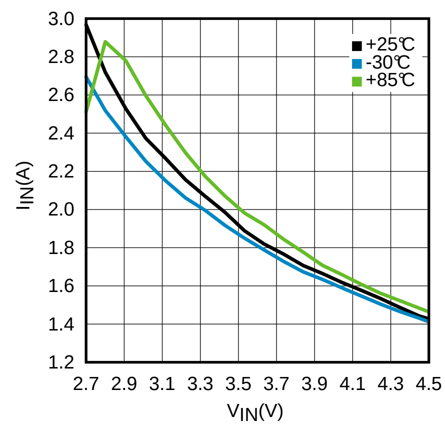


Figure 6. Input Current vs Input Voltage at 750mA

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

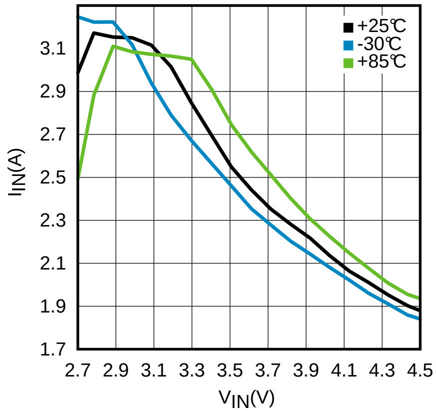


Figure 7. Input Current vs Input Voltage at 930mA

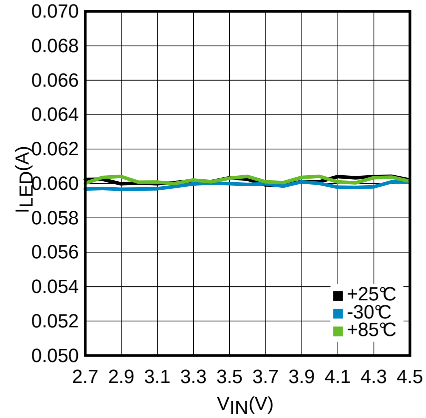


Figure 8. 60mA Torch LED Current vs Input Voltage

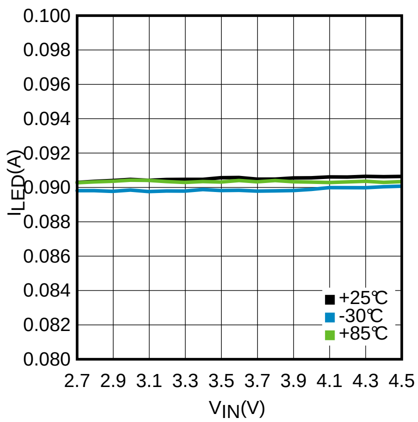


Figure 9. 90mA Torch LED Current vs Input Voltage

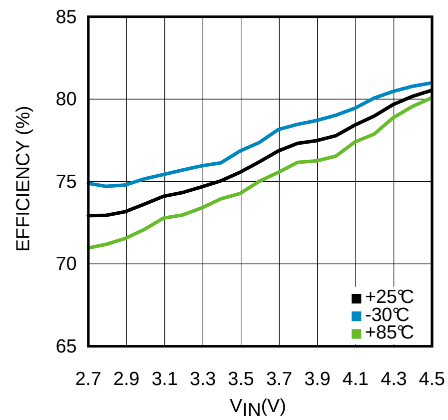


Figure 10. LED Efficiency vs Input Voltage at 60mA

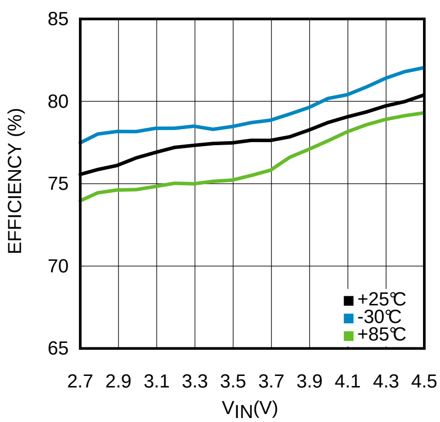


Figure 11. LED Efficiency vs Input Voltage at 90mA

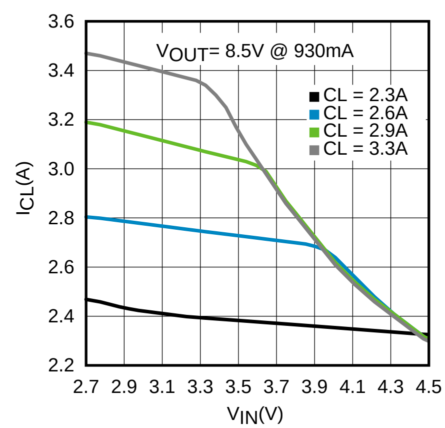


Figure 12. Inductor Current Limit vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

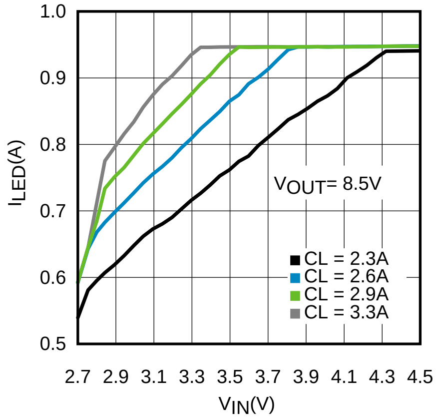


Figure 13. LED Current vs Input Voltage in Current Limit

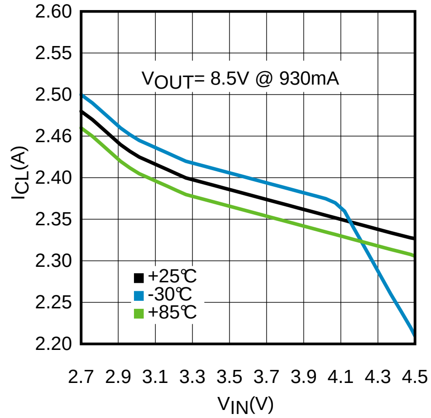


Figure 14. Inductor Current vs Input Voltage, CL = 2.3A

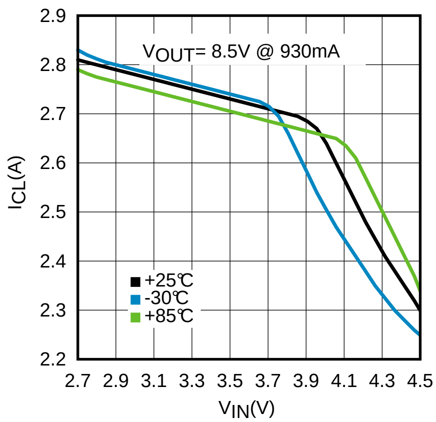


Figure 15. Inductor Current vs Input Voltage, CL = 2.6A

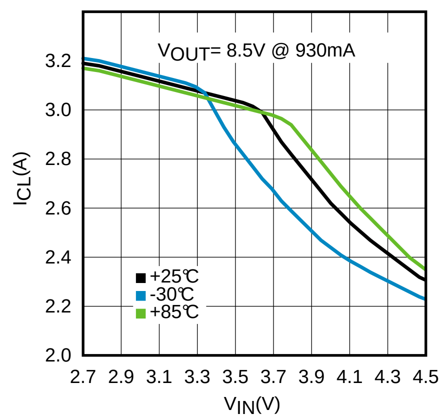


Figure 16. Inductor Current vs Input Voltage, CL = 2.9A

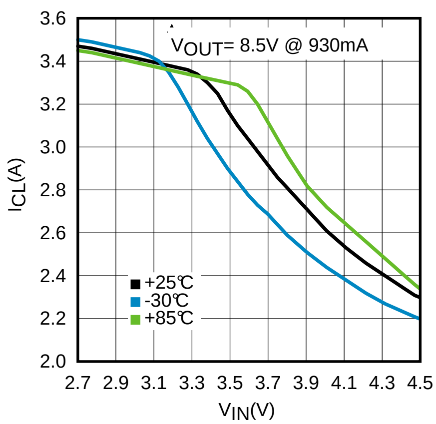


Figure 17. Inductor Current vs Input Voltage, CL = 3.3A

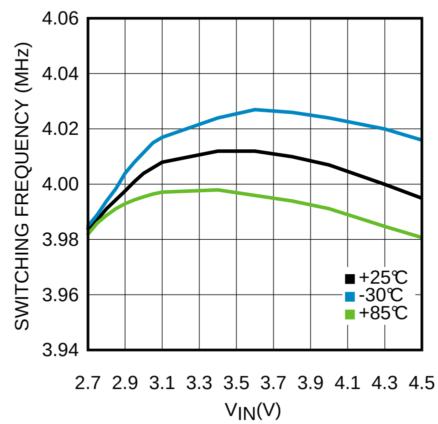


Figure 18. Frequency vs Input Voltage

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

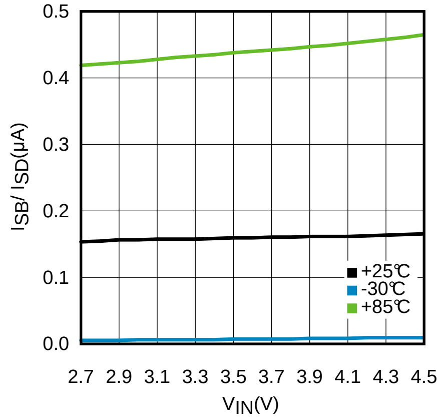


Figure 19. Standby/Shutdown Current vs Input Voltage

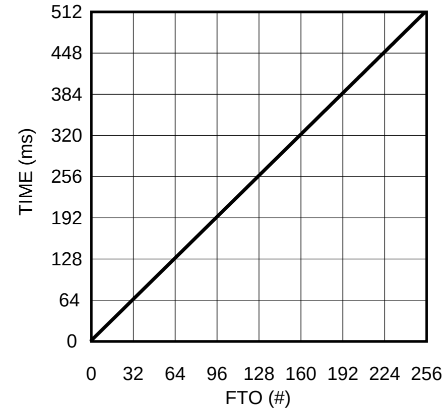


Figure 20. Flash Timeout vs Flash Timeout Code

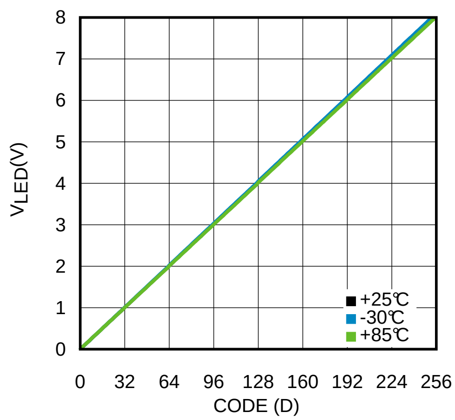


Figure 21. ADC Linearity

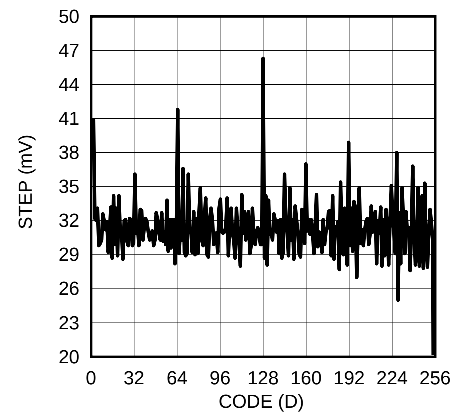


Figure 22. ADC Step Size

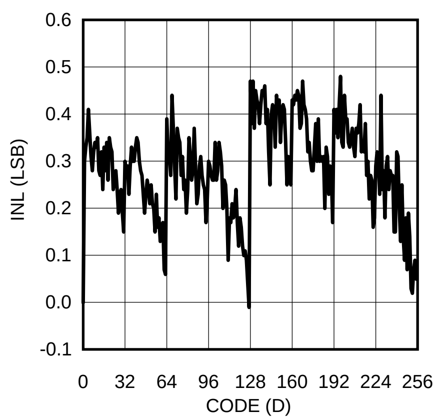


Figure 23. ADC INL

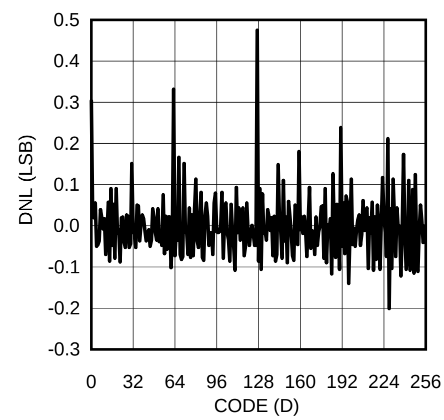


Figure 24. ADC DNL

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

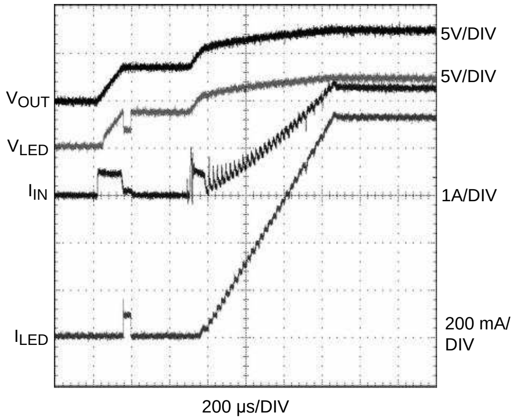


Figure 25. Flash Startup

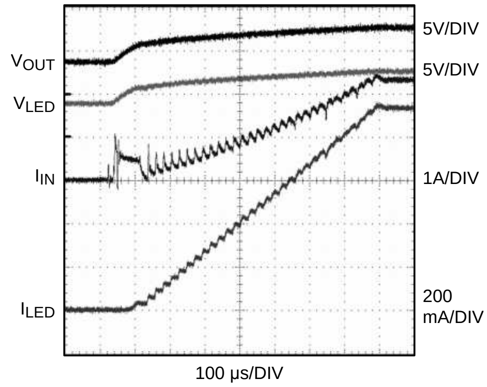


Figure 26. Flash Ramp-Up

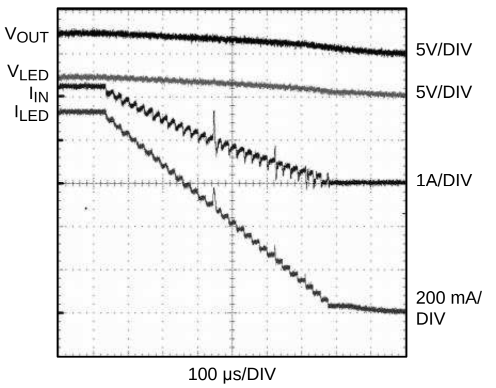


Figure 27. Flash Ramp-Down

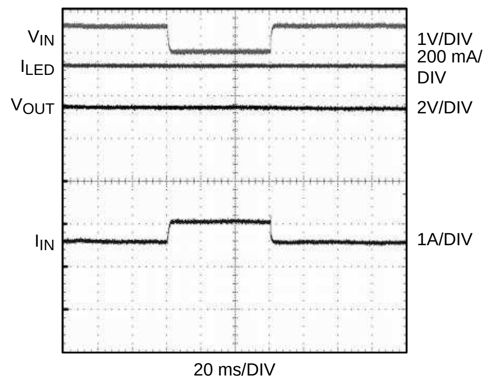


Figure 28. Line-Step During Flash

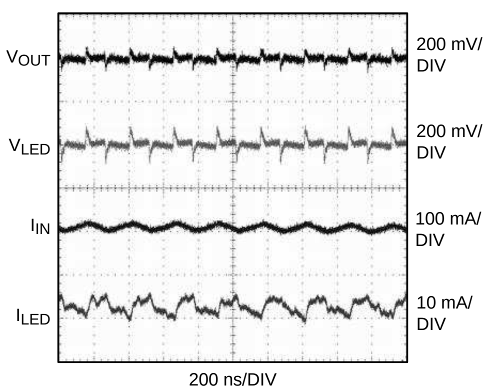


Figure 29. LED Current Ripple at 750mA

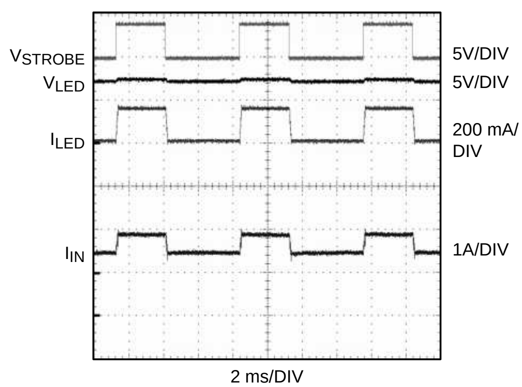


Figure 30. Flash PWM

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

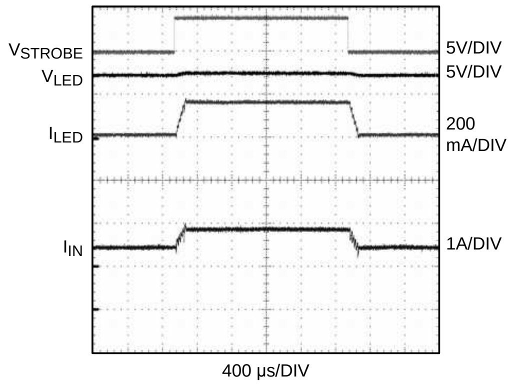


Figure 31. Flash PWM Ramp-Up & Ramp-Down

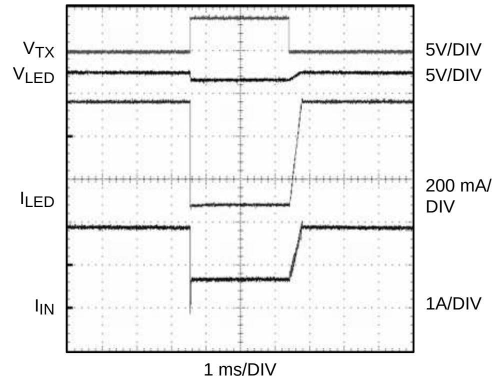


Figure 32. Tx-Mask Event

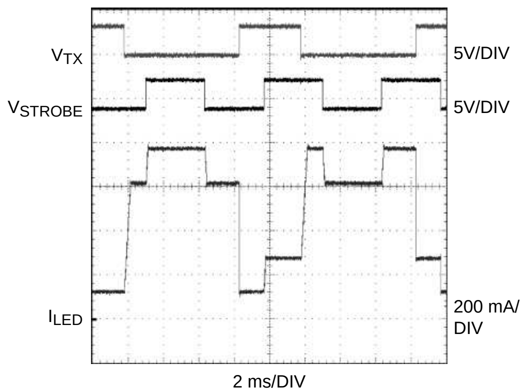


Figure 33. PWM and Tx-Mask Event

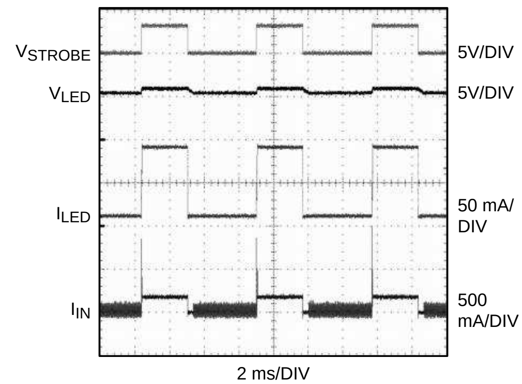


Figure 34. Assist PWM

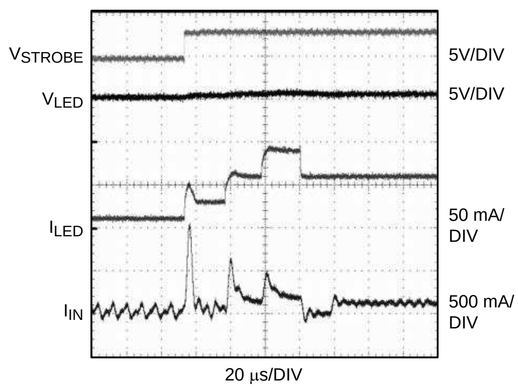


Figure 35. 60mA Assist PWM Ramp-Up

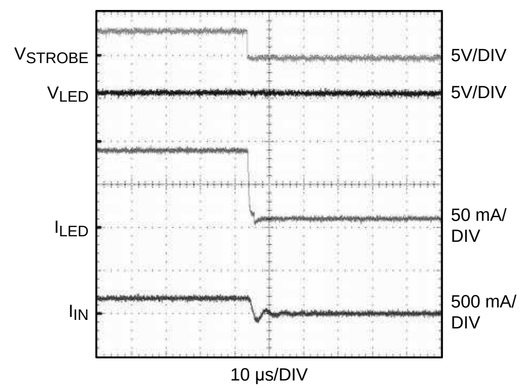


Figure 36. Assist PWM Down

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

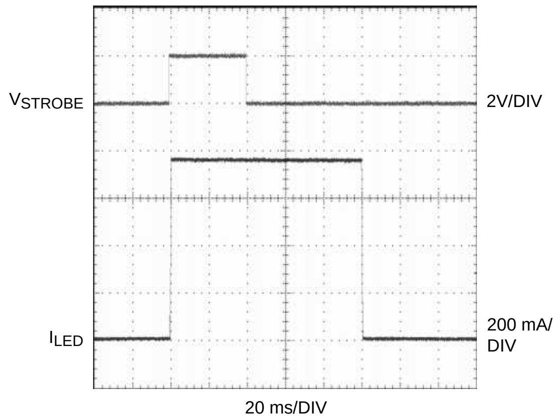


Figure 37. Edge-Sensitive Strobe

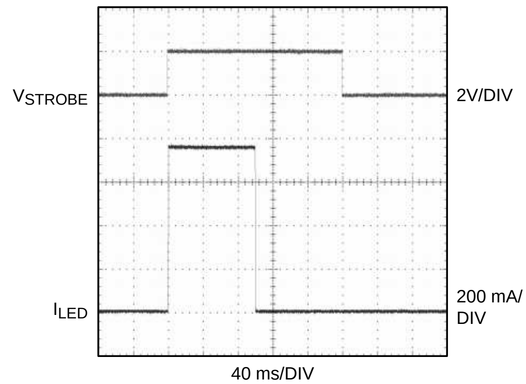


Figure 38. Level-Sensitive Strobe with Timeout

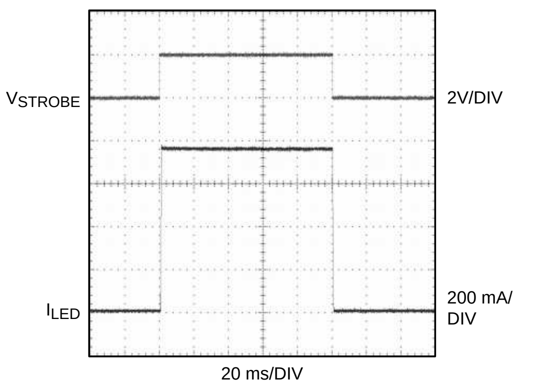


Figure 39. Level-Sensitive Strobe without Timeout

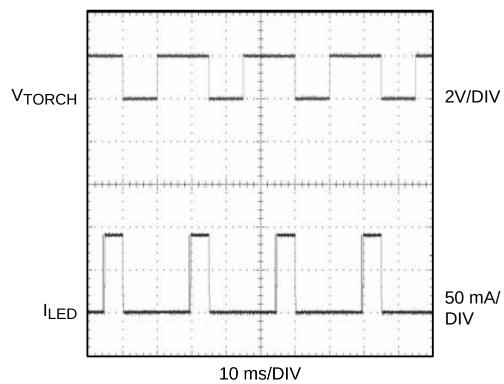


Figure 40. Torch Deglitching Time

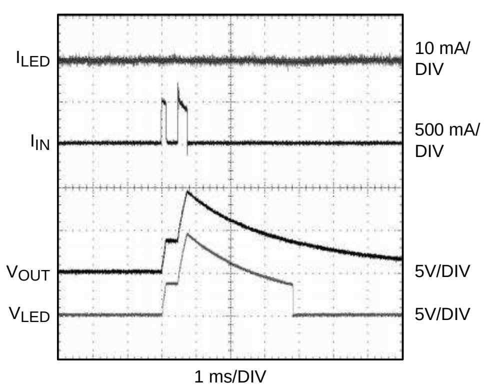


Figure 41. Over-Voltage Protection Fault (OVP)

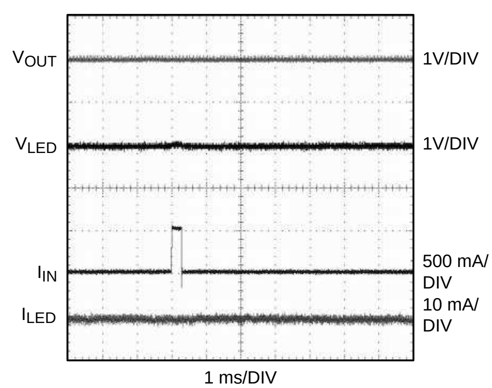


Figure 42. VOUT Short to GND Fault

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; C_{IN1}= 10 µF, C_{IN2}= 0.1 µF, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, L = 1 µH.

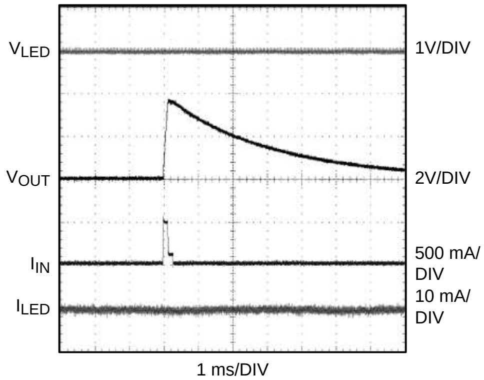


Figure 43. VLED Short to GND Fault

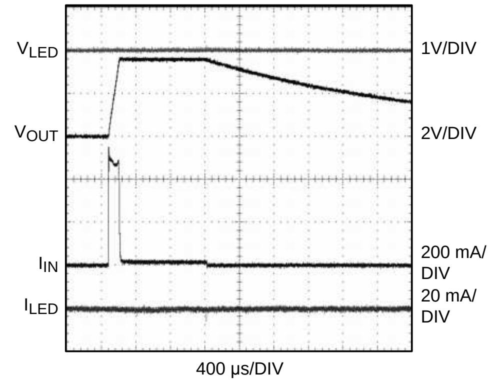


Figure 44. Indicator Short to GND Fault

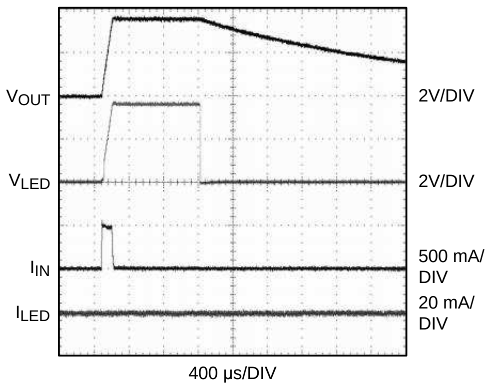


Figure 45. Indicator Open Fault

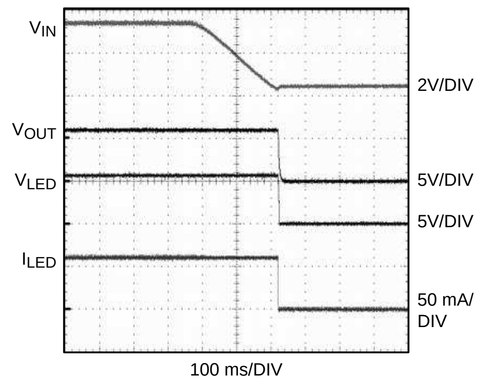
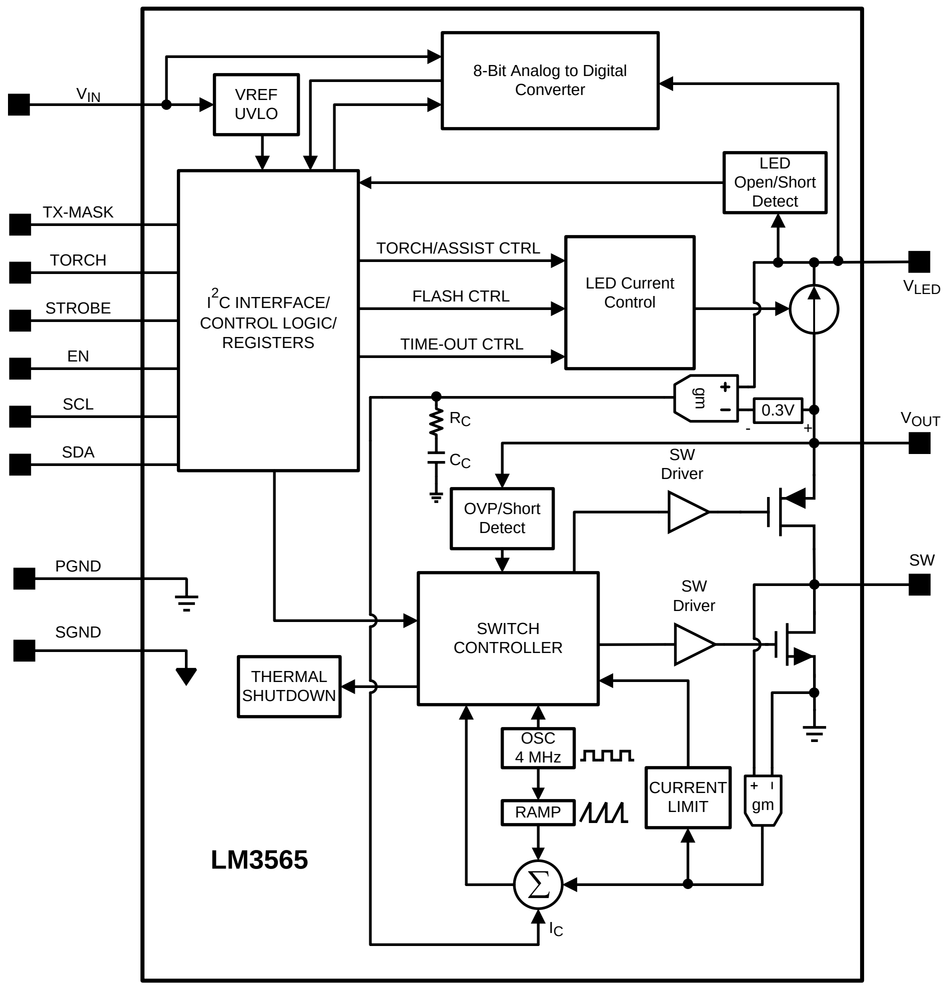


Figure 46. Under-Voltage Lockout (UVLO)

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Circuit Description

Overview

The LM3565 is a high-power white LED flash driver capable of delivering up to 930 mA of LED current into two series LEDs. The device incorporates a 4 MHz constant frequency, synchronous, current mode PWM boost converter, and a single high-side current source to regulate the LED current over the 2.5V to 5.5V input voltage range.

Circuit Components

Synchronous Boost Converter

The LM3565 operates in boost mode in LED Flash or Assist operation. In LED boost mode, the PWM converter switches and maintains at least 300 mV across the current source. This minimum headroom voltage ensures that the current sink remains in regulation.

High-Side Current Source

The High-Side current source of the LM3565 is capable of driving two LEDs in series. The flash current range is 480 mA to 930 mA in 30 mA steps with a default current equal to 750 mA.

Additionally, the high-side current source is capable of supporting two Assist/Torch current levels (continuous current) equal to 60 mA (default) or 90 mA.

A/D Converter

An internal 8-bit ADC can be utilized to measure the input voltage and the LED voltage during a flash or assist event. If the ADC input voltage measurement bit is set to a '1' (IV bit in register 0x09), the digitized value of the LM3565's input voltage can be read back from the Input Voltage ADC Register (0x0A). The input voltage is sampled before the start of the flash or assist event if the FON bit in register 0x09 is set to a '0' and 2ms after the LED current ramp up is completed if it is set to a '1'. The LED voltage can be read back from the LED Voltage ADC Register (0x0B) if the ADC LED voltage measurement bit is set to a '1' (LV bit in register 0x09). The LED voltage is sampled 2ms after the LED current is ramped up.

ENABLE Pin

The ENABLE pin on the LM3565 places the part into Shutdown Mode (low) or Standby Mode (high). In Shutdown Mode, most of the control functionality is disabled. In shutdown, it is possible to enable the part through the use of the Torch pin. In standby, the LM3565 can be controlled via the I^2C-compatible interface or the Torch and Strobe pins if the part has been configured to do so. The ENABLE pin must be held low before power is applied to the LM3565.

SDA and SCL Pins

The SDA and SCL pins are the I^2C-compatible control interface inputs for the LM3565. SDA is the interface data input and SCL is the interface clock input.

STROBE Pin

The Strobe pin of the LM3565 provides an external method for initiating a flash or assist event. In most cases, the Strobe pin is connected to an imaging module so that the image capture and flash event are synchronized. The Strobe pin is only functional when the LM3565's Output Enable (OEN in 0x07) and Strobe Signal Mode (SEN in 0x06) bits are set ('1'). The Strobe pin can be configured to be an edge-sensitive or level-sensitive input by setting the Strobe Signal Usage bit (SSU in 0x06. '1' = Level, '0' = Edge). In edge-sensitive mode, a rising edge transition ('0' to '1') will start the flash event and the internal flash timer will terminate the event. In level-sensitive mode, a rising edge transition ('0' to '1') will start the flash event and a falling edge transition ('1' to '0') or the internal flash timer, which ever occurs first, will terminate the event.

Additionally, the Strobe pin can be used to pulse-width modulate (PWM) the diode current during a flash or assist event. In flash mode, by setting the PWM bit in the Strobe signaling register (PWM in register 0x06) to a '1', and toggling the Strobe pin high and low, the diode current will transition between the target flash current and a reduced current value selected in register 0x06 (SPL3-SPL0). When the Strobe pin is high ('1'), the flash current is equal to the target LED current. When the Strobe pin is low ('0'), the flash current is equal to the target LED current minus the reduction current value, or 60 mA, whichever is higher. The diode current is ramped up and down during the transitions between the full current state and the reduced current state.

In assist mode, by setting the PWM bit in the Strobe signaling register (PWM in register 0x06) to a '1', and toggling the Strobe pin high and low, the diode current will transition between the target assist current and 10 mA. When the Strobe pin is high ('1'), the assist current is equal to the target LED current. When the Strobe pin is low ('0'), the assist current is equal to 10 mA. The diode current is always ramped up to 90 mA, then reduced to 60 mA if the assist target current is set to 60 mA. The transition between the full-assist current and the 10 mA current level is done in one step.

TORCH Pin

The Torch pin of the LM3565, depending on the state and configuration, allows the user to enable Torch/Assist Mode without having to write the command through the I^2C bus. In standby mode, the external torch mode bit (ETEN bit in register 0x03) must be set to a '1' to allow an external torch (default value = '1'). The torch mode current is equal to the Assist mode current level stored in register 0x02 (AS0 bit, default value = '0' or 60 mA). In shutdown mode, driving the Torch pin high will enable the LM3565 and drive the flash LEDs at 60 mA.

TX-MASK Pin

The TX-Mask pin provides the RF PA a direct method to reduce the flash current by a predetermined value stored in the TX-Mask register (0x03), to prevent a battery over-current fault. When the TX-Mask pin is set low, the normal target current is realized. When the TX-Mask pin is set high, the flash current is reduced. The flash current is not ramped during the transition from full-scale to the reduced level; the flash current is ramped when transitioning back to the full-scale value from the reduced value. As in the Fflash PWM Mode, the lowest flash current is set to 60 mA.

Fault Protections

The LM3565 has numerous internal fault protection mechanisms to help prevent damage to the LM3565 as well as the system in the event of a fault. Most fault conditions will cause the LM3565 to enter Shutdown Mode and will report a fault to the fault register (0x08) or (0x09). The faults that can be detected are as follows:

- Over-Voltage Protection (VOUT)
- Short-Circuit Protection (VOUT and VLED)
- Over-Temperature Protection
- Flash Time-Out
- TX-Mask Event
- Under-Voltage Lock-Out
- Input Low Voltage Detect
- Inductor Current Limit (not reported)
- Output Capacitor Open Protection

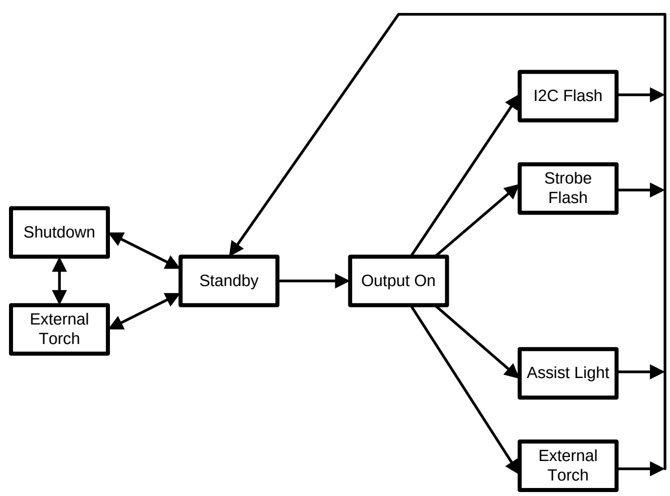


Figure 47. Mode Diagram

I²C-Compatible Interface

Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

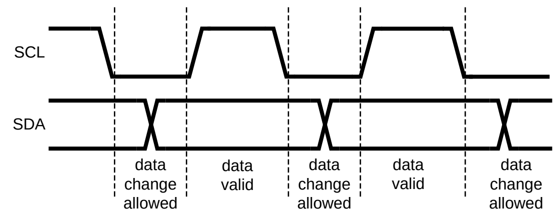


Figure 48. Data Validity Diagram

A pull-up resistor between VIO and SDA must be greater than [(**VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C-compatible session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C-compatible master always generates START and STOP conditions. The I²C-compatible bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C-compatible master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

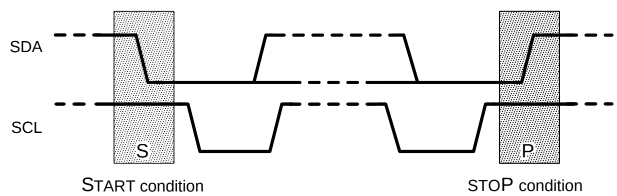
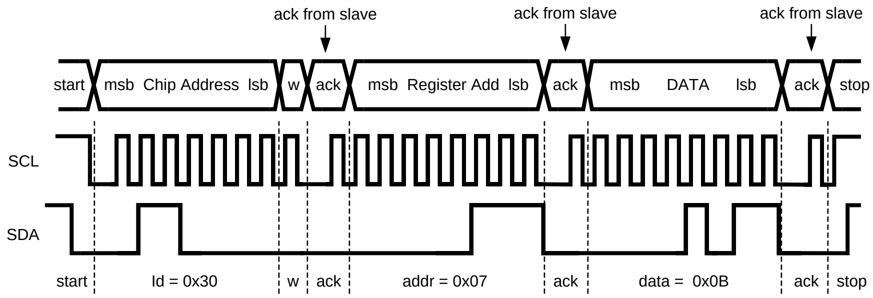


Figure 49. Start and Stop Conditions

Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3565 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3565 generates an acknowledge after each byte has been received.

After the START condition, the I²C-compatible master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3565 address is 30h. For the eighth bit, a '0' indicates a WRITE and a '1' indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

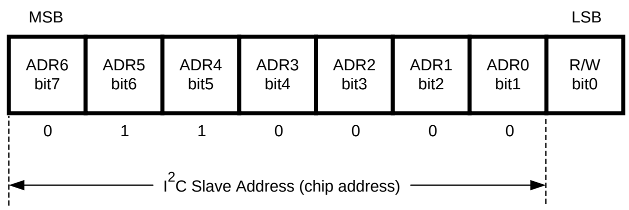


NOTE: w = write (SDA = "0"), ack = acknowledge (SDA pulled down by the slave), id = chip address, 30h for LM3565

Figure 50. Write Cycle

I²C-Compatible Chip Address

The chip address for LM3565 is 0110000, or 30hex.



Internal Registers of LM3565

Table 1. Summary of LM3565 Registers

REGISTER	INTERNAL HEX ADDRESS	POWER ON VALUE
Design Information Register	0x00	0011 0100
Version Control Register	0x01	0000 0110
Current Set Register	0x02	0000 1001
TX-Mask Register	0x03	0111 1011
Low Voltage Control Register	0x04	0100 0100
Timing Control Register	0x05	0010 0011
Strobe Signaling Register	0x06	1100 1000
Output Mode Register	0x07	0000 0000
Fault and Info Register	0x08	0000 0000
ADC Control Register	0x09	0000 0000
Input Voltage ADC Register	0x0A	0000 0000
LED Voltage ADC Register	0x0B	0000 0000

Register Definitions (bold table values = default register settings)

Design Information Register
Address: 0x00

Definition:	MN3	MN2	MN1	MN0	MO3	MO2	MO1	MO0
Default:	0	0	1	1	0	1	0	0

MN3–MN0: Manufacturer ID = 0011
MO3–MO0: Model ID = 0100

Version Control Register
Address: 0x01

Definition:	RF3	RF2	RF1	RF0	DR3	DR2	DR1	DR0
Default:	0	0	0	0	0	1	1	0

RF3–RF0: Unused
DR3–DR0: Design Revision = 0110

Current Set Register
Address: 0x02

Definition:	NA	NA	NA	AS0	FS3	FS2	FS1	FS0
Default:	0	0	0	0	1	0	0	1

AS0: Assist Current Level Bit. '0' = 60 mA, '1' = 90 mA
FS3-FS0: Flash Set Current bits. Refer to Table 2 for details.

Table 2. Flash Currents

FS3	FS2	FS1	FS0	Flash Current Level
0	0	0	0	480 mA
0	0	0		510 mA
0	0	1	0	540 mA
0	0	1	1	570 mA
0	1	0	0	600 mA
0	1	0	1	630 mA
0	1	1	0	660 mA
0	1	1	1	690 mA
1	0	0	0	720 mA
1	0	0	1	**750 mA**
1	0	1	0	780 mA
1	0	1	1	810 mA
1	1	0	0	840 mA
1	1	0	1	870 mA
1	1	1	0	900 mA
1	1	1	1	930 mA

Tx-Mask Register
Address: 0x03

Definition:	TXEN	TXR3	TXR2	TXR1	TXR0	ICL1	ICL0	ETEN
Default:	0	1	1	1	1	0	1	1

TXEN: TX-Mask Enable Bit. '0' = TX-Mask Disabled. '1' = TX-Mask Enabled.
TXR3-TXR0: TX-Mask Current Reduction Bits. See TX-Mask Flash Current Reduction Levels table.
ICL1-ICL0: Inductor Peak Current Limit Bits. See Peak Inductor Current Limit Levels table.
ETEN: External Torch Enable Bit. '0' = External Torch Mode disabled in standby.
'1' = External Torch Mode allowed/enabled in standby.

Table 3. TX-Mask Flash Current Reduction Levels

TXR3	TXR2	TXR1	TXR0	Flash Reduction Level
0	0	0	0	30 mA
0	0	0	1	60 mA
0	0	1	0	90 mA
0	0	1	1	120 mA
0	1	0	0	150 mA
0	1	0	1	180 mA
0	1	1	0	210 mA
0	1	1	1	240 mA
1	0	0	0	270 mA
1	0	0	1	300 mA
1	0	1	0	330 mA
1	0	1	1	360 mA
1	1	0	0	390 mA
1	1	0	1	420 mA
1	1	1	0	450 mA
1	1	1	1	**480 mA**

Table 4. Peak Inductor Current Limit Levels

ICL1	ICL0	Peak Inductor Current Limit
0	0	2.3A
0	1	**2.6A**
1	0	2.9A
1	1	3.3A

Low Voltage Control Register
Address: 0x04

Definition:	NA	LVEN	LVL2	LVL1	LVL0	LVR1	LVR0	LVRS
Default:	0	1	0	0	0	1	0	0

LVEN: Flash Low Voltage Checking Enable Bit. '0' = Disabled, '1' = Enabled
LVL2-LVL0: Flash Low Voltage Detection Level. See Table 5.
LVR1-LVR0: Flash Low Voltage Current Reduction Level.
See Table 5.
LVRS: State Machine Reset Bit. '0' = Normal operation, '1' = RESET

Table 5. Flash Low Voltage Detection Levels

LVL2	LVL1	LVL0	Input Voltage Level
0	**0**	**0**	**3.0V**
0	0	1	3.1V
0	1	0	3.2V
0	1	1	3.3V
1	0	0	3.4V
1	0	1	3.5V
1	1	0	3.6V
1	1	1	3.7V

Table 6. Flash Low Voltage Current Reduction Values

ICL1	ICL0	Peak Inductor Current Limit
0	0	150 mA
0	1	180 mA
1	**0**	**210 mA**
1	1	240 mA

Timing Control Register
Address: 0x05

Definition:	FT7	FT6	FT5	FT4	FT3	FT2	FT1	FT0
Default:	0	0	1	0	0	0	1	1

FT7-FT0: Flash Timeout Duration Bits.
Flash Time = (2 + N x 2)ms, where $0 \leq N \leq 255$
'0x00' = 2ms, '0x01' = 4ms, '0x02' = 6ms, . . ., '0x22' = 126ms, . . ., '0xFF' = 512 ms.

Strobe Signaling Register
Address: 0x06

Definition:	SEN	SSU	PWM	SPL3	SPL2	SPL1	SPL0	SLL
Default:	1	1	0	0	1	0	0	0

SEN: = Strobe Enable Bit. '0' = Disabled, '1' = Enabled
SSU: Strobe Signal Usage Bit. '0' = edge-sensitive, '1' = Level Sensitive
PWM: Flash PWM w/ Strobe Signal Enable bit. '0' =Disabled, '1' = Enabled
SPL3-SPL0: Stobe PWM Flash Current Reduction Level.
See Strobe PWM Flash Current Reduction Levels table.
SLL: Strobe Logic Level Bit. '0' = 1.2V Logic, '1' = 1.8V Logic

Table 7. Strobe PWM Flash Current Reduction Levels

SPL3	SPL2	SPL1	SPL0	Flash Current Level
0	0	0	0	30 mA
0	0	0	1	60 mA
0	0	1	0	90 mA
0	0	1	1	120 mA
0	1	0	0	**150 mA**
0	1	0	1	180 mA
0	1	1	0	210 mA
0	1	1	1	240 mA
1	0	0	0	270 mA
1	0	0	1	300 mA
1	0	1	0	330 mA
1	0	1	1	360 mA
1	1	0	0	390 mA
1	1	0	1	420 mA
1	1	1	0	450 mA
1	1	1	1	480 mA

Output Mode Register
Address: 0x07

Definition:	x	x	x	x	OEN	x	OM1	OM0
Default:	0	0	0	0	0	0	0	0

OEN: Output Enable Bit. '0' = Disabled, '1' = Enabled
OM1-OM0: Output Mode Bits. See Output Modes table.

Table 8. Output Modes

OM1	OM0	Output Mode
0	0	External Torch
0	1	Do Not Use
1	0	Assist Light
1	1	Flash

Fault and Info Register
Address: 0x08

Definition:	OVP	SC	OTP	TO	TXM	RFU	ILV	UVLO
Default:	0	0	0	0	0	0	0	0

OVP: Over-Voltage Protection Fault Flag
SC: Short Circuit Fault Flag
OTP: Over Temperature Protection Flag
TO: Flash Timeout Flag TXM: TX-Mask Event Flag
ILV: Input Low Voltage Fault Flag
UVLO: Under Voltage Lock Out Fault Flag

ADC Control
Address: 0x09

Definition:	IV	LV	FON	CO	RFU	RFU	RFU	RFU
Default:	0	0	0	0	0	0	0	0

IV: ADC Input Voltage Measurement Enable Bit. '0' = Disabled, '1' = Enabled
LV: ADC LED Voltage Measurement Enable Bit. '0' = Disabled, '1' = Enabled
FON: Input Voltage Measurement during Flash Bit. '0' = Without Flash Current, '1' = With Flash Current
CO: Open Output Capacitor Fault Bit. '0' = Normal Operation, '1' = Missing Output Capacitor

Input Voltage ADC Register
Address: 0x0A

Definition:	IVD7	IVD6	IVD5	IVD4	IVD3	IVD2	IVD1	IVD0
Default:	0	0	0	0	0	0	0	0

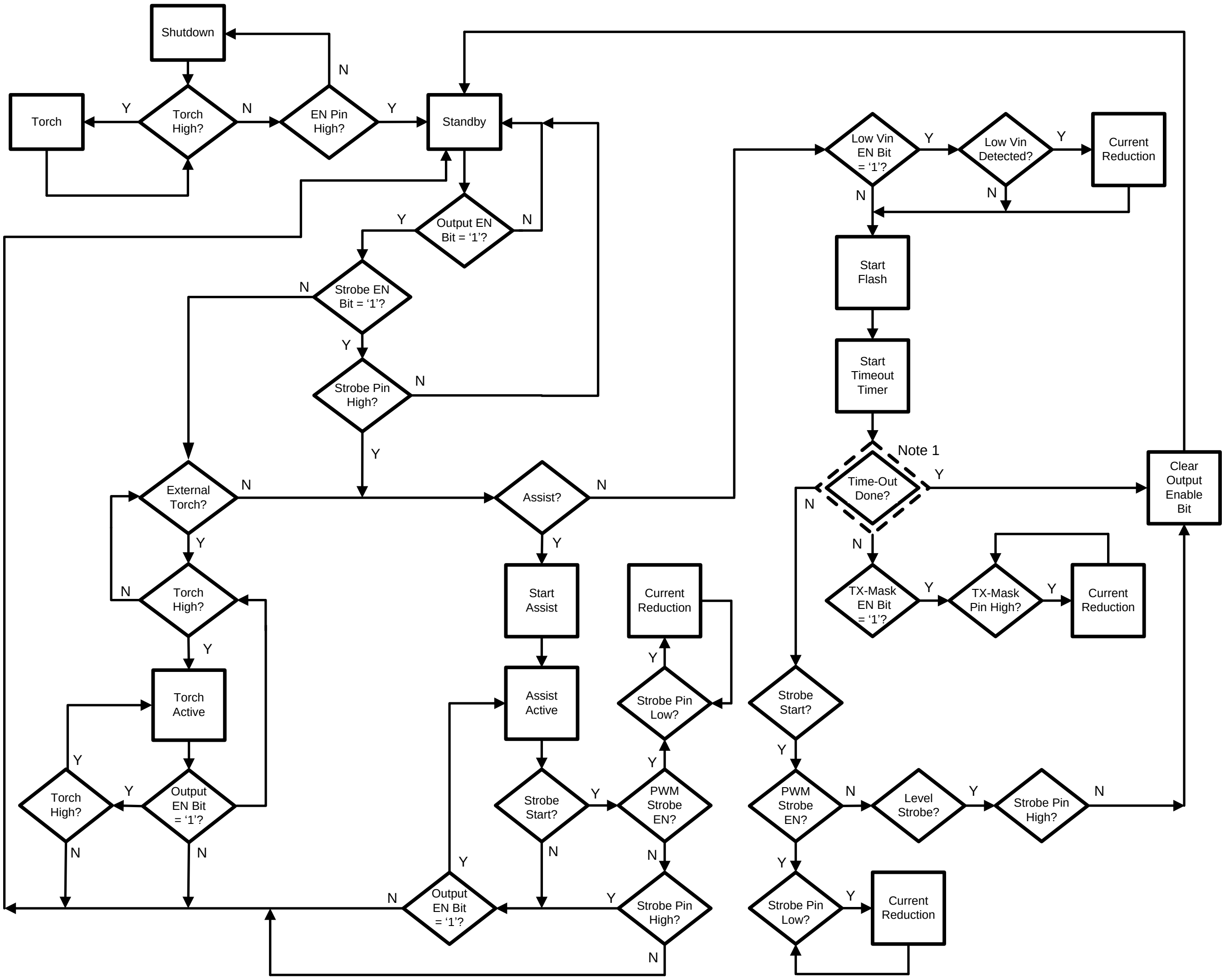
IVD7-IVD0: ADC Input Voltage Measurement Data

LED Voltage ADC Register
Address: 0x0B

Definition:	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Default:	0	0	0	0	0	0	0	0

LED7-LED0: ADC LED Voltage Measurement Data

Control State Diagram



Note 1: Flash time-out is always checked during flash.
Flash is terminated when time-out is done.

I²C Mode Truth Table

OEN	OM1	OM0	ETEN	SEN	TORCH	STROBE	Mode
0	0	0	0	X	X	X	Standby
0	0	0	1	X	0	X	Standby
0	0	0	1	X	1	X	Ext Torch
0	0	1	X	X	X	X	Standby
0	1	0	X	X	X	X	Standby
0	1	1	X	X	X	X	Standby
1	0	0	X	X	0	X	Standby
1	0	0	1	X	1	X	Ext Torch
1	0	1	X	0	X	X	RFU
1	1	0	X	0	X	X	Assist
1	1	1	X	0	X	X	Internal Flash
1	0	0	X	1	X	0	Standby
1	0	1	X	1	X	1	RFU
1	1	0	X	1	X	1	Strobe Assist
1	1	1	X	1	X	1	Strobe Flash

APPLICATION INFORMATION

Torch or Assist (Continuous Current) Operation

There are two different continuous current modes on the LM3565: Torch and Assist.

Torch Mode is enabled through the use of the dedicated Torch pin. The Torch pin functionality can be enabled and disabled by setting the value of the ETEN bit in the TX-Control Register (Address 0x03). ETEN = '1' allows an external Torch while ETEN = '0' does not.

The primary method to enable Assist Mode is by setting the Output Mode bits (OM1 and OM0) to '10' and setting the Output Enable bit (OEN) to a '1' in the Control Register (0x07). Assist Mode will remain active in I^2C-compatible Mode until the OEM bit is set to '0'.

The secondary Assist Mode enabling method involves using the Strobe pin. By setting the SEN bit in the Stobe Signaling Register (Address 0x06) to a '1', then setting the Output Mode bits (OM1 and OM0) to '10' and setting the Output Enable bit (OEN) to a '1' in the Control Register (0x07), the LM3565 will be configured to enable Assist Mode upon the Strobe pin transitioning state from low to high. In this configuration, Assist Mode will remain active until the OEN bit is set to '0'. Transitioning the Strobe pin from high to low does not automatically clear the OEN. In Assist Mode, the Strobe Signal Usage bit (SSU in Strobe Signaling Register 0x06) is ignored, and the Strobe pin is always set to be edge sensitive.

The LM3565 can drive two LEDs at continuous current levels of 60 mA or 90 mA. The current is set in the Current Set Register utilizing the AS0 bit (Address 0x02, AS0). Writing a '0' (default) sets the assist current to 60 mA while writing a '1' sets the assist current to 90 mA.

In Torch or Assist Mode, the LED current is ramped up to 90 mA in 30 mA steps at 20 µs intervals, then reduced to 60 mA if the assist target current is set to 60 mA. The assist current is terminated in one step.

Flash (Pulsed Current) Operation

A flash event using the LM3565 can be initiated though the I^2C-compatible control interface, and through the use of the Strobe pin.

When using the I^2C-compatible Control Mode, a flash event is initiated when the Output Mode bits (OM1 and OM0) are set to '11' and the Output Enable bit (OEN) is set to a '1' in the Control Register (0x07). In I^2C-compatible Mode, the flash event will remain active as long as the OEN bit is set to a '1' and will terminate upon a time-out event. The safety timer duration can be set in 2 ms intervals ranging from 2 ms to 512 ms by writing the desired value to the FT7-FT0 bits in the Timer Register (Address 0x05, with the default timer set to 72 msec.).

The Strobe pin provides added system flexibility in that it allows an additional external device (Camera Module, GPU etc.) to trigger a flash event. To initiate a Strobe event in I^2C-compatible Control Mode, the Strobe Enable (SEN) bit in the Strobe Signaling Register (0x06) must first be set to a '1', and the Output Enable (OEN) bits and Output Mode bits (OM1 and OM0) in the Control Register (Address 0x07) must be set to '1's.

Following the setting of the SEN and OEN bits, the user must choose to have an edge-sensitive or level-sensitive strobe event. Writing a '1' to the Strobe Signal Usage (SSU) bit in the Control Register (Address 0x06), the LM3565 will be configured to be level sensitive, while writing a '0' configures the part to be edge-sensitive. In both cases, the strobe flash event is started upon the Strobe pin being driven high.

In an edge-sensitive event, the flash duration will stay active until the flash duration timer lapses regardless of the state of the Strobe pin. If a level-sensitive strobe is used, the flash event will remain active as long as the Strobe pin is held high and as long as the flash duration time has not lapsed.

In Flash Mode, the LED current is ramped up and down in 30 mA steps at 20 µs intervals.

At the end of a flash event, whether initiated through the Control Register or Strobe pin, the LM3565 will force the OEN bit to a '0' and will place the LM3565 back into the Standby state.

Fault Protections

The LM3565 has a number of fault protection mechanisms designed to not only protect the LM3565 itself, but also to reset the system. Active fault protections include:

- Over-Voltage Protection (VOUT)
- Short-Circuit Protection (VOUT and VLED)
- Over-Temperature Protection
- Flash Time-Out
- Under-Voltage Lock-Out (UVLO)
- Output Capacitor Open Protection

In the event that any of these faults occur, the LM3565 will set a flag in the appropriate Fault Register (Address 0x08 or 0x09) and place the part into standby. Normal operation cannot resume until the fault has been fixed and an I^2C read of the fault register (0x08 and/or 0x09) has been completed. All faults are cleared upon reading the Fault Registers (0x08 and 0x09).

Output Over-Voltage Protection (OVP)

An OVP fault is triggered when the output voltage of the LM3565 reaches a value greater than 9.5V (typ). The OVP condition is cleared when the output voltage (V_{OUT}) is able to operate below 9.5V. An output capacitor or an LED that have become an open circuit can cause an OVP event to occur. This fault is reported to the OVP fault bit in the Fault Register (bit7 in address 0x05).

Output and LED Short Circuit Protection (SC)

An SC fault is triggered when the output voltage (VOUT) and/or the LED voltage (VLED) does not reach 0.8V in 0.5 ms. The short circuit condition is cleared when the output (VOUT) is allowed to reach its steady state target and when the LED voltage rises above 0.8V. A shorted output capacitor or a shorted LED could cause this fault to occur. This fault is reported to the SC fault bit in the Fault Register (bit6 in address 0x08).

Over-Temperature Protection (OTP)

An OTP fault is triggered when the diode junction temperature of the LM3565 reaches an internal temperature of around 150°C. The OTP condition is cleared when the junction temperature falls below 115°C and the fault register is read. A printed circuit board (PCB) with poor thermal dissipation properties and very high ambient temperatures (greater that 85°C) could cause this fault to occur. Refer to Texas Instruments Application Note: AN-1112: DSBGA Wafer Level Chip Scale Package for more information regarding proper PCB layout. This fault is reported to the OTP fault bit in the Fault Register (bit5 in address 0x08).

Flash Time-Out (TO)

The TO fault will be triggered whenever a flash is initiated with a level-sensitive Strobe event controlled by a camera module and the Strobe pulse duration exceeds the selected Flash Time-out duration. This fault is reported to the TO fault bit in the Fault Register (bit4 in address 0x08). This bit only gets set when PWM Mode is disabled.

Under-Voltage Lock-Out (UVLO)

An Under-Voltage Lock-Out (UVLO) fault occurs when the input voltage at the LM3565 drops below 2.4V (typ). When this fault occurs, the LM3565 will be forced into Standby Mode and the UVLO bit will be set to a '1'. To exit a UVLO state, the input voltage to the LM3565 must increase by 100 mV (typ.) and the UVLO Fault bit must be cleared. This fault is reported to the UVLO fault bit in the Fault Register (bit0 in address 0x08).

Output Capacitor Open Protection (CO)

An Output Capacitor Open fault is triggered when the LM3565 detects that the capacitance at the VOUT pin has dropped below the acceptable value (typically 0.1 µF). This fault indicates that the output capacitors are either disconnected or damaged and is reported to the Output Capacitor fault bit in the ADC Control Register (bit4 in address 0x09). Once an Output Capacitor Open fault is detected, the State Machine Reset bit (LVRS) in the Low Voltage Control register (0x04) has to bo toggled between a '1' and a '0' in order for normal operation to resume.

Input Low Voltage Flag (ILV)

The LM3565 has an Input Low Voltage (ILV) detection mechanism that sets the ILV flag (bit1 in address 0x08) when this feature is enabled (LVEN = 1, bit6 in address 0x04) and the input voltage is below the threshold set in the Low Voltage Control Register (LVL2-LVL0 in address 0x04). The input voltage is only monitored before the start of a flash event. This is a reporting flag bit and not a fault bit. The ILV flag bit does not halt or reset the LM3565.

TX-Mask Flag (TXM)

The LM3565 has a Transmit Interrupt flag bit (TXM, bit 3 in address 0x08) that gets set if the TX-Mask feature is enabled (TXEN = 1, bit7 in address 0x03) and if the TX-Mask pin is high, indicating a TX-Mask event. This is a reporting flag bit and not a fault bit. The TXM flag bit does not halt or reset the LM3565.

Table 9. Application Circuit Components List

Component	Manufacturer	Value	Part Number	Current/Voltage Rating (Resistance)
L	Toko	1µH	1239AS-H-1R0N	I_{SAT} = 3A (59 mΩ)
COUT1, COUT2	Murata	10 µF	GRM21BR61C106KE15	16 V
CIN1	Murata	10 µF	GRM188R60J106ME47	6.3 V
CIN2	Murata	0.1 µF	GRM155R71C104KA88	16 V

Inductor Current Limit

To prevent damage to the LM3565's inductor and to limit the power drawn by the LM3565 during a flash event, an Inductor Current Limit circuit is present. The LM3565 monitors the current through the inductor during the charge phase of the boost cycle. In the event that the inductor current reaches the current limit, the NFET of the converter will terminate the charge phase for that cycle. The process will repeat itself until the flash event has ended or until the input voltage increases to the point where the peak current is no longer reached. Hitting the peak inductor current limit will not disable the part. It will however limit the output power delivery to the LEDs.

The inductor current limit can be set to 2.3A, 2.6A (default), 2.9A or 3.3A depending on the values of the ICL1 and ICL0 bits in the TX-Masking Register (Address 0x03). The peak inductor current limit value can be used to help size the inductor to the appropriate saturation current level. For more information on inductor sizing, refer to the INDUCTOR SELECTION section of this datasheet.

Inductor Selection

The LM3565 is designed to use a 1µH inductor. When the device is boosting ($V_{OUT} > V_{IN}$) the inductor is one of the biggest sources of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the LM3565. This prevents excess efficiency loss that can occur with inductors that operate in saturation and prevents over-heating of the inductor and possible damage. For proper inductor operation and circuit performance ensure that the inductor saturation and the peak current limit setting of the LM3565 (2.3A, 2.6A (default), 2.9A or 3.3A) is greater than I_{PEAK}. I_{PEAK} can be calculated by:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L$$

where

$$\Delta I_L = \frac{V_{IN} \times \left(V_{OUT} - V_{IN}\right)}{2 \times f_{SW} \times L \times V_{OUT}}$$

Capacitor Selection

The LM3565 requires 3 external capacitors for proper operation (C_{IN} = 10 µF recommended (4.7 µF min) and 2 × C_{OUT} = 10 µF). An additional 0.1 µF input capacitor placed right next to the VIN pin is recommended. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low equivalent series resistance (ESR <20 mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM3565 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM3565. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over −55°C to 125°C; X5R: ±15% over −55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM3565. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, −20%) and vary significantly over temperature (Y5V: +22%, −82% over −30°C to +85°C range; Z5U: +22%, −56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM3565.

The recommended voltage rating for the input capacitor is 10V (min = 6.3V). The recommended output capacitor voltage rating is 16V (min = 10V). The recommended value takes into account the DC bias capacitance losses, while the minimum rating takes into account the OVP trip levels.

Layout Considerations

The DSBGA is a chip-scale package with good thermal properties. For more detailed instructions on handling and mounting DSBGA packages, refer to Texas Instruments Application Note AN-1112.

The high switching frequencies and large peak currents make the PCB layout a critical part of the design. The proceeding steps must be followed to ensure stable operation and proper current source regulation.

1. Connect the inductor as close as possible to the SW pin. This reduces the inductance and resistance of the switching node which minimizes ringing and excess voltage drops.
2. Connect the return terminals of the input capacitor and the output capacitor as close as possible to the PGND pins and through low impedance traces.
3. Bypass V_{IN} with a 10 µF ceramic capacitor and an additional 0.1 µF ceramic capacitor. Connect the positive terminal of this capacitor as close as possible to V_{IN}.
4. Connect C_{OUT} as close as possible to the V_{OUT} pin. This reduces the inductance and resistance of the output bypass node which minimizes ringing and voltage drops. This will improve efficiency and decrease the noise injected into the current sources.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3565TLE/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3565	Samples
LM3565TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3565	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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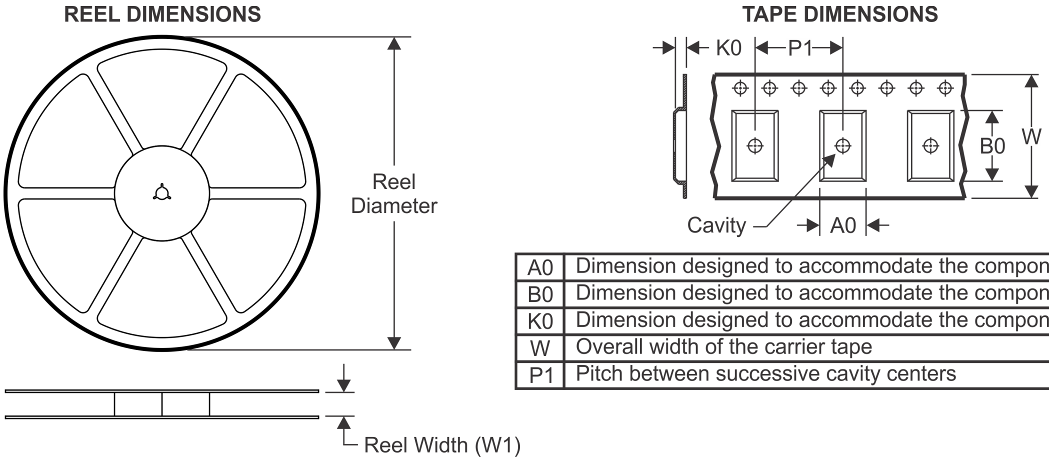
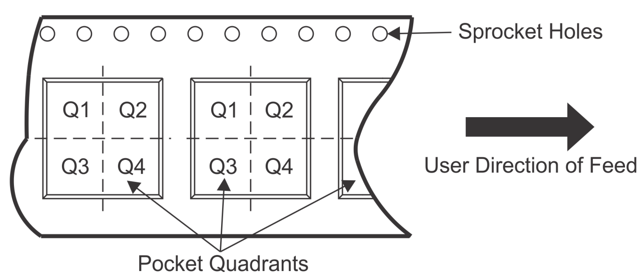
TAPE AND REEL INFORMATION



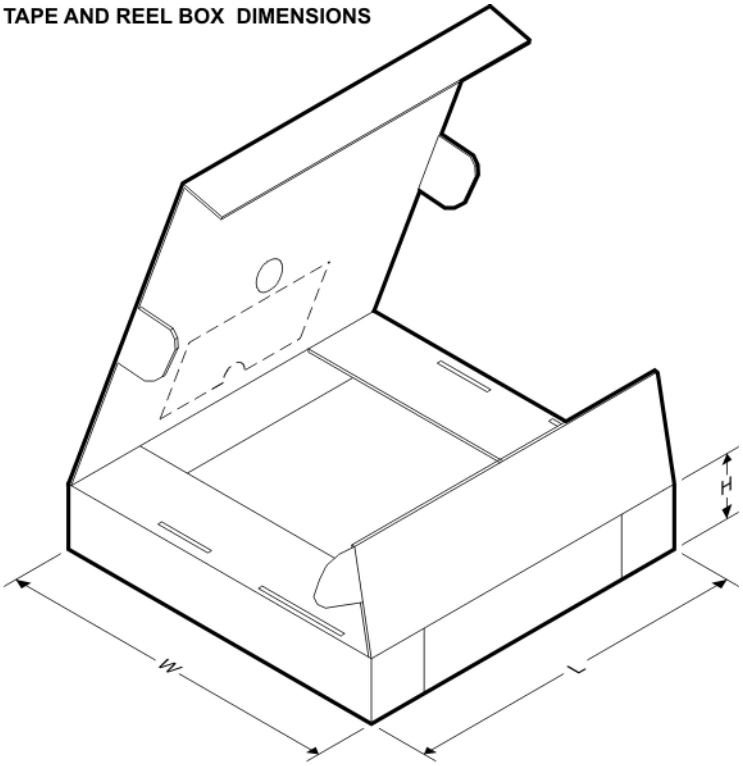
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3565TLE/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.18	2.18	0.76	4.0	8.0	Q1
LM3565TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.18	2.18	0.76	4.0	8.0	Q1

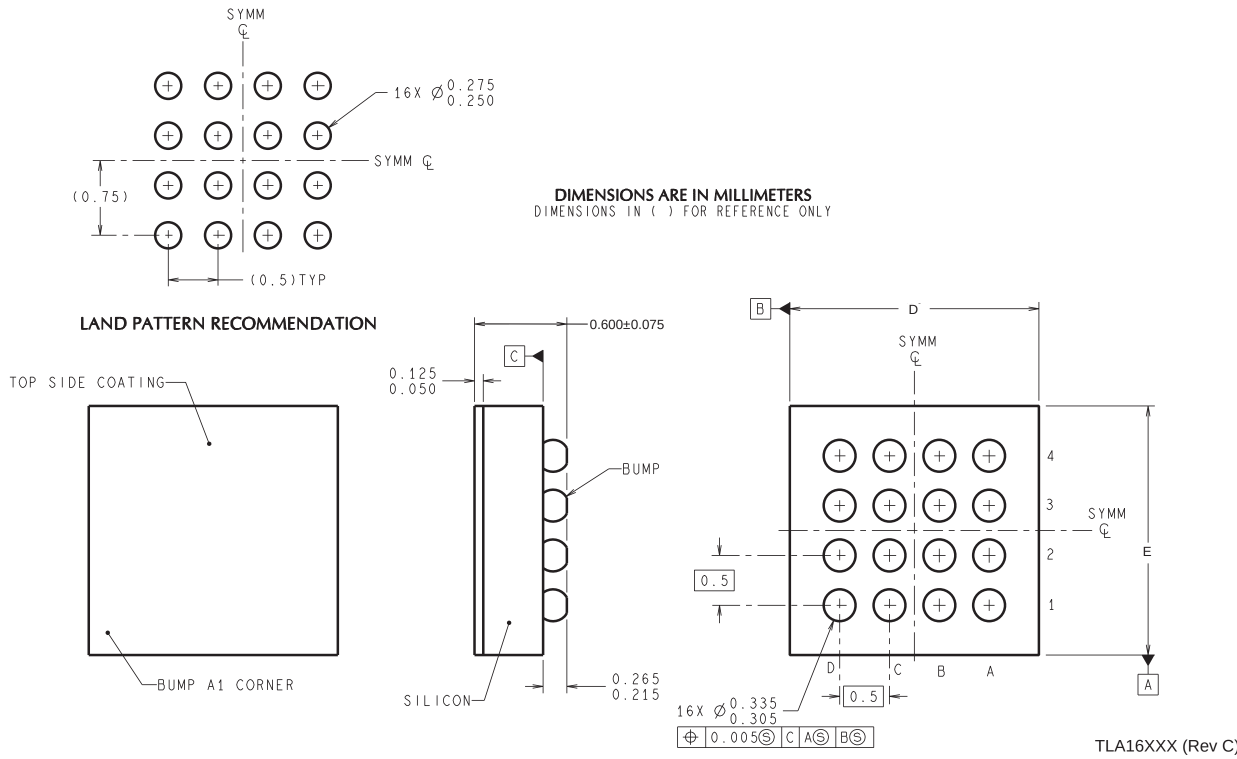
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3565TLE/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM3565TLX/NOPB	DSBGA	YZR	16	3000	210.0	185.0	35.0

YZR0016



D: Max = 2.015 mm, Min =1.955 mm

E: Max = 2.015 mm, Min =1.955 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.