

# Ultra Series<sup>™</sup> Crystal Oscillator Si540 Data Sheet

## Ultra Low Jitter Any-Frequency XO (125 fs), 0.2 to 1500 MHz

The Si540 Ultra Series<sup>™</sup> oscillator utilizes Silicon Laboratories' advanced 4<sup>th</sup> generation DSPLL® technology to provide an ultra-low jitter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 1500 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. The Si540 offers excellent reliability and frequency stability as well as guaranteed aging performance. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in industry-standard footprints, the Si540 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples 1-2 weeks after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si540 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. This process also guarantees 100% electrical testing of every device. The Si540 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.







Pin #	Descriptions
1, 2	Selectable via ordering option OE = Output enable; NC = No connect
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output. Not used for CMOS.
6	VDD = Power supply

#### KEY FEATURES

- · Available with any frequency from 0.2 MHz to 1500 MHz
- · Very low jitter: 125 fs Typ RMS (12 kHz - 20 MHz)
- · Excellent PSNR and supply noise immunity: -80 dBc Typ
- 7 ppm stability option (-40 to 85C)
- + 3.3 V, 2.5 V and 1.8 V  $V_{\text{DD}}$  supply operation from the same part number
- · LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 2.5×3.2, 3.2×5, 5x7 mm package footprints
- Any custom frequency available with 1-2 week lead times

#### APPLICATIONS

- · 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- · Servers, switches, storage, NICs, search acceleration
- · Test and measurement
- · Clock and data recovery
- FPGA/ASIC clocking



## 1. Ordering Guide

The Si540 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.



#### Notes:

- 1. Contact Silicon Labs for non-standard configurations.
- 2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
- 3. For example: 156.25 MHz = 156M250; 25 MHz = 25M0000. Create custom part numbers at www.silabs.com/oscillators.

#### 1.1 Technical Support

Frequently Asked Questions (FAQ)	www.silabs.com/Si540-FAQ
Oscillator Phase Noise Lookup Utility	www.silabs.com/oscillator-phase-noise-lookup
Quality and Reliability	www.silabs.com/quality
Development Kits	www.silabs.com/oscillator-tools

## 2. Electrical Specifications

## Table 2.1. Electrical Specifications

 $V_{DD}$  = 1.8 V, 2.5 or 3.3 V ± 5%,  $T_A$  = –40 to 85 °C

Parameter	Symbol	Test Condition/Comment	Min	Тур	Max	Unit
Temperature Range	T <sub>A</sub>		-40	—	85	°C
Frequency Range	F <sub>CLK</sub>	LVPECL, LVDS, CML	0.2	_	1500	MHz
		HCSL	0.2	_	400	MHz
		CMOS, Dual CMOS	0.2	_	250	MHz
Supply Voltage	V <sub>DD</sub>	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	I <sub>DD</sub>	LVPECL (output enabled)	_	100	145	mA
		LVDS/CML (output enabled)	_	75	111	mA
		HCSL (output enabled)	_	80	125	mA
		CMOS (output enabled)	_	74	108	mA
		Dual CMOS (output enabled)	—	80	125	mA
		Tristate Hi-Z (output disabled)	_	64	100	mA
Temperature Stability		Frequency stability Grade A	-20	_	20	ppm
		Frequency stability Grade B	-10		10	ppm
		Frequency stability Grade C	-7	_	7	ppm
Total Stability <sup>1</sup>	F <sub>STAB</sub>	Frequency stability Grade A	-50	_	50	ppm
		Frequency stability Grade B	-25	_	25	ppm
		Frequency stability Grade C	-20	_	20	ppm
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>	LVPECL/LVDS/CML	_	—	350	ps
(20% to 80% V <sub>PP</sub> )		CMOS / Dual CMOS (C <sub>L</sub> = 5 pF)	—	0.5	1.5	ns
		HCSL, F <sub>CLK</sub> >50 MHz		_	550	ps
Duty Cycle	D <sub>C</sub>	All formats	45	_	55	%
Output Enable (OE) <sup>2</sup>	V <sub>IH</sub>		0.7 × V <sub>DD</sub>		—	V
	VIL		_	_	0.3 × V <sub>DD</sub>	V
	T <sub>D</sub>	Output Disable Time, F <sub>CLK</sub> >10 MHz	_	_	3	μs
	T <sub>E</sub>	Output Enable Time, F <sub>CLK</sub> >10 MHz	_	_	20	μs
Powerup Time	tosc	Time from $0.9 \times V_{DD}$ until output fre- quency ( $F_{CLK}$ ) within spec—10		10	ms	
LVPECL Output Option <sup>3</sup>	V <sub>OC</sub>	Mid-level	V <sub>DD</sub> – 1.42	_	V <sub>DD</sub> – 1.25	V
	Vo	Swing (diff)	1.1	_	1.9	V <sub>PP</sub>

Parameter	Symbol	Test Condition/Comment	Min	Тур	Max	Unit
LVDS Output Option <sup>4</sup>	V <sub>OC</sub>	Mid-level (2.5 V, 3.3 V VDD)	1.125	1.20	1.275	V
		Mid-level (1.8 V VDD)	0.8	0.9	1.0	V
	Vo	Swing (diff)	0.5	0.7	0.9	V <sub>PP</sub>
HCSL Output Option <sup>5</sup>	V <sub>OH</sub>	Output voltage high	660	750	850	mV
	V <sub>OL</sub>	Output voltage low	-150	0	150	mV
	V <sub>C</sub>	Crossing voltage	250	350	550	mV
CML Output Option (AC-Coupled)	Vo	Swing (diff)	0.6	0.8	1.0	V <sub>PP</sub>
CMOS Output Option	V <sub>OH</sub>	I <sub>OH</sub> = 8/6/4 mA for 3.3/2.5/1.8V VDD	$0.85 \times V_{DD}$		_	V
	V <sub>OL</sub>	I <sub>OL</sub> = 8/6/4 mA for 3.3/2.5/1.8V VDD	—	—	0.15 × V <sub>DD</sub>	V

#### Notes:

1. Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 °C.

2. OE includes a 50 k $\Omega$  pull-up to VDD for OE active high. Includes a 50 k $\Omega$  pull-down to GND for OE active low. NC (No Connect) pins include a 50 k $\Omega$  pull-down to GND.

3.50  $\Omega$  to  $V_{DD}$  – 2.0 V.

4.  $R_{term}$  = 100  $\Omega$  (differential).

5.50  $\Omega$  to GND.

#### Table 2.2. Clock Output Phase Jitter and PSNR

## $V_{DD}$ = 1.8 V, 2.5 or 3.3 V $\pm$ 5%, $T_A$ = –40 to 85 °C

Parameter	Symbol	Test Condition/Comment	Min	Тур	Мах	Unit
Phase Jitter (RMS, 12kHz - 20MHz) <sup>1</sup>	фJ	Differential Formats	—	125	200	fs
2.5 x 3.2 mm, 3.2 x 5 mm, F <sub>CLK</sub> ≥ 100 MHz		CMOS, Dual CMOS	_	200	_	fs
Phase Jitter (RMS, 12kHz - 20MHz) <sup>1</sup> 5 x 7 mm, F <sub>CLK</sub> ≥ 100 MHz		Differential Formats	—	150	200	fs
		CMOS, Dual CMOS	_	200	_	fs
Spurs Induced by External Power Supply	PSNR	100 kHz sine wave		-83	_	
Output		200 kHz sine wave	—	-83	—	dPo
		500 kHz sine wave	_	-82	—	UDC
		1 MHz sine wave	—	-85	—	
Note:	·		•		•	·

1. Guaranteed by characterization. Jitter inclusive of any spurs.

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-110	-107	-99	
1 kHz	–121	–120	-109	
10 kHz	–132	-130	–121	
100 kHz	–139	–137	–127	dBc/Hz
1 MHz	–151	-149	–138	
10 MHz	-160	-161	-155	
20 MHz	–161	-162	-157	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	–113	-110	-100	
1 kHz	-123	-120	-110	
10 kHz	–133	–130	–119	
100 kHz	–139	–137	–127	dBc/Hz
1 MHz	–151	-149	–138	
10 MHz	-162	-166	-156	
20 MHz	-163	-167	-157	





Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.



#### Table 2.4. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL): 3.2 x 5, 5 x 7 packages	1
Moisture Sensitivity Level (MSL): 2.5 x 3.2 package	2
Contact Pads	Gold over Nickel

Note:

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/ quality/Pages/RoHSInformation.aspx.

#### Table 2.5. Thermal Conditions

#### Max Junction Temperature = 125° C

Package	Parameter	Symbol	Test Condition	Value	Unit
	Thermal Resistance Junction to Ambient	Θ <sub>JA</sub>	Still Air, 85 °C	80	°C/W
2.5 x 3.2 mm 6-pin DFN	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	39	°C/W
	Thermal Parameter Junction to Top Center	$\Psi_{JT}$	Still Air, 85 °C	17	°C/W
	Thermal Resistance Junction to Ambient	Θ <sub>JA</sub>	Still Air, 85 °C	55	°C/W
3.2 × 5 mm 6-pin CLCC	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	20	°C/W
·	Thermal Parameter Junction to Top Center	$\Psi_{JT}$	Still Air, 85 °C	20	°C/W
	Thermal Resistance Junction to Ambient	Θ <sub>JA</sub>	Still Air, 85 °C	53	°C/W
5 × 7 mm 6-pin CLCC	Thermal Parameter Junction to Board	$\Psi_{JB}$	Still Air, 85 °C	26	°C/W
,	Thermal Parameter Junction to Top Center	$\Psi_{JT}$ Still Air, 85 °C17°C/V $\Theta_{JA}$ Still Air, 85 °C55°C/V $\Psi_{JB}$ Still Air, 85 °C20°C/V $\Psi_{JT}$ Still Air, 85 °C20°C/V $\Theta_{JA}$ Still Air, 85 °C53°C/V $\Psi_{JB}$ Still Air, 85 °C26°C/V $\Psi_{JB}$ Still Air, 85 °C26°C/V $\Psi_{JT}$ Still Air, 85 °C26°C/V	°C/W		
Nata	1	1			

Note:

1. Based on PCB Dimensions: 4.5" x 7", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.

#### Table 2.6. Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	T <sub>AMAX</sub>	95	°C
Storage Temperature	T <sub>S</sub>	–55 to 125	°C
Supply Voltage	V <sub>DD</sub>	-0.5 to 3.8	°C
Input Voltage	V <sub>IN</sub>	–0.5 to V <sub>DD</sub> + 0.3	V
ESD HBM (JESD22-A114)	НВМ	2.0	kV

Parameter	Symbol	Rating	Unit
Solder Temperature <sup>2</sup>	T <sub>PEAK</sub>	260	°C
Solder Time at T <sub>PEAK</sub> <sup>2</sup>	Τ <sub>Ρ</sub>	20–40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. The device is compliant with JEDEC J-STD-020.

## 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si540 device.



Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

## 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.



Figure 4.1. LVPECL Output Terminations

AC Coupled LVPECL Termination Resistor Values			Teri	DC Coupled LVPECL mination Resistor Va	Iues	
VDD	R1	R2	Rp	VDD	R1	R2
3.3 V	127 Ω	82.5 Ω	130 Ω	3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω	2.5 V	250 Ω	62.5 Ω







Figure 4.3. CML and CMOS Output Terminations

## 5. Package Outline

#### 5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si540. The table below lists the values for the dimensions shown in the illustration.





Table 5.1.	Package	Diagram	Dimensions	(mm)
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Dimension	Min	Nom	Мах	Dimension	Min	Nom	Мах
А	1.13	1.28	1.43	L	1.17	1.27	1.37
A2	0.50	0.55	0.60	L1	0.05	0.10	0.15
A3	0.50	0.55	0.60	р	1.70	_	1.90
b	1.30	1.40	1.50	R		0.70 REF	
С	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb		0.15	
D1	4.30	4.40	4.50	CCC		0.08	
е	2.54 BSC			ddd		0.10	
E	7.00 BSC			eee		0.05	
E1	6.10	6.20	6.30				

#### Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

#### 5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si540. The table below lists the values for the dimensions shown in the illustration.



Figure 5.2. Si540 (3.2×5 mm) Outline Diagram

Dimension	Min	Nom	Мах		
A	1.06	1.17	1.33		
b	0.54	0.64	0.74		
С	0.35	0.45	0.55		
D		3.20 BSC			
D1	2.55	2.60	2.65		
e		1.27 BSC			
E		5.00 BSC			
E1	4.35	4.40	4.45		
Н	0.45	0.55	0.65		
L	0.80	0.90	1.00		
L1	0.05	0.10	0.15		
р	1.36	1.46	1.56		
R		0.32 REF			
ааа	aaa		0.15		
bbb		0.15			
ccc	0.08				
ddd	0.10				
eee	0.05				

#### Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

#### 5.3 Package Outline (2.5x3.2 mm)

The figure below illustrates the package details for the 2.5x3.2 mm Si540. The table below lists the values for the dimensions shown in the illustration.





Table 5.3.	Package	Diagram	Dimensions	(mm)	)
------------	---------	---------	------------	------	---

Min	Nom	Мах
0.90	0.95	1.00
	0.36 REF	
0.53 REF		
0.55 0.60 0.65		0.65
3.2 BSC		
2.5 BSC		
1.10 BSC		
0.65 0.70 0.75		
5		
2.2 BSC		
1.589 BSC		
0.10		
0.10		
0.08		
	Min 0.90 0.55 0.65	Min Nom   0.90 0.95   0.36 REF 0.53 REF   0.55 0.60   3.2 BSC 3.2 BSC   2.5 BSC 1.10 BSC   0.65 0.70   5 2.2 BSC   1.589 BSC 0.10   0.10 0.08

Notes:

1. The dimensions in parentheses are reference.

2. All dimensions in millimeters (mm).

3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

# 6. PCB Land Pattern

## 6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.



Figure 6.1. Si540 (5×7 mm) PCB Land Pattern

#### Table 6.1. PCB Land Pattern Dimensions (mm)

C1 4.20	
E 2.54	
X1 1.55	
Y1 1.95	

Notes:

#### General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

#### Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1.

## Card Assembly

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

#### 6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.



Figure 6.2. Si540 (3.2×5 mm) PCB Land Pattern

#### Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

#### Notes:

#### General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

#### Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 1:1.

#### **Card Assembly**

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

#### 6.3 PCB Land Pattern (2.5×3.2 mm)

The figure below illustrates the 2.5×3.2 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.



Figure 6.3. Si540 (2.5×3.2 mm) PCB Land Pattern

#### Table 6.3. PCB Land Pattern Dimensions (mm)

Dimension	Description	Value (mm)
X1	Width - leads on long sides	0.85
Y1	Height - leads on long sides	0.7
D1	Pitch in X directions of XLY1 leads	1.639
E1	Lead pitch XLY1 leads	1.10

**Notes:** The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

#### General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.
- 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

#### Stencil Design

- 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 2. The stencil thickness should be 0.125 mm (5 mils).
- 3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

#### **Card Assembly**

- 1. A No-Clean, Type-3 solder paste is recommended.
- 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Top Marking (5x7 and 3.2x5 Packages)

The figure below illustrates the mark specification for the Si540 5x7 and 3.2x5 package sizes. The table below lists the line information.



Figure 7.1. Mark Specification

#### Table 7.1. Si540 Top Mark Description

Line	Position	Description
1	1–8	"Si540", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si540AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

## 8. Top Marking (2.5x3.2 Package)

The figure below illustrates the mark specification for the Si540 2.5x3.2 package sizes. The table below lists the line information.





#### Table 8.1. Si540 Top Mark Description

Line	Position	Description
1	1–6	A = Si540, CCCCC = Custom Mark Code
2		Trace Code
	1–6	6 digit trace code per assembly release instructions
3	Position 1	Pin 1 orientation mark (dot)
	Position 2–3	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 4–5	Calendar Work Week number (1–53), to be assigned by assembly site

## 9. Revision History

#### **Revision 1.1**

November 2019

Added 2.5x3.2 mm package option

## **Revision 1.0**

July 2018

Added 20 ppm total stability option.

## **Revision 0.75**

March, 2018

Added 25 ppm total stability option.

## **Revision 0.71**

December 11, 2017

• Added 5x7 package and land pattern.

## **Revision 0.7**

June 27, 2017

· Initial release.



#### Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specificant personal injury or death. Silicon Labs products are not designed or authorized to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs

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